

# NTMFS4933N

## Power MOSFET

### 30 V, 210 A, Single N-Channel, SO-8 FL

#### Features

- Low  $R_{DS(on)}$  to Improve Conduction and Overall Efficiency
- These Devices are Pb-Free, Halogen Free/BFR Free and are RoHS Compliant

#### Applications

- OR-ing FET, Power Load Switch, Motor Control
- Refer to Application Note AND8195/D for Mounting Information

#### End Products

- Server, UPS, Fault-Tolerant Power Systems, Hot Swap

#### MAXIMUM RATINGS ( $T_J = 25^\circ\text{C}$ unless otherwise stated)

Parameter	Symbol	Value	Unit
Drain-to-Source Voltage	$V_{DS}$	30	V
Gate-to-Source Voltage	$V_{GS}$	$\pm 20$	V
Continuous Drain Current $R_{\theta JA}$ (Note 1)	$I_D$	$T_A = 25^\circ\text{C}$	34
		$T_A = 100^\circ\text{C}$	21.5
Power Dissipation $R_{\theta JA}$ (Note 1)	$P_D$	2.74	W
Continuous Drain Current $R_{\theta JA} \leq 10$ s (Note 1)	$I_D$	$T_A = 25^\circ\text{C}$	43
		$T_A = 100^\circ\text{C}$	27
Power Dissipation $R_{\theta JA} \leq 10$ s (Note 1)	$P_D$	7.3	W
Continuous Drain Current $R_{\theta JA}$ (Note 2)	$I_D$	$T_A = 25^\circ\text{C}$	20
		$T_A = 100^\circ\text{C}$	12.5
Power Dissipation $R_{\theta JA}$ (Note 2)	$P_D$	1.06	W
Continuous Drain Current $R_{\theta JC}$ (Note 1)	$I_D$	$T_C = 25^\circ\text{C}$	210
		$T_C = 100^\circ\text{C}$	132
Power Dissipation $R_{\theta JC}$ (Note 1)	$P_D$	104	W
Pulsed Drain Current	$T_A = 25^\circ\text{C}, t_p = 10 \mu\text{s}$	$I_{DM}$	400
Operating Junction and Storage Temperature	$T_J, T_{STG}$	-55 to +150	$^\circ\text{C}$
Source Current (Body Diode)	$I_S$	95	A
Drain to Source DV/DT	$dV/dt$	4.4	V/ns
Single Pulse Drain-to-Source Avalanche Energy ( $T_J = 25^\circ\text{C}, V_{DD} = 24$ V, $V_{GS} = 10$ V, $I_L = 58$ A <sub>pk</sub> , $L = 0.3$ mH, $R_G = 25 \Omega$ )	$E_{AS}$	504	mJ
Lead Temperature for Soldering Purposes (1/8" from case for 10 s)	$T_L$	260	$^\circ\text{C}$

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

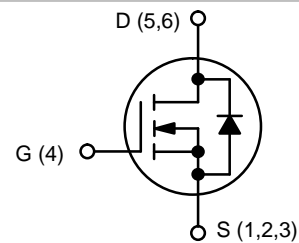
1. Surface-mounted on FR4 board using 1 sq-in pad, 1 oz Cu.
2. Surface-mounted on FR4 board using the minimum recommended pad size. (Cu area = 50 mm<sup>2</sup> [1 oz])



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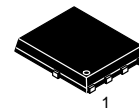
[www.onsemi.com](http://www.onsemi.com)

$V_{(BR)DSS}$	$R_{DS(ON)}$ MAX	$I_D$ MAX
30 V	1.2 m $\Omega$ @ 10 V	210 A
	2.0 m $\Omega$ @ 4.5 V	

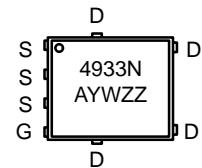


N-CHANNEL MOSFET

#### MARKING DIAGRAM



SO-8 FLAT LEAD  
CASE 488AA  
STYLE 1



- A = Assembly Location
- Y = Year
- W = Work Week
- ZZ = Lot Traceability

#### ORDERING INFORMATION

Device	Package	Shipping†
NTMFS4933NT1G	SO-8 FL (Pb-Free)	1500 / Tape & Reel
NTMFS4933NT3G	SO-8 FL (Pb-Free)	5000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

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## THERMAL RESISTANCE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Junction-to-Case (Drain)	$R_{\theta JC}$	1.1	°C/W
Junction-to-Ambient – Steady State (Note 3)	$R_{\theta JA}$	45.6	
Junction-to-Ambient – Steady State (Note 4)	$R_{\theta JA}$	117.5	
Junction-to-Ambient – ( $t \leq 10$ s) (Note 3)	$R_{\theta JA}$	17.13	

3. Surface-mounted on FR4 board using 1 sq-in pad, 1 oz Cu.

4. Surface-mounted on FR4 board using the minimum recommended pad size. (Cu area = 50 mm<sup>2</sup> [1 oz])

## ELECTRICAL CHARACTERISTICS ( $T_J = 25^\circ\text{C}$ unless otherwise specified)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
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### OFF CHARACTERISTICS

Drain-to-Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS} = 0$ V, $I_D = 250$ $\mu$ A	30			V
Drain-to-Source Breakdown Voltage Temperature Coefficient	$V_{(BR)DSS}/T_J$			15		mV/°C
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{GS} = 0$ V, $V_{DS} = 24$ V	$T_J = 25^\circ\text{C}$		1.0	$\mu$ A
			$T_J = 125^\circ\text{C}$		10	
Gate-to-Source Leakage Current	$I_{GSS}$	$V_{DS} = 0$ V, $V_{GS} = \pm 20$ V			$\pm 100$	nA

### ON CHARACTERISTICS (Note 5)

Gate Threshold Voltage	$V_{GS(TH)}$	$V_{GS} = V_{DS}$ , $I_D = 250$ $\mu$ A	1.2	1.6	2.2	V	
Negative Threshold Temperature Coefficient	$V_{GS(TH)}/T_J$			4.0		mV/°C	
Drain-to-Source On Resistance	$R_{DS(on)}$	$V_{GS} = 10$ V	$I_D = 30$ A		0.9	1.2	m $\Omega$
			$I_D = 15$ A		0.9		
		$V_{GS} = 4.5$ V	$I_D = 30$ A		1.5	2.0	
			$I_D = 15$ A		1.5		
Forward Transconductance	$g_{FS}$	$V_{DS} = 1.5$ V, $I_D = 15$ A		82		S	

### CHARGES, CAPACITANCES & GATE RESISTANCE

Input Capacitance	$C_{ISS}$	$V_{GS} = 0$ V, $f = 1$ MHz, $V_{DS} = 15$ V		10930		pF
Output Capacitance	$C_{OSS}$			3230		
Reverse Transfer Capacitance	$C_{RSS}$			92		
Total Gate Charge	$Q_{G(TOT)}$	$V_{GS} = 4.5$ V, $V_{DS} = 15$ V; $I_D = 30$ A		62.1		nC
Threshold Gate Charge	$Q_{G(TH)}$			15.7		
Gate-to-Source Charge	$Q_{GS}$			27		
Gate-to-Drain Charge	$Q_{GD}$			10.1		
Total Gate Charge	$Q_{G(TOT)}$		$V_{GS} = 10$ V, $V_{DS} = 15$ V; $I_D = 30$ A		148	

### SWITCHING CHARACTERISTICS (Note 6)

Turn-On Delay Time	$t_{d(ON)}$	$V_{GS} = 4.5$ V, $V_{DS} = 15$ V, $I_D = 15$ A, $R_G = 3.0$ $\Omega$		31		ns
Rise Time	$t_r$			33		
Turn-Off Delay Time	$t_{d(OFF)}$			47		
Fall Time	$t_f$			23		

5. Pulse Test: pulse width  $\leq 300$   $\mu$ s, duty cycle  $\leq 2\%$ .

6. Switching characteristics are independent of operating junction temperatures.

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## ELECTRICAL CHARACTERISTICS ( $T_J = 25^\circ\text{C}$ unless otherwise specified)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
<b>SWITCHING CHARACTERISTICS</b> (Note 6)						
Turn-On Delay Time	$t_{d(ON)}$	$V_{GS} = 10\text{ V}, V_{DS} = 15\text{ V},$ $I_D = 15\text{ A}, R_G = 3.0\ \Omega$		20		ns
Rise Time	$t_r$			26		
Turn-Off Delay Time	$t_{d(OFF)}$			88.6		
Fall Time	$t_f$			22		

## DRAIN-SOURCE DIODE CHARACTERISTICS

Forward Diode Voltage	$V_{SD}$	$V_{GS} = 0\text{ V},$ $I_S = 30\text{ A}$	$T_J = 25^\circ\text{C}$		0.82	1.1	V
			$T_J = 125^\circ\text{C}$		0.68		
Reverse Recovery Time	$t_{RR}$	$V_{GS} = 0\text{ V}, dI_S/dt = 100\text{ A}/\mu\text{s},$ $I_S = 30\text{ A}$			73.5		ns
Charge Time	$t_a$				35.9		
Discharge Time	$t_b$				37.6		
Reverse Recovery Charge	$Q_{RR}$				117		

## PACKAGE PARASITIC VALUES

Source Inductance	$L_S$	$T_A = 25^\circ\text{C}$		0.50		nH
Drain Inductance	$L_D$			0.005		nH
Gate Inductance	$L_G$			1.84		nH
Gate Resistance	$R_G$			1.1	2.2	$\Omega$

5. Pulse Test: pulse width  $\leq 300\ \mu\text{s}$ , duty cycle  $\leq 2\%$ .

6. Switching characteristics are independent of operating junction temperatures.

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

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## TYPICAL CHARACTERISTICS

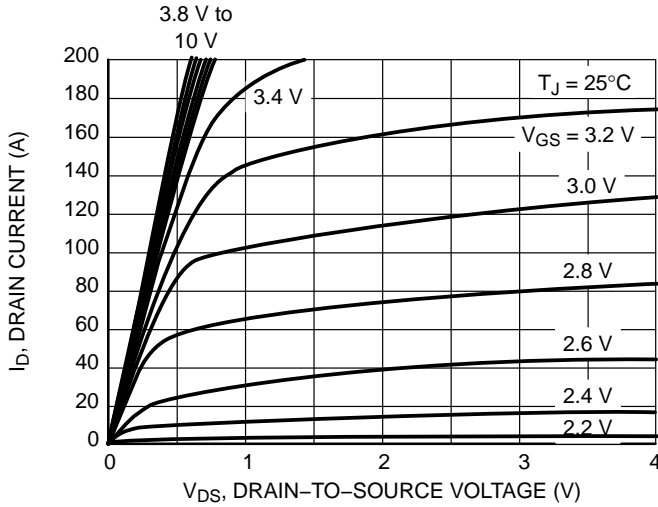


Figure 1. On-Region Characteristics

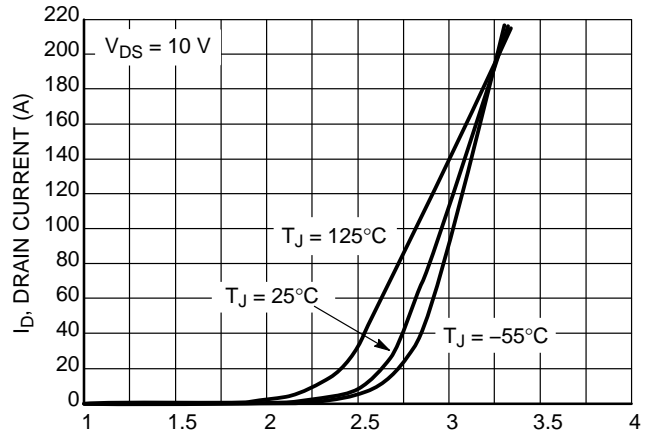


Figure 2. Transfer Characteristics

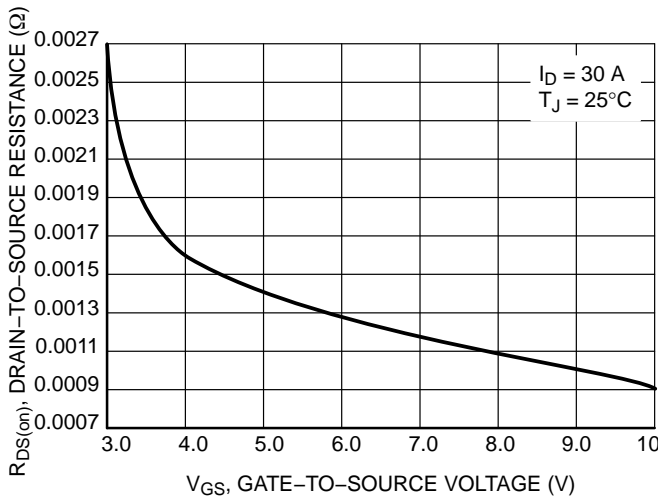


Figure 3. On-Resistance vs. Gate-to-Source Voltage

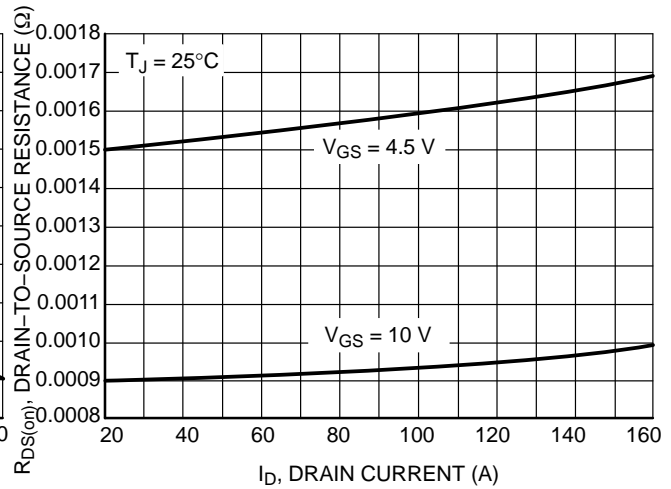


Figure 4. On-Resistance vs. Drain Current and Gate Voltage

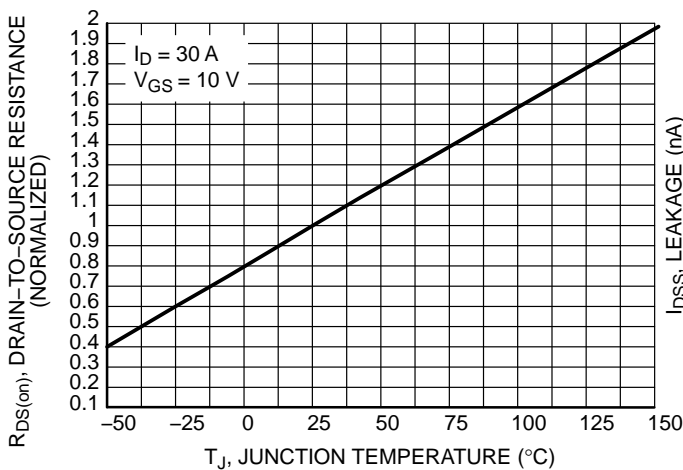


Figure 5. On-Resistance Variation with Temperature

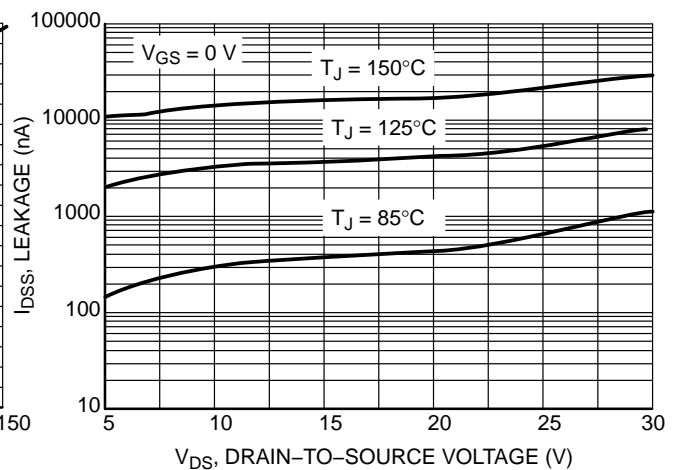


Figure 6. Drain-to-Source Leakage Current vs. Voltage

TYPICAL CHARACTERISTICS

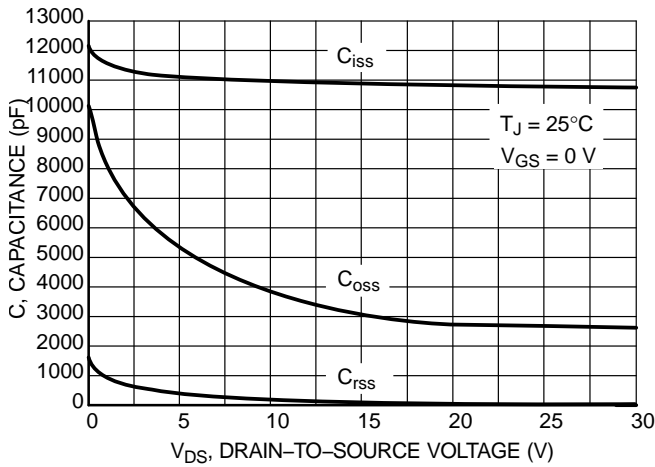


Figure 7. Capacitance Variation

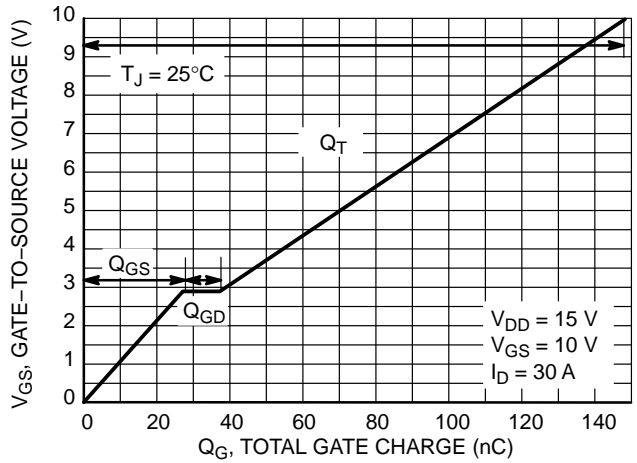


Figure 8. Gate-To-Source and Drain-To-Source Voltage vs. Total Charge

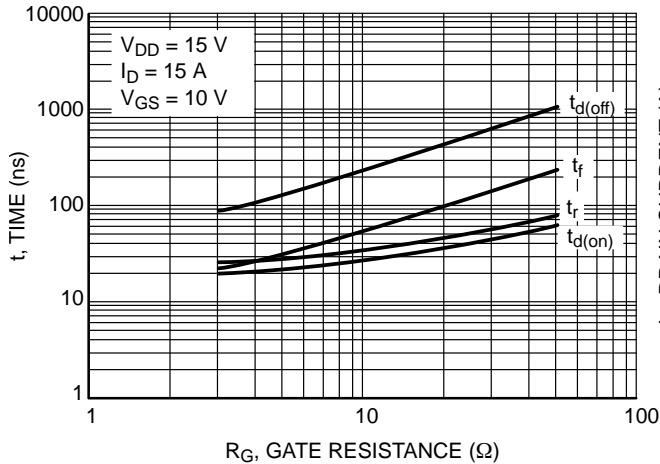


Figure 9. Resistive Switching Time Variation vs. Gate Resistance

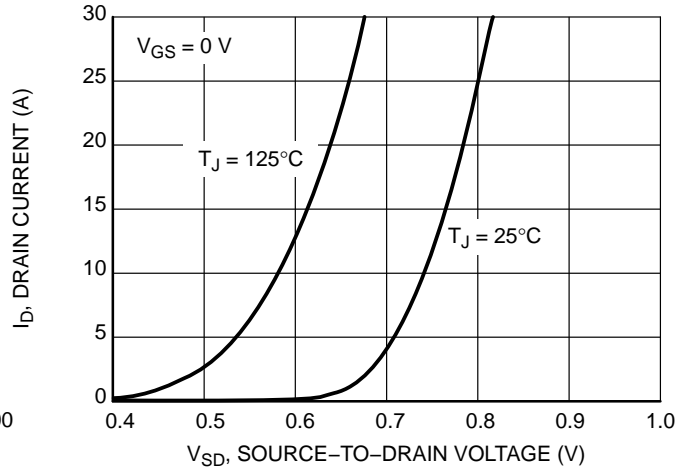


Figure 10. Diode Forward Voltage vs. Current

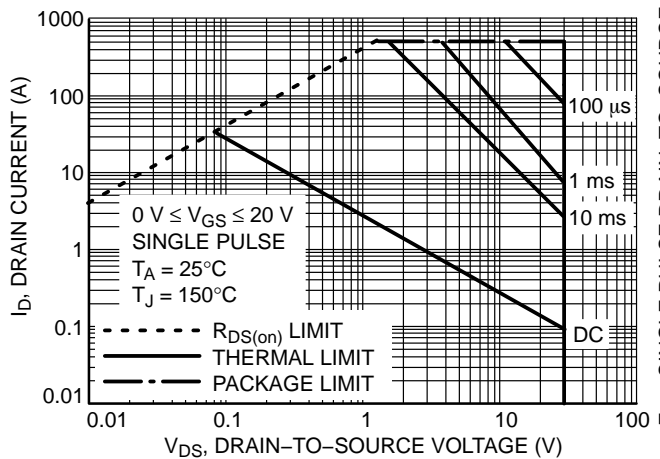


Figure 11. Maximum Rated Forward Biased Safe Operating Area

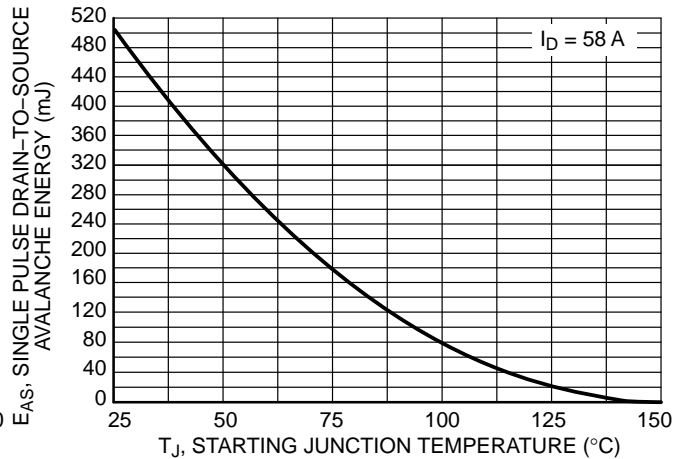


Figure 12. Maximum Avalanche Energy vs. Starting Junction Temperature

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## TYPICAL CHARACTERISTICS

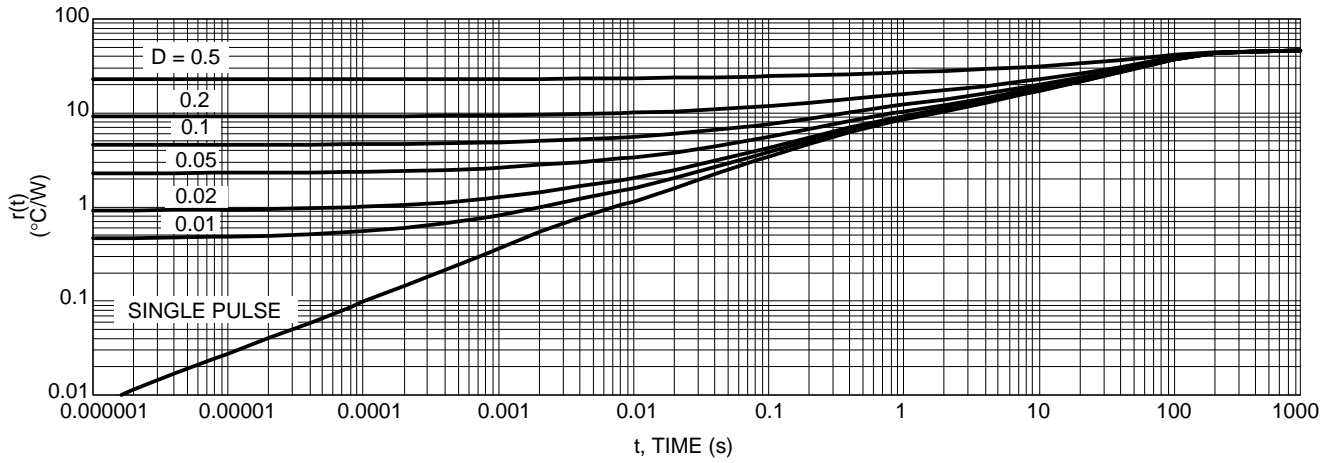


Figure 13. Thermal Response

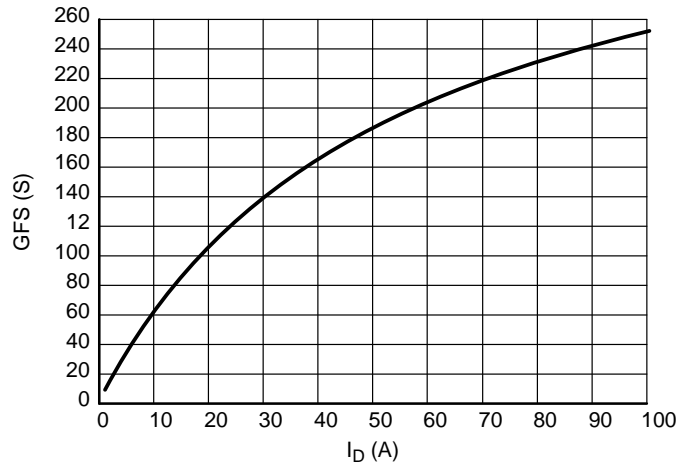


Figure 14. GFS vs.  $I_D$

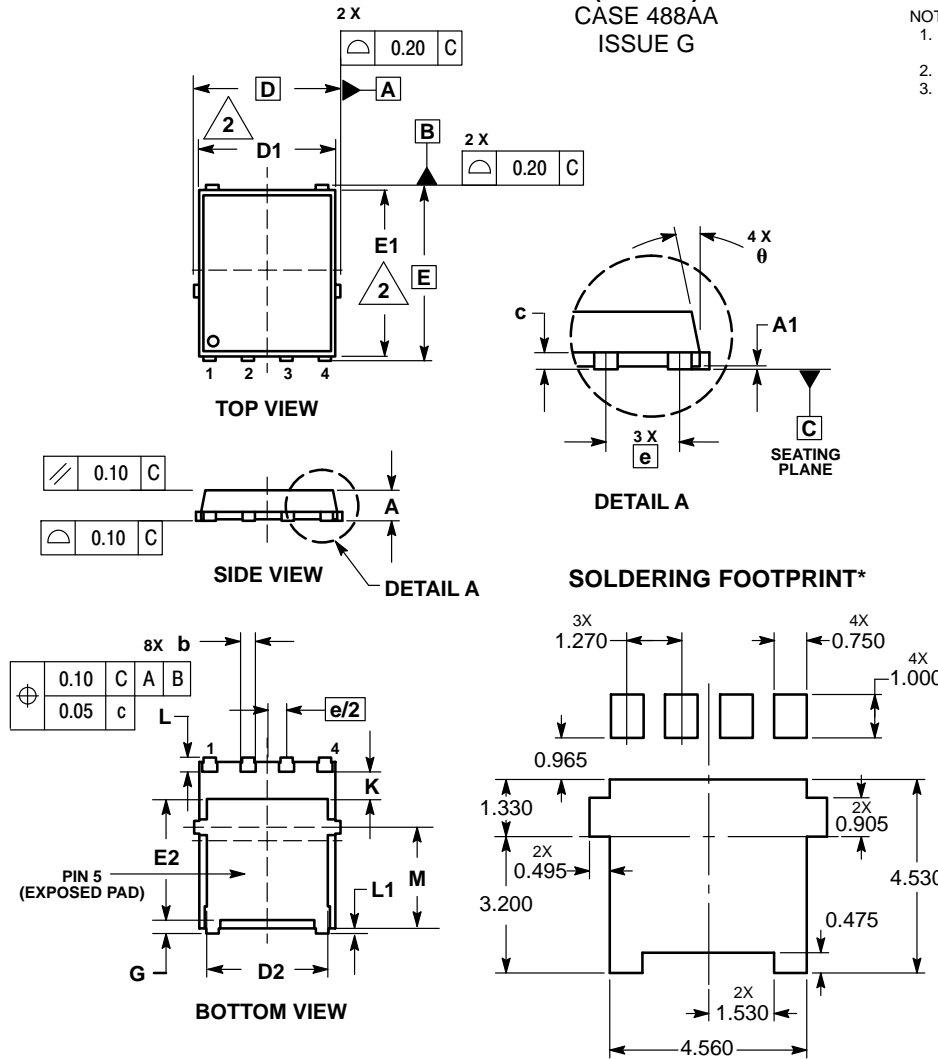
# NTMFS4933N

## PACKAGE DIMENSIONS

DFN5 5x6, 1.27P  
(SO-8FL)  
CASE 488AA  
ISSUE G

NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION D1 AND E1 DO NOT INCLUDE MOLD FLASH PROTRUSIONS OR GATE BURRS.



STYLE 1:  
PIN 1. SOURCE  
2. SOURCE  
3. SOURCE  
4. GATE  
5. DRAIN

\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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