LTC4232: 5A Integrated Hot Swap Controller

DESCRIPTION

Demonstration circuit 1886A features the LTC4232 5A Integrated Hot Swap™ Controller. The LTC4232 is ideally suited for demanding power distribution control in 2.9V to 15V applications for hot board insertion protection, high side power switching, and electronic circuit breaker functions. The LTC4232 provides a rich set of features to support Hot Swap applications including:

- 2% accurate undervoltage and overvoltage protection
- Overtemperature protection
- Adjustable inrush current control
- Adjustable, 10% accurate current limit with programmable cutout time
- Programmable output voltage ramp rate
- Configurable for auto-retry or latchoff on overcurrent faults
- Power good and fault outputs

Available in a 16-lead 5mm × 3mm DFN package, the LTC4232 is showcased on demonstration circuit 1886A, configured for a 12V application. By changing a few passive components, 2.9V to 15V applications can easily be evaluated.

Design files for this circuit board are available at http://www.linear.com/demo

PERFORMANCE SUMMARY (T_A = 25°C)

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
V_{DD}	Input Supply Range		2.9		15	V
dVGATE/dt	GATE Pin Turn-On Ramp Rate		0.15	0.3	0.55	V/ms
R_{ON}	MOSFET + Sense Resistor On-Resistance		15	33	50	mΩ
$I_{LIM(TH)}$	Current Limit Threshold	V_{FB} = 1.23V	5.0	5.6	6.1	A
$I_{LIM(TH)}$	Current Limit Threshold	V_{FB} = 0V V_{FB} = 1.23V, R_{SET} = 20k	1.2 2.6	1.5 2.9	1.8 3.3	A A
V_{TH}	OV, UV, FB Pin Threshold Voltage	V_{IN} Rising	1.21	1.235	1.26	V
$V_{UV(RTH)}$	UV Pin Reset Threshold Voltage	V_{UV} Falling	0.55	0.62	0.7	V
$V_{FB(HYST)}$	FB Pin Power Good Hysteresis		10	20	30	mV
$V_{TIMER(H)}$	TIMER Pin High Threshold	V_{TIMER} Rising	1.2	1.235	1.28	V
$V_{TIMER(L)}$	TIMER Pin Low Threshold	V_{TIMER} Falling	0.1	0.21	0.3	V
$I_{TIMER(UP)}$	TIMER Pin Pull-Up Current	V_{TIMER} = 0	–80	–100	–120	µA
$I_{TIMER(DN)}$	TIMER Pin Pulldown Current	V_{TIMER} = 1.2V	1.4	2	2.6	µA
$I_{GATE(UP)}$	Gate Pull-Up Current	Gate Drive On, V_{GATE} = V_{OUT} = 12V	–18	–14	–29	µA
$t_{D(AUTO-RET)}$	Auto-Retry Turn-On Delay		50	100	150	ms

QUICK START PROCEDURE

Demonstration circuit 1886A is easy to set up to evaluate the performance of the LTC4232. Refer to Figure 1 for proper measurement equipment setup and follow the procedure below.

Demonstration Circuit 1886A has two user configurable jumper options:

- JP1 TIMER DURATION: Set to 2ms for the internal 2ms timer or 12ms determined by C1. C1 may be replaced for other timer durations. (Default position: 12ms)
- JP2 AUTORETRY: Set to ON for auto-retry or OFF for latchoff on overcurrent faults. (Default position: OFF)

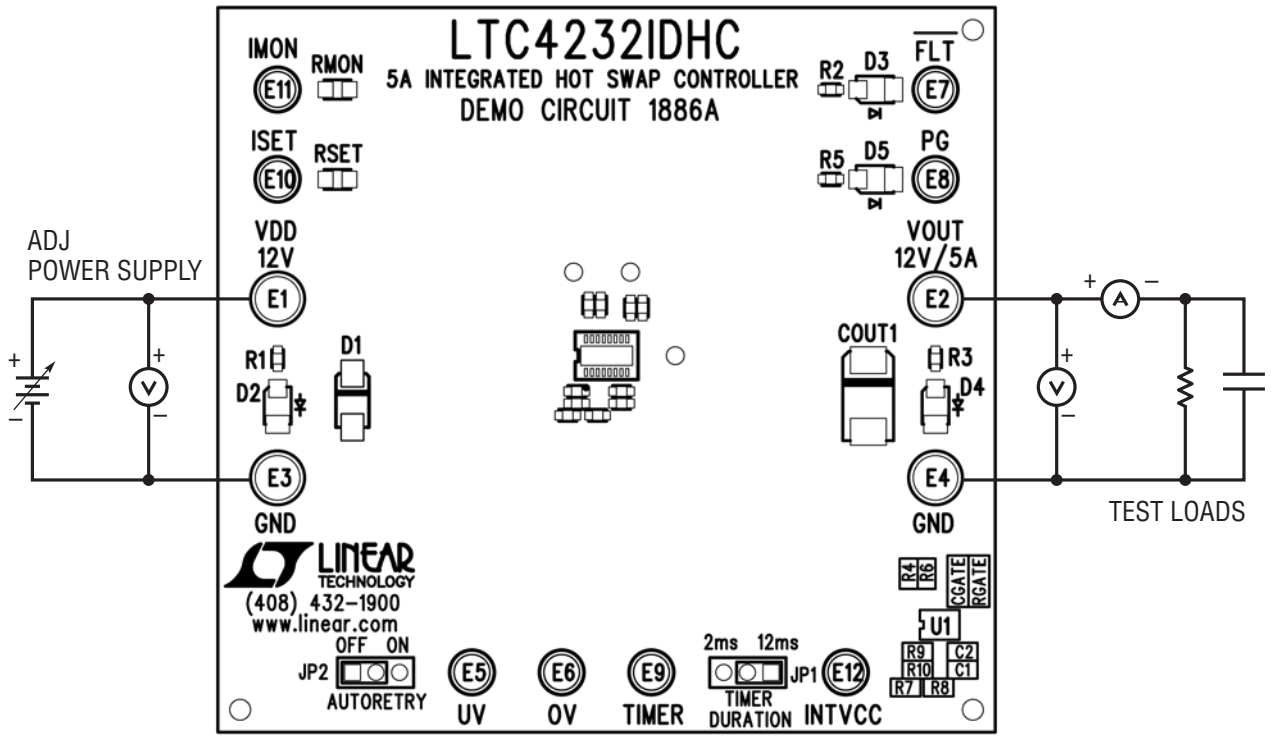


Figure 1. Proper Measurement Equipment Setup

QUICK START PROCEDURE

LEDs indicate the state of input power, output power, $\overline{FAULT}$ and PG. Load current can be monitored on the I_{MON} turret, which has a gain of 0.4V/A determined by R_{MON} (20k).

Set an adjustable power supply capable of supplying 10A to 12V. Turn off power and connect the supply to the V_{DD} and GND turrets.

Connect a suitable load to the V_{OUT} and GND turrets. This load can be an electronic load or power resistors capable of dissipating 100W.

NOTE: Because the LTC4232 incorporates foldback current limiting, the nominal start-up current supplied to the load is 1.5A and can be as low as 1.2A. This current limit increases linearly until the FB pin exceeds 0.6V (V_{OUT} > 5.1V). An electronic constant current load set to 1.5A will not permit the circuit to turn on unless it is gated on by the PG signal (as would be the case with a DC/DC converter controlled by the PG signal). Resistive loading will not have this problem.

Turn on the power supply, verify the input voltage is 12V. Verify the output voltage and the load current, D2 and D4 should both be lit (input voltage and output voltage, respectively) and both D3 ($\overline{FLT}$) and D5 (PG) should be off. On power-up, observe the slope of V_{OUT}. This should be in the range of 0.15 to 0.55V/ms, corresponding to a ramp-up time of 22ms to 80ms to 12V. With the circuit functioning, additional evaluations can now be performed.

OV/UV/PG thresholds: Set the input supply to zero and ramp the voltage slowly, observing the following events. Above 10.3V, the circuit will be out of UV lockout and the output should ramp-up, lighting D4. Above 10.9V the FB pin will be past its threshold, asserting the PG pin high and extinguishing D5. Increasing the supply past 15.8V will engage OV lockout; D4 will extinguish and D5 will light. Note that the voltages indicated in this step are maximums, taking into consideration the tolerances of the resistors and the LTC4232 inputs.

Current Limit Thresholds: With the input supply set to 12V, load the output with a 2.5Ω power resistor capable of dissipating 60W. Power should remain on, as the current will be below the 5.0A minimum current limit threshold. Next, load the output with a 1.8Ω power resistor. Power should be interrupted, as the current will be above the 6.1A maximum current limit threshold.

QUICK START PROCEDURE

Inrush into capacitive load: One of the main functions of a hot swap circuit is to provide controlled ramp-up into a capacitive load to avoid disturbing the input power supply. For the following tests, ensure that the AUTORETRY jumper is set to OFF and the TIMER DURATION jumper is set to 12ms. To guarantee that current limit is never reached during ramp-up into a capacitor, the current must be less than the minimum current limit threshold of 1.2A when the gate ramp rate is at its maximum value of 0.55V/ms. (Note that the minimum current limit threshold occurs when the FB pin is at zero.)

C = I/(dV/dt) = 1.2A/(0.55V/ms) = 2182µF

Thus, the circuit will always power up successfully with a 2000µF capacitor at V_{OUT}, and observation of the TIMER turret post will show that it never begins to ramp. Figure 2 shows successful ramp-up into a 1200µF capacitor. Inrush current is determined by ramp rate alone.

It is more complicated to find the smallest capacitor that is guaranteed to prevent successful ramp-up, since the current into the load capacitor is a function of the scaled output voltage at the FB pin. As a starting point, the minimum ramp rate of 0.15V/ms should produce a current greater than the maximum current limit threshold of 1.8A (when FB is at zero) to ensure that the timer begins to ramp as soon as the output begins to rise.

C = I/(dV/dt) = 1.8A/(0.15V/ms) = 12000µF

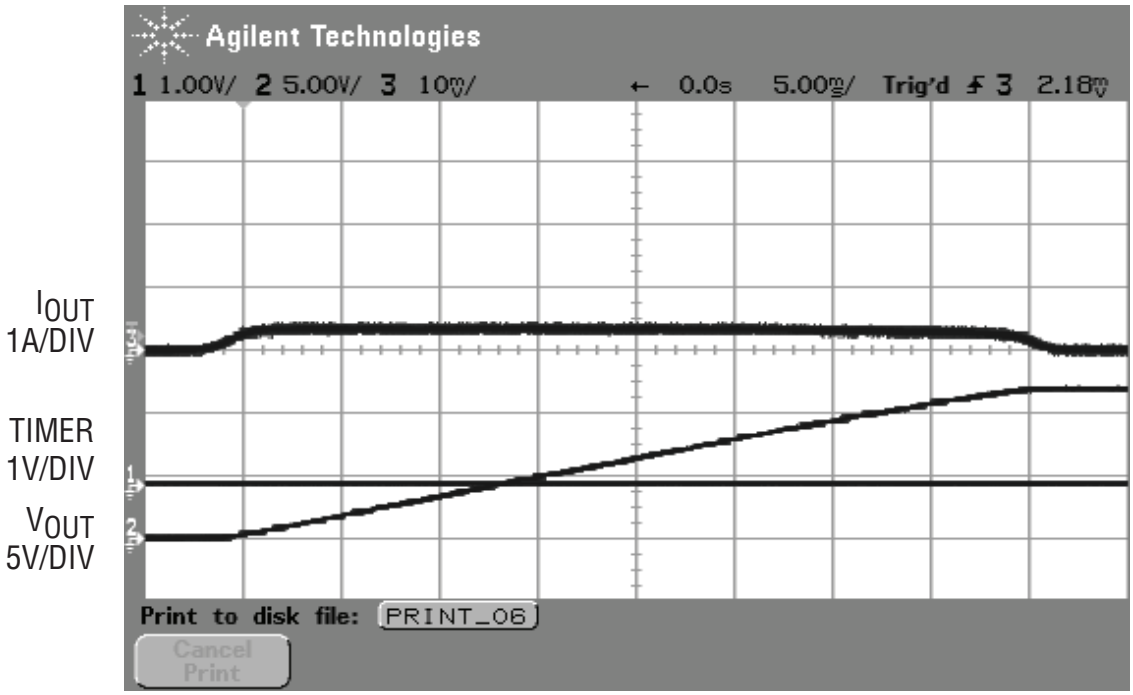


Figure 2. Successful Ramp-Up into 1200µF

QUICK START PROCEDURE

Observation of the TIMER pin will show that it begins to ramp as soon as the output begins to ramp. At this ramp rate, the output voltage will only be at 1.8V after 12ms, and hence the FB pin will be at 0.21V, above the point at which the current limit threshold begins to increase. If the ramp-up becomes limited by the slew rate of the gate pin, the output voltage will continue to rise and successfully power up. However, if the ramp-up continues to be limited by the current limit threshold, the timer will expire. Figure 3 shows unsuccessful ramp-up into an 8000µF capacitor. Current reaches the initial limit when FB is at zero. Once FB rises above approximately 100mV the current (and hence the output ramp rate) increases, however the timer expires before the output reaches its final value.

The correct way to ensure successful power-up into an output capacitance greater than 2000µF is to reduce the ramp rate by installing a 1k resistor and a suitable capacitor for R_{GATE} and C_{GATE} following the procedure in the data sheet. Increasing the timer duration carries the risk of exceeding the Safe Operating Area (SOA) of the internal MOSFET.

Circuit Testing Notes: As in all high current testing, it is a good idea to use twisted pair power leads to minimize circuit inductance. Under step loads significant voltage spikes can occur as a result of this inductance causing false overvoltage or undervoltage trips. If there is significant lead length between the power supply and the DC1886A, add additional bulk capacitance across the V_{IN} and GND turrets. This capacitance may also be needed if stepping the load results in significant voltage steps on the input, particularly if performing tests of the circuit breaker function.

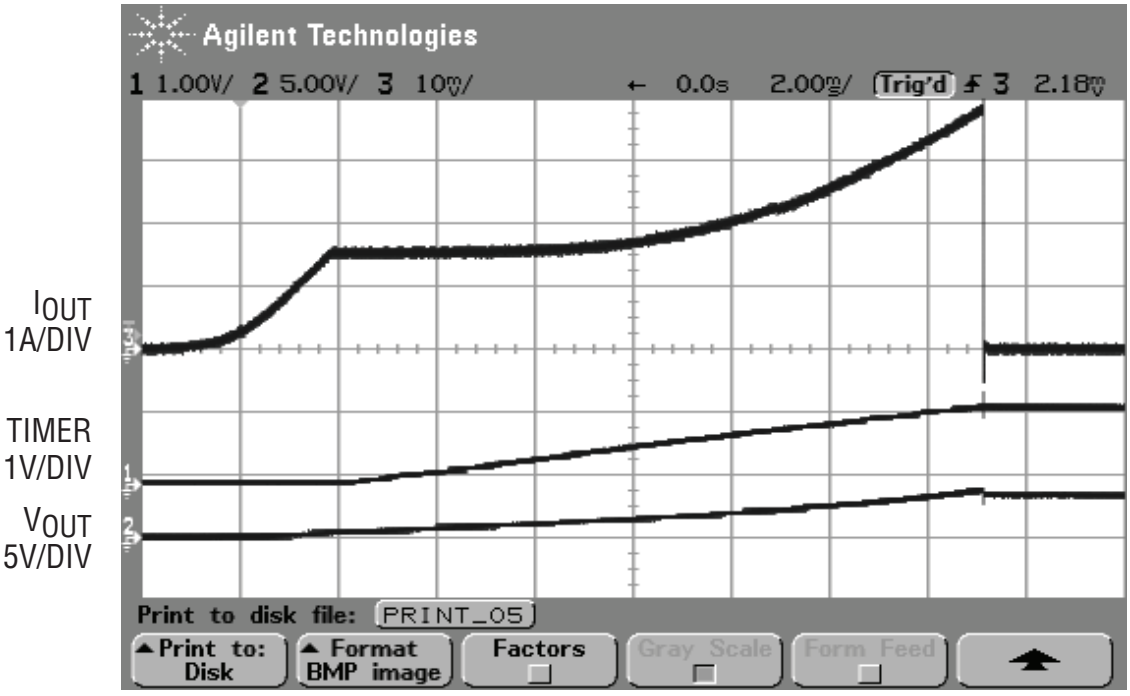
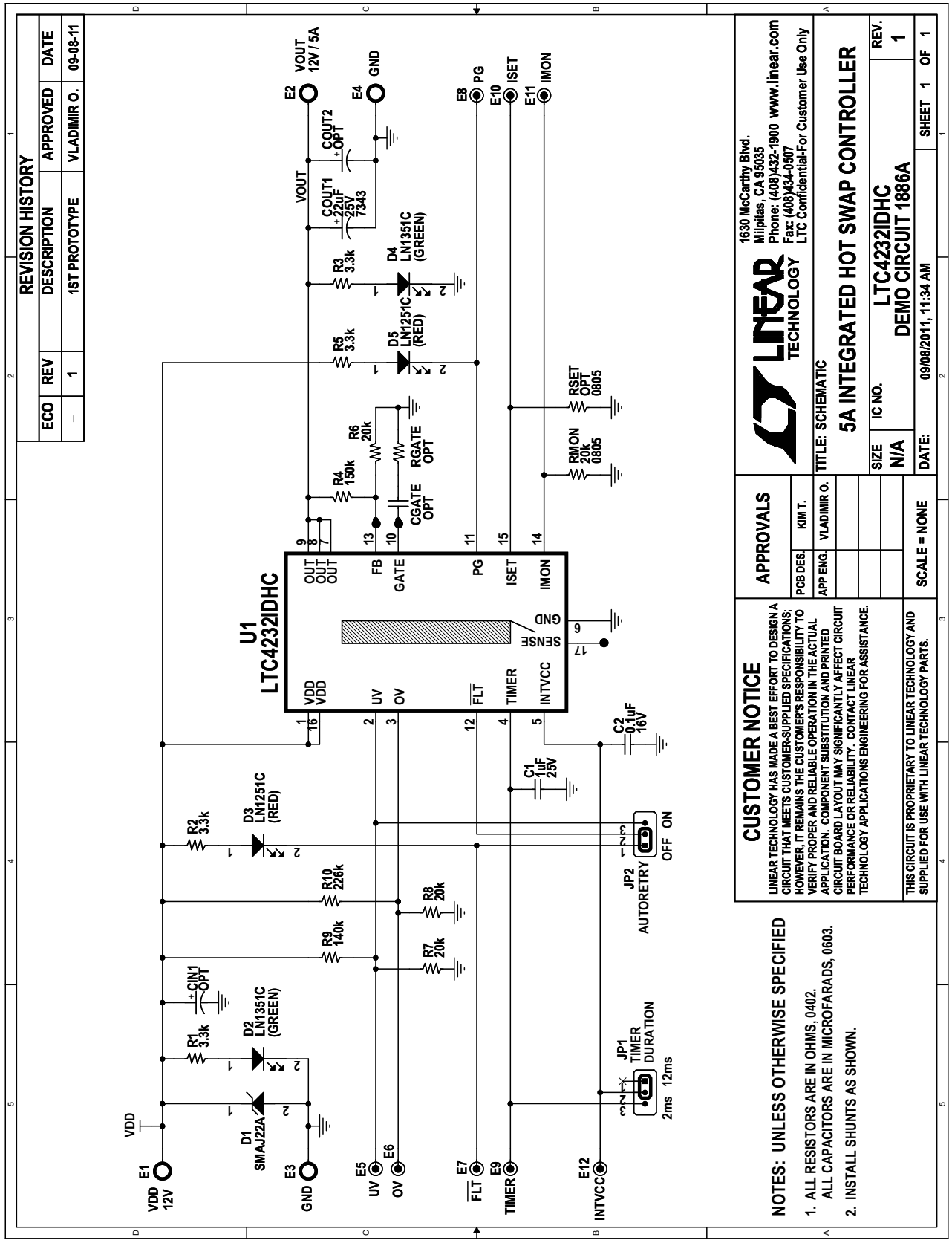


Figure 3. Unsuccessful Ramp-Up into 8000µF

SCHEMATIC DIAGRAM



PARTS LIST

ITEM	QTY	REFERENCE	PART DESCRIPTION	MANUFACTURER/PART NUMBER
1	0	RGATE, CGATE	CAP., 0603	OPT
2	0	CIN1, COUT2	CAP., SANYO\16X25\H	OPT
3	1	COUT1	CAP., TANT, 22µF 25V, 20%, 7343	AVX, TPSD226M025R0200
4	1	C1	CAP., X5R, 1µF 25V, 0603	AVX, 06033D105KAT2A
5	1	C2	CAP., X5R, 0.1µF 25V, 0603	AVX, 06033C104KAT2A
6	1	D1	DIODE, 400W TRANSIENT VOLTAGE SUPPRESSOR, SMA-DIODE	DIODES INC., SMAJ22A
7	2	D2, D4	LED, SMT, GREEN	PANASONIC, LN1351C-(TR)
8	2	D3, D5	LED, SMT, RED	PANASONIC, LN1251C-(TR)
9	4	E1, E2, E3, E4	TURRET, TEST PIN, .094"	MILL-MAX, 2501-2-00-80-00-00-07-0
10	8	E5-E12	TURRET, TEST PIN, .064"	MILL-MAX, 2308-2-00-80-00-00-07-0
11	2	JP1, JP2	JMP, HD1X3, .079CC	SAMTEC, TMM-103-02-L-S
12	1	RMON	RES., CHIP, 20K, 1/16W, 5%, 0805	YAGEO, RC0805JR-0720KL
13	0	RSET	RES., CHIP, 0805	OPT
14	4	R1, R2, R3, R5	RES., CHIP, 3.3K, 1/16W, 5%, 0603	YAGEO, RC0603JR-073K3L
15	1	R4	RES., CHIP, 150K, 1/16W, 5%, 0603	YAGEO, RC0603JR-07150KL
16	3	R6, R7, R8	RES., CHIP, 20K, 1/16W, 5%, 0603	YAGEO, RC0603JR-0720KL
17	1	R9	RES., CHIP, 140K, 1/16W, 5%, 0603	YAGEO, RC0603JR-07140KL
18	1	R10	RES., CHIP, 226K, 1/16W, 5%, 0603	YAGEO, RC0603JR-07226KL
19	1	U1	I.C., LTC4232IDHC, DFN16DHC	LINEAR TECH., LTC4232IDHC
20	1	SHUNT, 0.079" CENTER	SAMTEC, 2SN-BK-G	325

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This notice contains important safety information about temperatures and voltages. For further safety concerns, please contact a LTC application engineer.

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