FAIRCHILD SEMICONDUCTOR™

October 1987
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MM74C165
Parallel-Load 8-Bit Shift Register

General Description

The MM74C165 functions as an 8-bit parallel-load, serial shift register. Data is loaded into the register independent of the state of the clock(s) when PARALLEL LOAD ($\overline{PL}$) is low. Shifting is inhibited as long as $\overline{PL}$ is low. Data is sequentially shifted from complementary outputs, Q_7 and $\overline{Q_7}$, highest-order bit (P7) first. New serial data may be entered via the SERIAL DATA (Ds) input. Serial shifting occurs on the rising edge of CLOCK1 or CLOCK2. Clock inputs may be used separately or together for combined clocking from independent sources. Either clock input may be used also as an active-low clock enable. To prevent double-clocking when a clock input is used as an enable, the enable must be changed to a high level (disabled) only while the clock is HIGH.

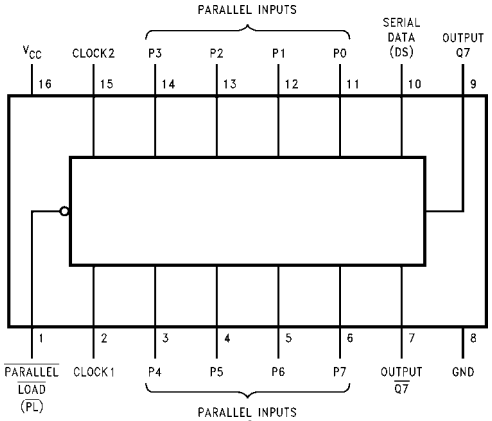
Features

- Wide supply voltage range: 3V to 15V
- Guaranteed noise margin: 1V
- High noise immunity: 0.45 V_{CC} (typ.)
- Low power TTL compatibility: fan out of 2 driving 74L
- Parallel loading independent of clock
- Dual clock inputs
- Fully static operation

Ordering Code:

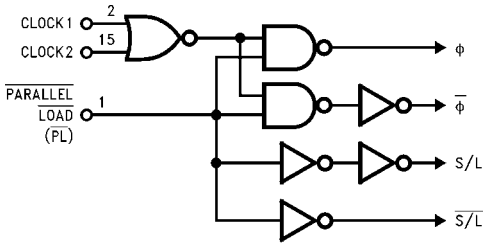
Order Number	Package Number	Package Description
MM74165N	N16E	16-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide

Connection Diagram

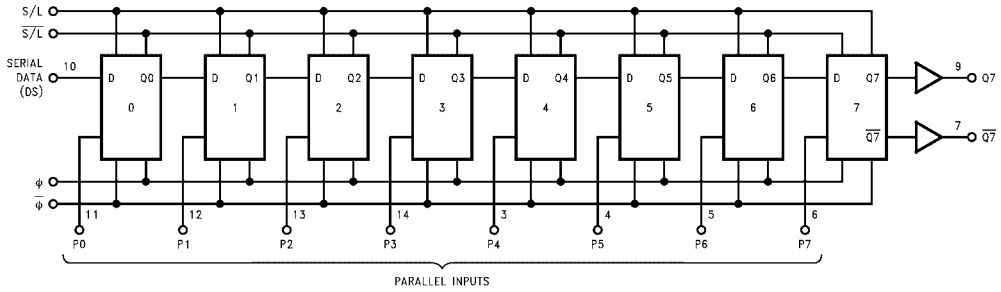


Top View

Block Diagrams



*Please look into Section 8, Appendix D for availability of various package types.



Truth Table

State	Inputs					Internal		Outputs	
	$\overline{PL}$	Clock1	Clock2 (as enable)	Ds	P0 thru P7	Q0	Q1	Q7	$\overline{Q7}$
Parallel Load	L	X	X	X	P0…P7	P0	P1	P7	$\overline{P7}$
Enable	H	L	L	X	X	P0	P1	P7	$\overline{P7}$
Shift (with Ds)	H	↑	L	H	X	H	P0	P6	$\overline{P6}$
Shift (with Ds)	H	↑	L	L	X	L	H	P5	$\overline{P5}$
Hold (Disable)	H	↑	H	X	X	L	H	P5	$\overline{P5}$

X = Don't Care
H = $V_{IN(1)}$
L = $V_{IN(0)}$
↑ = Clock transition from $V_{IN(0)}$ to $V_{IN(1)}$
P0 thru P7 = Data present (and loaded into) parallel inputs
Q0 thru Q6 = Internal flip-flop outputs

Absolute Maximum Ratings(Note 1)

Voltage at Any Pin	−0.3V to V_{CC} + 0.3V
Operating Temperature Range	−55°C to +125°C
Storage Temperature Range	−65°C to +150°C
Absolute Maximum V_{CC}	18V
Power Dissipation	
Dual-In-Line	700 mW
Small Outline	500 mW
Operating V_{CC} Range	3V to 15V
Lead Temperature	
(Soldering, 10 seconds)	260°C

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The Electrical Characteristics table provides conditions for actual device operation.

DC Electrical Characteristics

Min/Max limits apply across temperature range unless otherwise noted

Symbol	Parameter	Conditions	Min	Typ	Max	Units
CMOS TO CMOS						
$V_{IN(1)}$	Logical "1" Input Voltage	V_{CC} = 5V	3.5			V
		V_{CC} = 10V	8.0			
$V_{IN(0)}$	Logical "0" Input Voltage	V_{CC} = 5V			1.5	V
		V_{CC} = 10V			2.0	
$V_{OUT(1)}$	Logical "1" Output Voltage	V_{CC} = 5V, I_O = −10 μA	4.5			V
		V_{CC} = 10V, I_O = −10 μA	9.0			
$V_{OUT(0)}$	Logical "0" Output Voltage	V_{CC} = 5V, I_O = +10 μA			0.5	V
		V_{CC} = 10V, I_O = +10 μA			1.0	
$I_{IN(1)}$	Logical "1" Input Current	V_{CC} = 15V, V_{IN} = 15V		0.005	1.0	μA
$I_{IN(0)}$	Logical "0" Input Current	V_{CC} = 15V, V_{IN} = 0V	−1.0	−0.005		μA
I_{CC}	Supply Current	V_{CC} = 15V		0.05	300	μA
CMOS TO LPTTL INTERFACE						
$V_{IN(1)}$	Logical "1" Input Voltage	V_{CC} = 4.75V	V_{CC} − 1.5			V
$V_{IN(0)}$	Logical "0" Input Voltage	V_{CC} = 4.75V			0.8	V
$V_{OUT(1)}$	Logical "1" Output Voltage	V_{CC} = 4.75V, I_O = −360 μA	2.4			V
$V_{OUT(0)}$	Logical "0" Output Voltage	V_{CC} = 4.75V, I_O = 360 μA			0.4	V
OUTPUT DRIVE (See Family Characteristics Data Sheet) (short circuit current)						
I_{SOURCE}	Output Source Current	V_{CC} = 5V	−1.75	−3.3		mA
	(P-Channel)	T_A = 25°C, V_{OUT} = 0V				
I_{SOURCE}	Output Source Current	V_{CC} = 10V	−8.0	−15		mA
	(P-Channel)	T_A = 25°C, V_{OUT} = 0V				
I_{SINK}	Output Sink Current	V_{CC} = 5V	1.75	3.6		mA
	(N-Channel)	T_A = 25°C, V_{OUT} = V_{CC}				
I_{SINK}	Output Sink Current	V_{CC} = 10V	8.0	16		mA
	(N-Channel)	T_A = 25°C, V_{OUT} = V_{CC}				

AC Electrical Characteristics (Note 2)

$T_A = 25°C$, $C_L = 50$ pF, unless otherwise noted

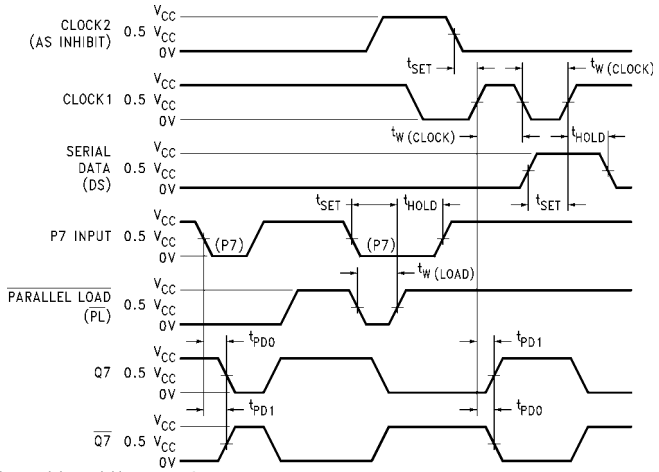
Symbol	Parameter	Conditions	Min	Typ	Max	Units
t_{pd0}, t_{pd1}	Propagation Delay Time to a Logical "0" or	$V_{CC} = 5V$		200	400	ns
	Logical "1" from Clock or Load to Q or $\overline{Q}$	$V_{CC} = 10V$		80	200	
t_{pd0}, t_{pd1}	Propagation Delay Time to a Logical "0" or	$V_{CC} = 5V$		200	400	ns
	Logical "1" from H to Q or $\overline{Q}$	$V_{CC} = 10V$		80	200	
t_S	Clock Inhibit Set-up Time	$V_{CC} = 5V$	150	75		ns
		$V_{CC} = 10V$	60	30		
t_S	Serial Input Set-up Time	$V_{CC} = 5V$	50	25		ns
		$V_{CC} = 10V$	30	15		
t_H	Serial Input Hold Time	$V_{CC} = 5V$	50	0		ns
		$V_{CC} = 10V$	30	0		
t_S	Parallel Input Set-Up Time	$V_{CC} = 5V$	150	75		ns
		$V_{CC} = 10V$	60	30		
t_H	Parallel Input Hold Time	$V_{CC} = 5V$	50	0		ns
		$V_{CC} = 10V$	30	0		
t_W	Minimum Clock Pulse Width	$V_{CC} = 5V$		70	200	ns
		$V_{CC} = 10V$		30	100	
t_W	Minimum Load Pulse Width	$V_{CC} = 5V$		85	180	ns
		$V_{CC} = 10V$		30	90	
f_{MAX}	Maximum Clock Frequency	$V_{CC} = 5V$	2.5	6		MHz
		$V_{CC} = 10V$	5	12		
t_r, t_f	Maximum Clock Rise and Fall Time	$V_{CC} = 5V$	10			µs
		$V_{CC} = 10V$	5			
C_{IN}	Input Capacitance	(Note 3)		5		pF
C_{PD}	Power Dissipation Capacitance	(Note 4)		65		pF

Note 2: AC Parameters are guaranteed by DC correlated testing.

Note 3: Capacitance is guaranteed by periodic testing.

Note 4: C_{PD} determines the no load AC power consumption of any CMOS device. For complete explanation see Family Characteristics application note AN-90.

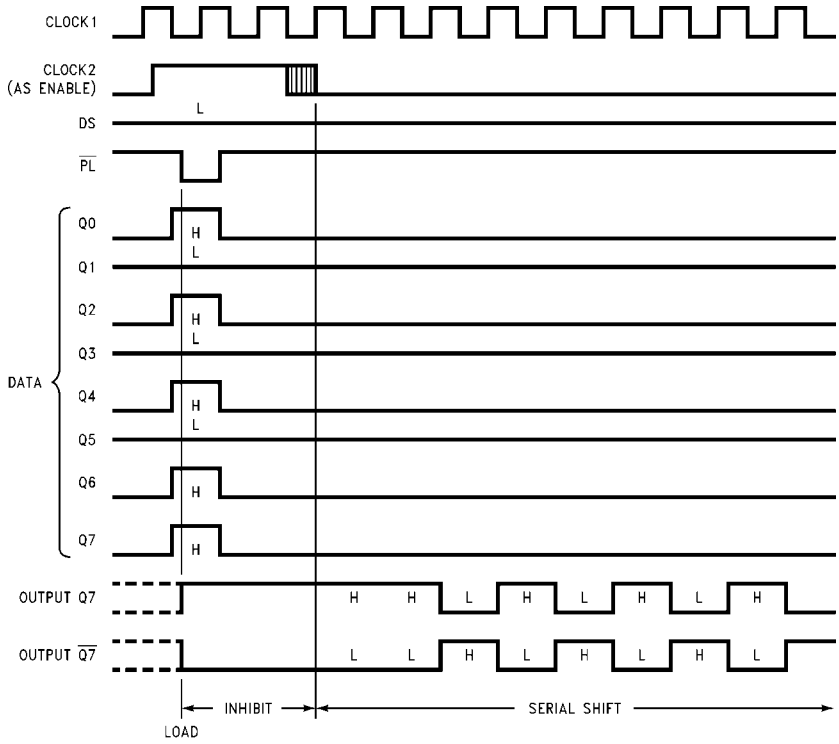
Switching Time Waveform



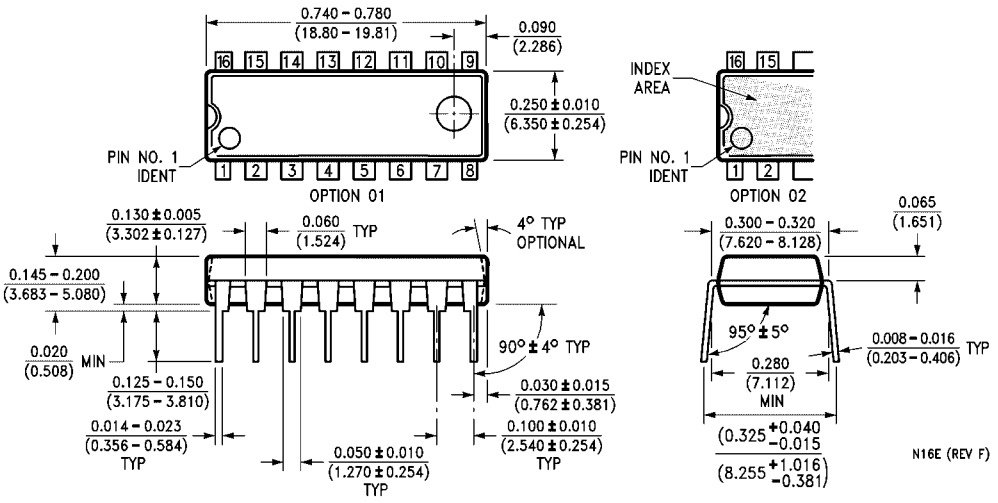
Note A: The remaining six data and the serial input are LOW.

Note B: Prior to test, HIGH level data is loaded into the P7 input.

Logic Waveform



Physical Dimensions inches (millimeters) unless otherwise noted



16-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide
Package Number N16E