

## P-channel -60 V, 23 mΩ typ., -42 A STripFET™ F6 Power MOSFET in a PowerFLAT™ 5x6 package

Datasheet - production data

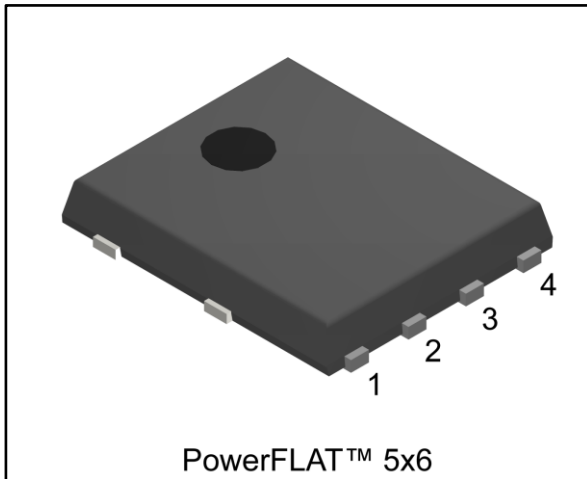
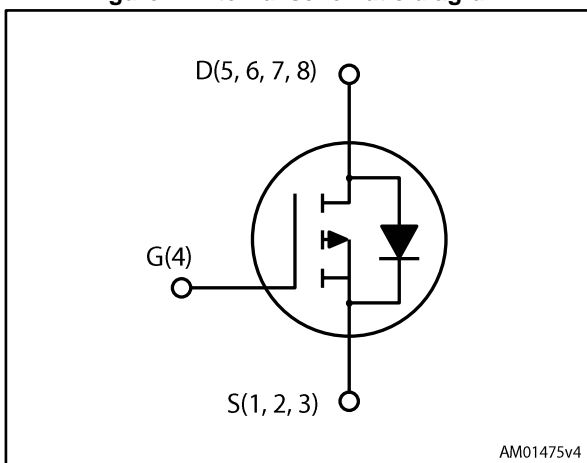


Figure 1: Internal schematic diagram



### Features

Order code	V <sub>DS</sub>	R <sub>DS(on)</sub> max.	I <sub>D</sub>
STL42P6LLF6	-60 V	26 mΩ	-42 A

- Very low on-resistance
- Very low gate charge
- High avalanche ruggedness
- Low gate drive power loss

### Applications

- Switching applications

### Description

This device is a P-channel Power MOSFET developed using the STripFET™ F6 technology, with a new trench gate structure. The resulting Power MOSFET exhibits very low R<sub>DS(on)</sub> in all packages.

Table 1: Device summary

Order code	Marking	Package	Packaging
STL42P6LLF6	42P6LLF6	PowerFLAT™ 5x6	Tape and reel

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# 1 Electrical ratings

Table 2: Absolute maximum ratings

Symbol	Parameter	Value	Unit
$V_{DS}$	Drain-source voltage	-60	V
$V_{GS}$	Gate-source voltage	$\pm 20$	V
$I_D^{(1)}$	Drain current (continuous) at $T_C = 25\text{ }^\circ\text{C}$	-42	A
$I_D^{(1)}$	Drain current (continuous) at $T_C = 100\text{ }^\circ\text{C}$	-30	A
$I_D^{(1)(3)}$	Drain current (pulsed)	-168	A
$I_D^{(2)}$	Drain current (continuous) at $T_{pcb} = 25\text{ }^\circ\text{C}$	-9	A
$I_D^{(2)}$	Drain current (continuous) at $T_{pcb} = 100\text{ }^\circ\text{C}$	-6.6	A
$I_{DM}^{(2)(3)}$	Drain current (pulsed)	-36	A
$P_{TOT}^{(1)}$	Total dissipation at $T_C = 25\text{ }^\circ\text{C}$	100	W
$P_{TOT}^{(2)}$	Total dissipation at $T_{pcb} = 25\text{ }^\circ\text{C}$	4.8	W
$T_{stg}$	Storage temperature range	-55 to 175	$^\circ\text{C}$
$T_j$	Operating junction temperature range		

**Notes:**

- (1)The value is rated by  $R_{thj-case}$ .  
 (2)The value is rated by  $R_{thj-pcb}$ .  
 (3)Pulse width is limited by safe operating area.

Table 3: Thermal data

Symbol	Parameter	Value	Unit
$R_{thj-case}$	Thermal resistance junction-case max	1.5	$^\circ\text{C}/\text{W}$
$R_{thj-pcb}^{(1)}$	Thermal resistance junction-pcb max	31.3	$^\circ\text{C}/\text{W}$

**Notes:**

- (1)When mounted on FR-4 board of 1 inch<sup>2</sup>, 2 Oz Cu,  $t < 10\text{ s}$ .

## 2 Electrical characteristics

( $T_C = 25\text{ °C}$  unless otherwise specified)

**Table 4: Static**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	$V_{GS} = 0\text{ V}$ , $I_D = -250\text{ }\mu\text{A}$	-60			V
$I_{DSS}$	Zero gate voltage Drain current	$V_{GS} = 0\text{ V}$ , $V_{DS} = -60\text{ V}$			-1	$\mu\text{A}$
		$V_{GS} = 0\text{ V}$ , $V_{DS} = -60\text{ V}$ , $T_C = 125\text{ °C}^{(1)}$			-10	$\mu\text{A}$
$I_{GSS}$	Gate-body leakage current	$V_{DS} = 0\text{ V}$ , $V_{GS} = \pm 20\text{ V}$			$\pm 100$	nA
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}$ , $I_D = -250\text{ }\mu\text{A}$	-1		-2.5	V
$R_{DS(on)}$	Static drain-source on-resistance	$V_{GS} = -10\text{ V}$ , $I_D = -4.5\text{ A}$		23	26	m $\Omega$
		$V_{GS} = -4.5\text{ V}$ , $I_D = -4.5\text{ A}$		28	34	

**Notes:**

<sup>(1)</sup>Defined by design, not subject to production testing

**Table 5: Dynamic**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$C_{iss}$	Input capacitance	$V_{DS} = -25\text{ V}$ , $f = 1\text{ MHz}$ , $V_{GS} = 0\text{ V}$	-	3780	-	pF
$C_{oss}$	Output capacitance		-	262	-	pF
$C_{rss}$	Reverse transfer capacitance		-	170	-	pF
$Q_g$	Total gate charge	$V_{DD} = -30\text{ V}$ , $I_D = -9\text{ A}$ , $V_{GS} = -4.5\text{ V}$ (see <a href="#">Figure 14: "Gate charge test circuit"</a> )	-	30	-	nC
$Q_{gs}$	Gate-source charge		-	10.8	-	nC
$Q_{gd}$	Gate-drain charge		-	10.5	-	nC
$R_G$	Gate input resistance	$I_D = 0\text{ A}$ , $f = 1\text{ MHz}$	-	1.7	-	$\Omega$

**Table 6: Switching times**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	$V_{DD} = -30\text{ V}$ , $I_D = -4.5\text{ A}$ , $R_G = 4.7\text{ }\Omega$ , $V_{GS} = -10\text{ V}$ (see <a href="#">Figure 13: "Switching times test circuit for resistive load"</a> )	-	51.4	-	ns
$t_r$	Rise time		-	39	-	ns
$t_{d(off)}$	Turn-off-delay time		-	171	-	ns
$t_f$	Fall time		-	21	-	ns

Table 7: Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$I_{SD}$	Source-drain current		-	-42		A
$I_{SDM}^{(1)}$	Source-drain current (pulsed)		-	-168		A
$V_{SD}^{(2)}$	Forward on voltage	$V_{GS} = 0 \text{ V}$ , $I_{SD} = -9 \text{ A}$	-		-1.1	V
$t_{rr}$	Reverse recovery time	$I_{SD} = -9 \text{ A}$ , $di/dt = 100 \text{ A}/\mu\text{s}$ , $V_{DD} = -4.8 \text{ V}$ , $T_j = 150 \text{ }^\circ\text{C}$ (see <a href="#">Figure 15: "Test circuit for inductive load switching and diode recovery times"</a> )	-	34		ns
$Q_{rr}$	Reverse recovery charge		-	48		nC
$I_{RRM}$	Reverse recovery current		-	-2.8		A

**Notes:**

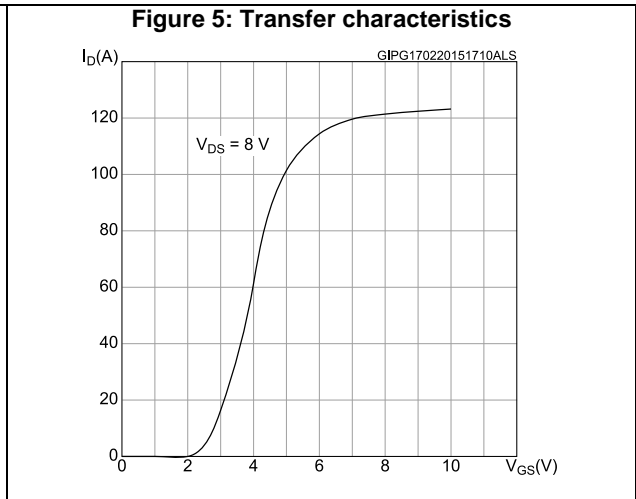
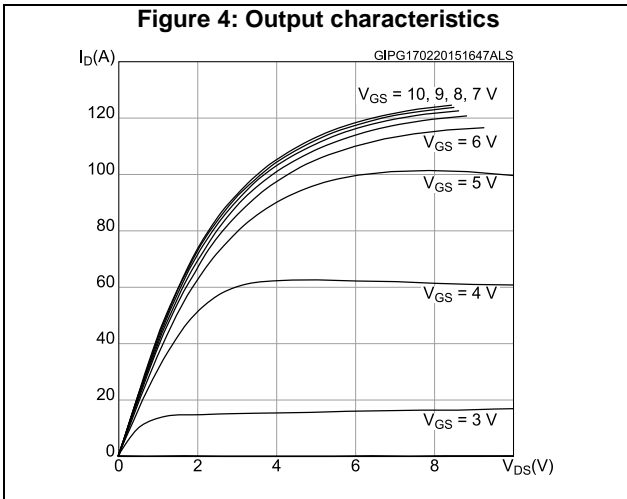
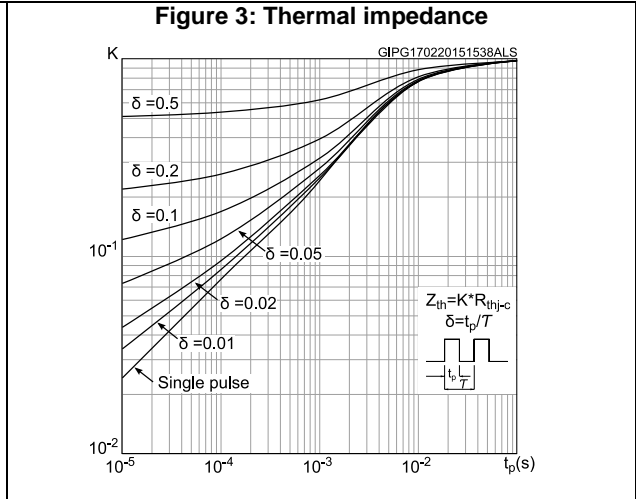
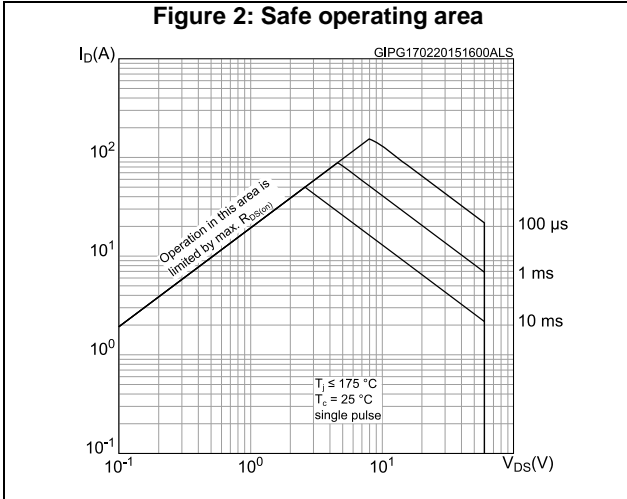
(1) Pulse width limited by safe operating area

(2) Pulse test: pulse duration = 300  $\mu\text{s}$ , duty cycle 1.5%

## 2.1 Electrical characteristics (curves)



For the P-channel Power MOSFET, current polarity of voltages and current have to be reversed.



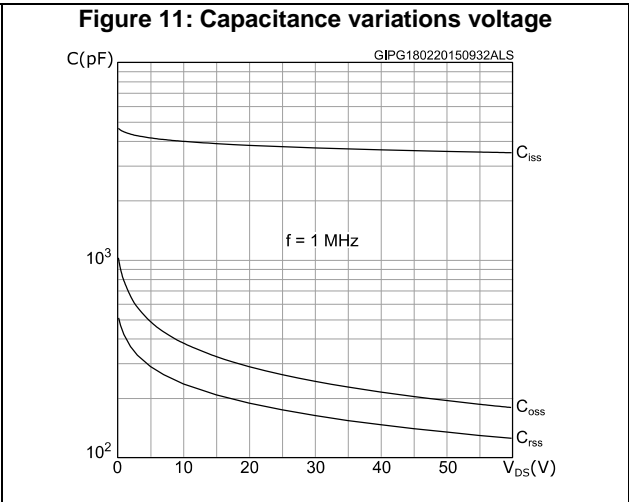
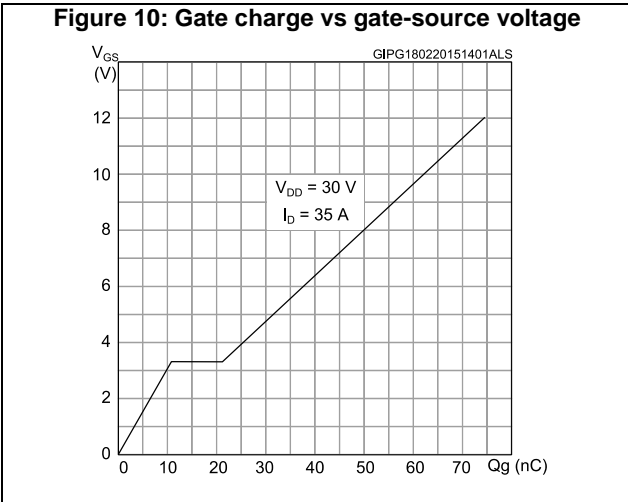
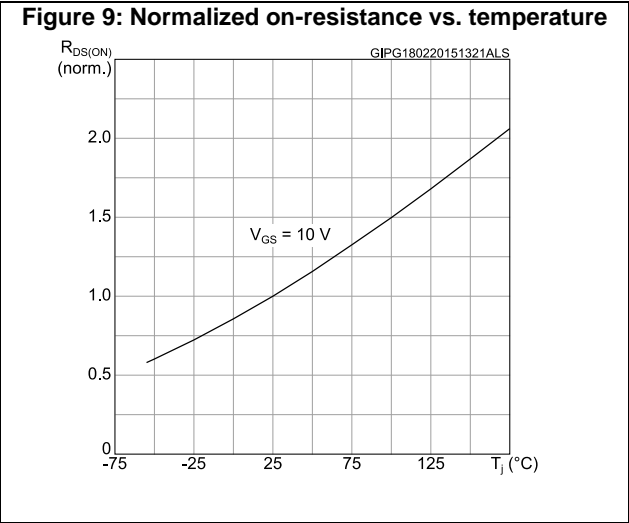
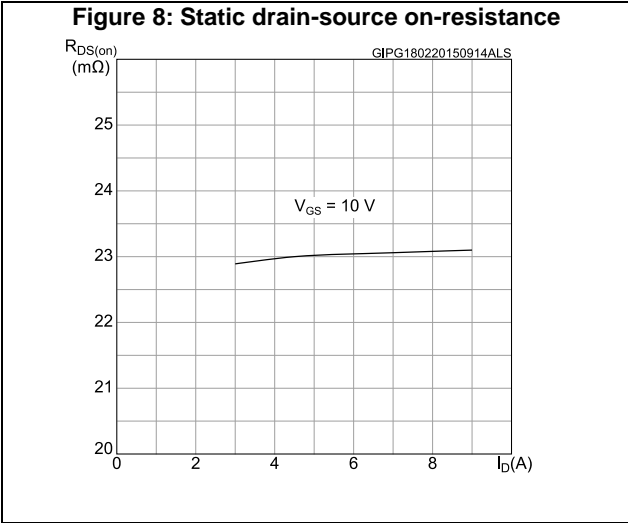
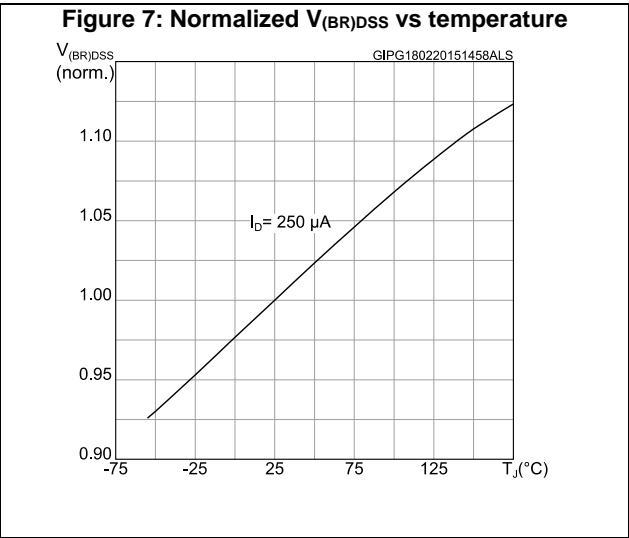
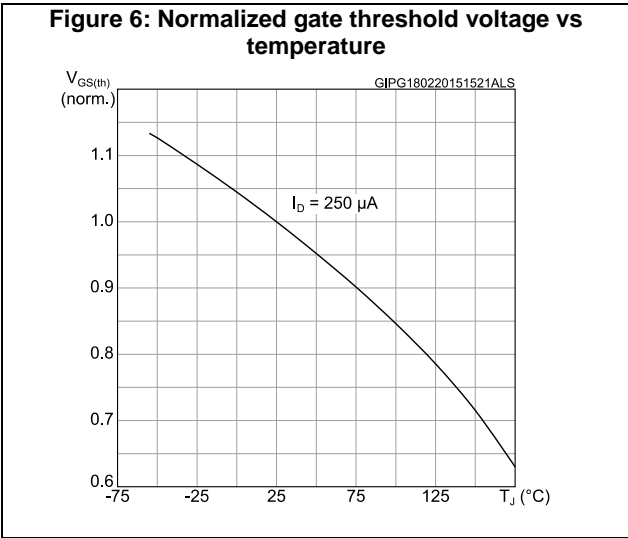
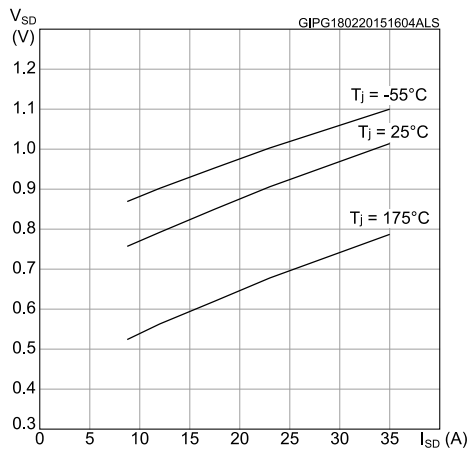


Figure 12: Source-drain diode forward characteristics





### 3 Test circuits

Figure 13: Switching times test circuit for resistive load

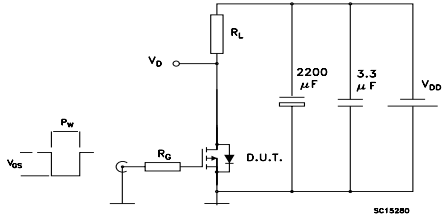


Figure 14: Gate charge test circuit

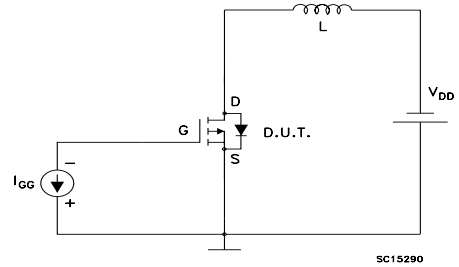
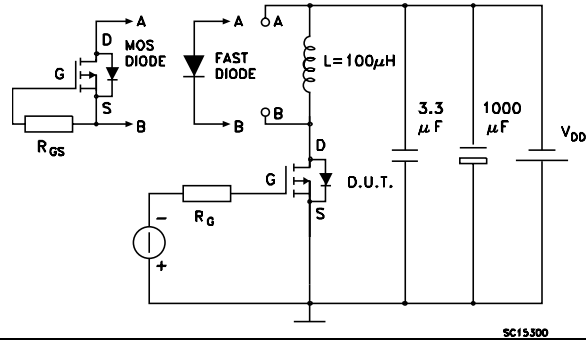


Figure 15: Test circuit for inductive load switching and diode recovery times

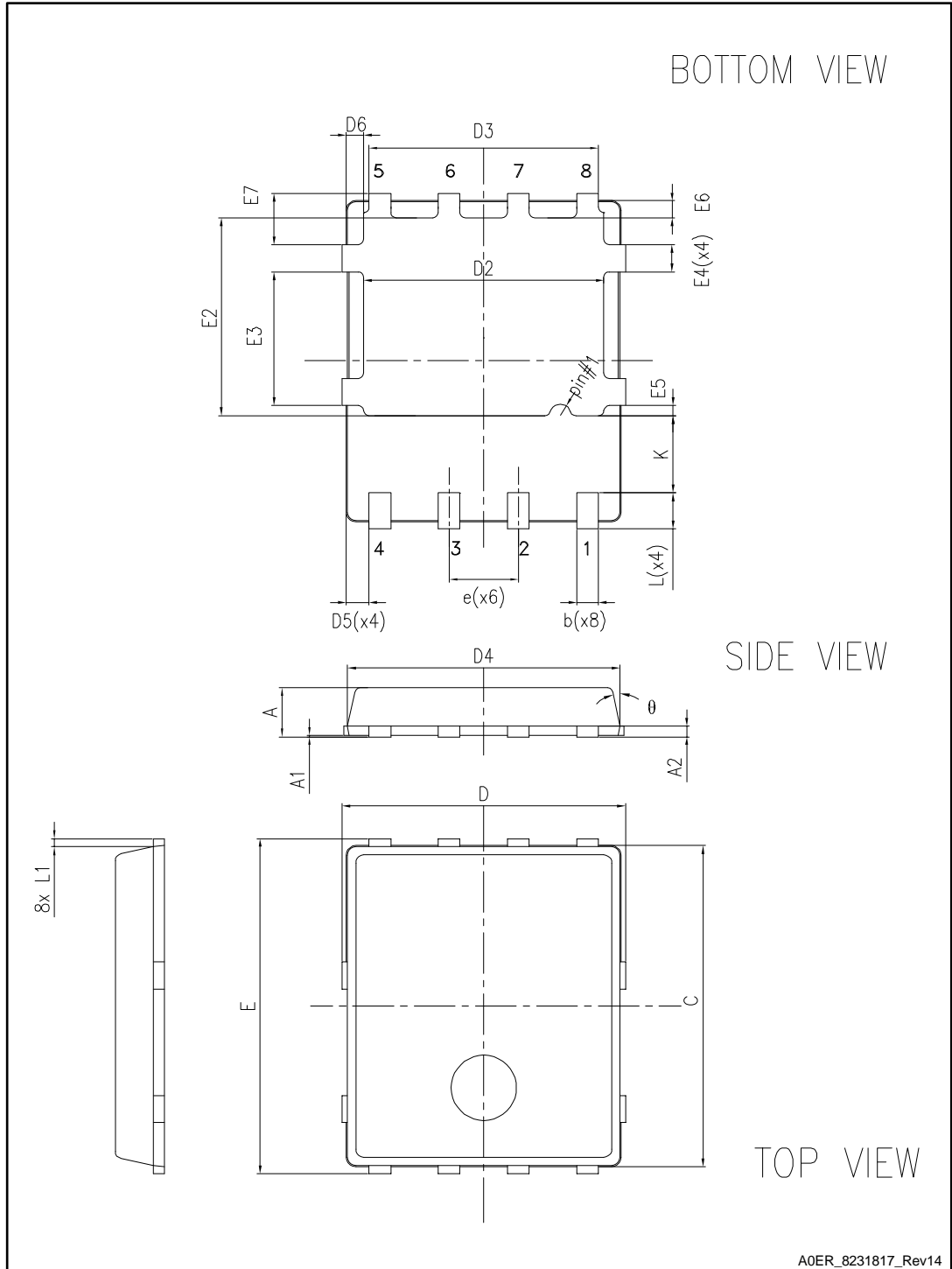


## 4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: [www.st.com](http://www.st.com). ECOPACK® is an ST trademark.

### 4.1 PowerFLAT™ 5x6 type R package information

Figure 16: PowerFLAT™ 5x6 type R package outline

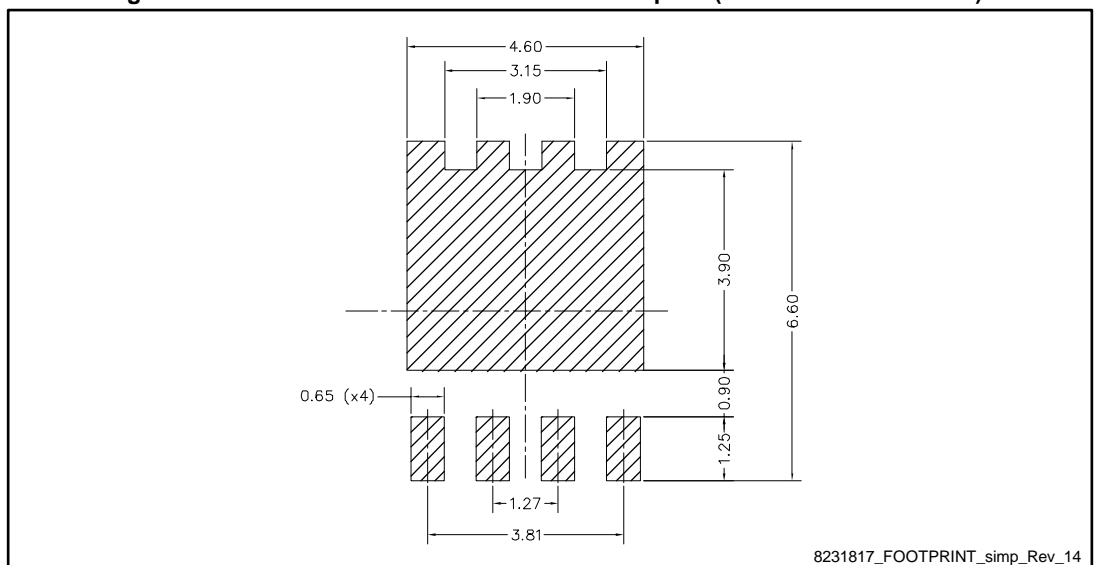


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Table 8: PowerFLAT™ 5x6 type R mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	0.80		1.00
A1	0.02		0.05
A2		0.25	
b	0.30		0.50
C	5.80	6.00	6.20
D	5.00	5.20	5.40
D2	4.15		4.45
D3	4.05	4.20	4.35
D4	4.80	5.00	5.20
D5	0.25	0.40	0.55
D6	0.15	0.30	0.45
e		1.27	
E	5.95	6.15	6.35
E2	3.50		3.70
E3	2.35		2.55
E4	0.40		0.60
E5	0.08		0.28
E6	0.20	0.325	0.45
E7	0.75	0.90	1.05
K	1.275		1.575
L	0.60		0.80
L1	0.05	0.15	0.25
θ	0°		12°

Figure 17: PowerFLAT™ 5x6 recommended footprint (dimensions are in mm)



## 4.2 PowerFLAT™ 5x6 packing information

Figure 18: PowerFLAT™ 5x6 tape (dimensions are in mm)

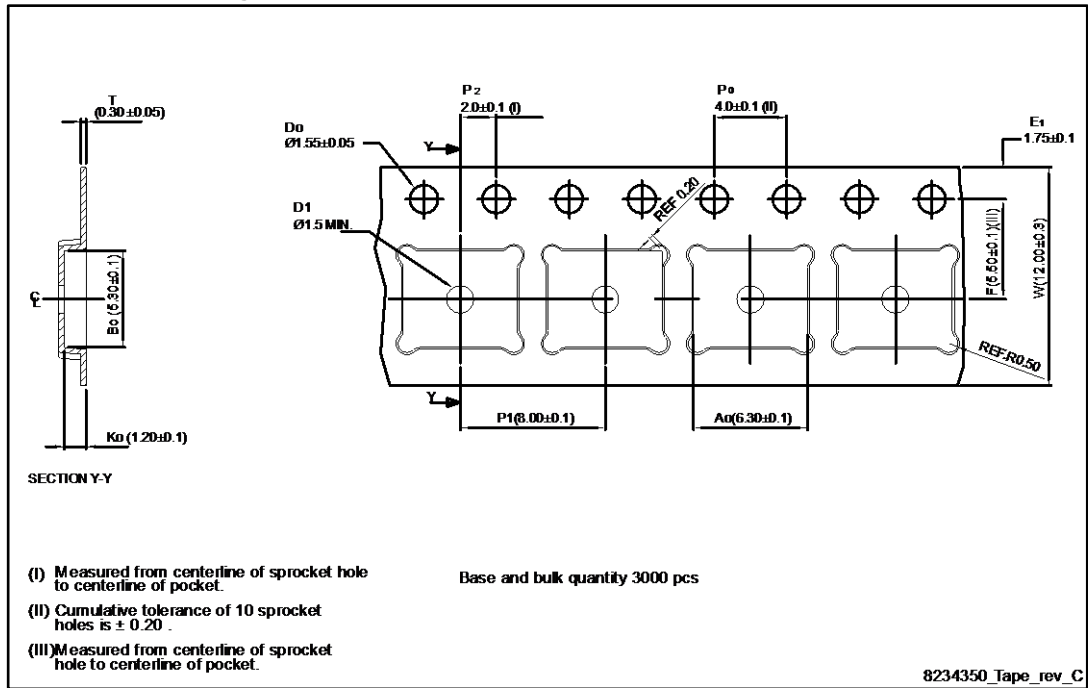


Figure 19: PowerFLAT™ 5x6 package orientation in carrier tape

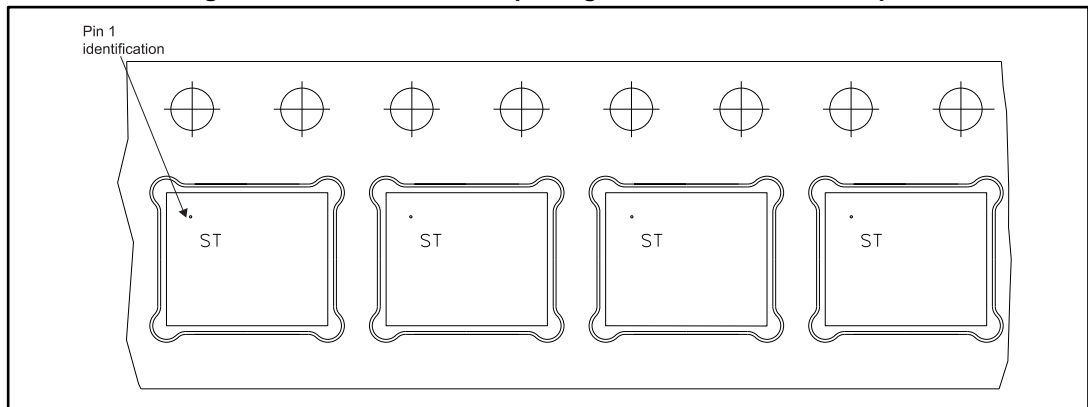
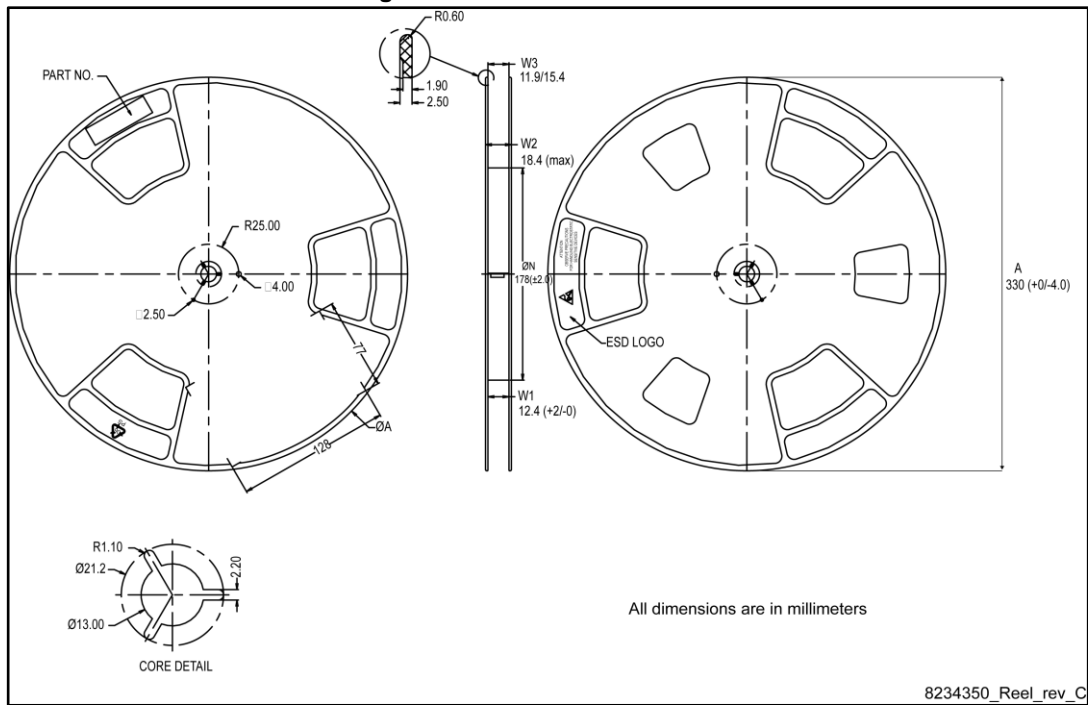


Figure 20: PowerFLAT™ 5x6 reel



## 5 Revision history

**Table 9: Document revision history**

Date	Revision	Changes
28-Oct-2013	1	First release.
25-Aug-2014	2	Modified: <i>Figure 1: "Internal schematic diagram"</i> Updated: <i>Section 10: "Package mechanical data"</i> Minor text changes
24-Feb-2015	3	In title description on cover page, changed 0.02 $\Omega$ to 0.023 $\Omega$ In features table on cover page, changed 0.028 $\Omega$ to 0.026 $\Omega$ Updated <i>Table 2: Absolute maximum ratings</i> Updated <i>Table 4: Static</i> – renamed table and updated Static drain-source on-resistance values Updated <i>Table 5: Dynamic</i> – test conditions and all typical values Updated <i>Table 6: Switching times</i> – test conditions and all typical values Updated <i>Table 7: Source-drain diode</i> – test conditions and all typical values Added <i>Section 2.2: Electrical characteristics (curves)</i> Updated <i>Section 4: Package mechanical data</i> Minor text changes
15-Nov-2016	4	Updated title, features table and description on cover page Updated <i>Table 2: "Absolute maximum ratings"</i> Updated <i>Table 4: "Static", Table 5: "Dynamic", Table 6: "Switching times"</i> and <i>Table 7: "Source drain diode"</i> Updated <i>Figure 9: "Normalized on-resistance vs. temperature"</i> Updated <i>Section 4.1: "PowerFLAT™ 5x6 type R package information"</i> Minor text changes

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