TSA1005

DUAL-CHANNEL, 10-BIT, 20/40MSPS A/D CONVERTER

NOT FOR NEW DESIGN

- 10-bit, dual-channel A/D converter in deep submicron CMOS technology, 20/40Msps
- Single supply voltage: 2.5V
  Independent supply for CMOS output stage with 2.5V/3.3V capability
- ENOB=9.67 @ 20Msps, ENOB=9.4 @ 40Msps, Fin=10MHz
- SFDR typically up to 62.5dB @ 40Msps, Fin=10MHz.
- 1GHz analog bandwidth Track-and-Hold
- Common clocking between channels
- Multiplexed outputs

DESCRIPTION

The TSA1005 belongs to a new generation of high speed, dual-channel Analog to Digital converters, processed in a mainstream 0.25 µm CMOS technology and yielding high performances.

The TSA1005 is specifically designed for applications requiring a very low noise floor, high SFDR and good isolation between channels. It is based on a pipeline structure and digital error correction, providing high static linearity at 20/40 Msp, and Fin = 10 MHz.

For each channel, a voltage reference is integrated to simplify the design and minimize externa components. It is nevertheless possible to use the circuit with external references.

Each ADC output is multiplexed on a common bus with small number of pins. A tri-state capability is available for the output signals, allowing for chip selection. The input signals of the ADC must be differentially driven.

The TSA1005 is supports an extended (0 to +85 C) temperature range, and is available in the small 48-pin TQFP package.

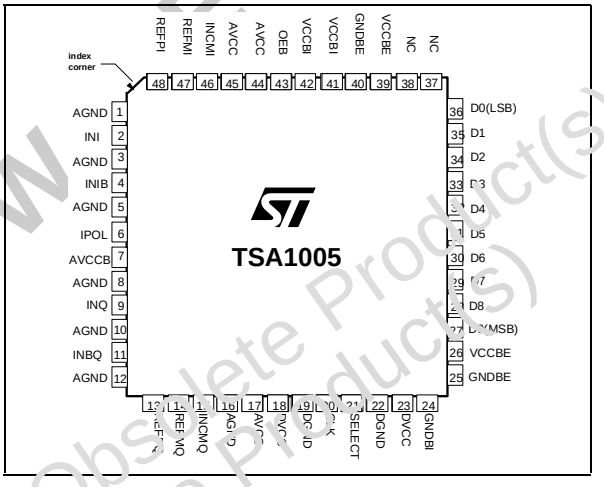
APPLICATIONS

- **Medical imaging and ultrasound**
- **I/Q signal processing applications**
- **High speed data acquisition system**
- **Portable instrumentation**
- **High resolution fax and scanners**

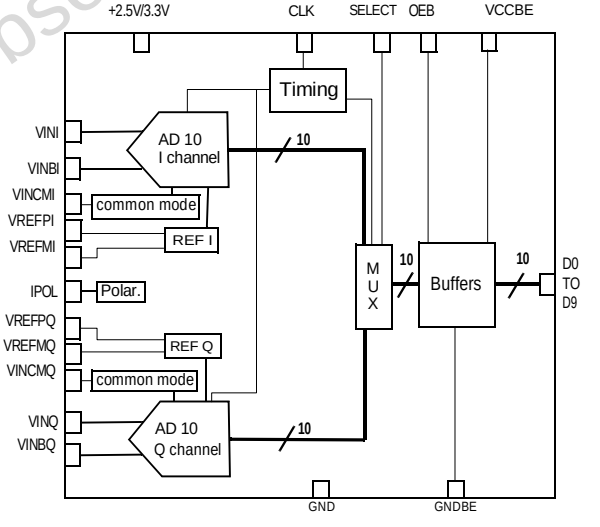
ORDER CODE

Part Number	Temperature Range	Status	Conditioning
TSA1005-20IF	-40 C to +85 C	Sample	Tray
TSA1005-20IFT	-40 C to +85 C	Sample	Tape & Reel
TSA1005I-40IF	0 C to +85 C	Production	Tray
TSA1005-40IFT	0 C to +85 C	Production	Tape & Reel
EVAL1005-20/BA EVAL1005-40/BA	Evaluation board		

PIN CONNECTIONS (top view)

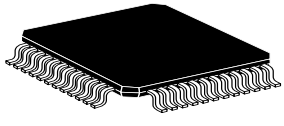


BLOCK DIAGRAM



PACKAGE

7 × 7 mm TQFP48



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Values	Unit
AVCC	Analog Supply voltage (1)	0 to 3.3	V
DVCC	Digital Supply voltage 1)	0 to 3.3	V
VCCBE	Digital buffer Supply voltage 1)	0 to 3.6	V
VCCBI	Digital buffer Supply voltage 1)	0 to 3.3	V
IDout	Digital output current	-100 to 100	mA
Tstg	Storage temperature	+150	C
ESD	HBM: Human Body Model(2) CDM: Charged Device Model(3)	2 1.5	kV
Latch-up	Class(4)	A	

1 All voltage values, except for differential voltage, are with respect to the network ground terminal. The magnitude of input and output voltages must not exceed -0.3 V or VCC

2 ElectroStatic Discharge pulse (ESD pulse) simulating a human body discharge of 100 pF through 1.5 kΩ

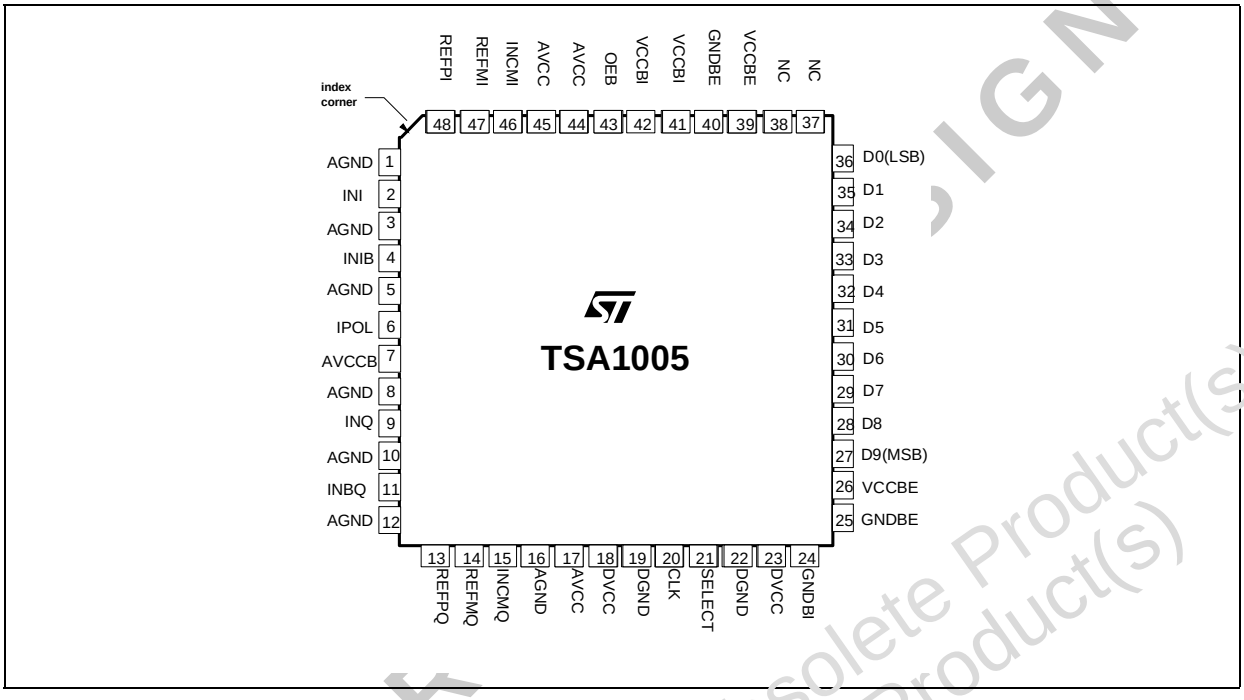
3 Discharge to Ground of a device that has been previously charged.

4 Corporate ST Microelectronics procedure number 0018695

OPERATING CONDITIONS

Symbol	Parameter	TSA1005-20(1)			TSA1005-40			
		Min.	Typ.	Max.	Min.	Typ.	Max.	Unit
AVCC	Analog Supply voltage	2.25	2.5	2.7	2.25	2.5	2.7	V
DVCC	Digital Supply voltage	2.25	2.5	2.7	2.25	2.5	2.7	V
VCCBE	External Digital buffer Supply voltage	2.25	2.5	3.5	2.25	2.5	3.5	V
VCCBI	Internal Digital buffer Supply voltage	2.25	2.5	2.7	2.25	2.5	2.7	V
VREFPI VREFPQ	Forced top voltage reference	0.94		1.4	0.94		1.4	V
VREFMI VREFMQ	Forced bottom reference voltage	0		0.4	0		0.4	V
INCMI INCMQ	Forced input common mode voltage	0.2		1	0.2		1	V

PIN CONNECTIONS (top view)



PIN DESCRIPTION

Pin No	Name	Description	Observation	Pin No	Name	Description	Observation
1	AGND	Analog ground	0V	25	GNDBE	Digital buffer ground	0V
2	INI	I channel analog input		26	VCCBE	Digital Buffer power supply	2.5V/3.3V
3	AGND	Analog ground	0V	27	D9(MSB)	Most Significant Bit output	CMOS output (2.5V/3.3V)
4	INBI	I channel inverted analog input		28	D8	Digital output	CMOS output (2.5V/3.3V)
5	AGND	Analog ground	0V	29	D7	Digital output	CMOS output (2.5V/3.3V)
6	IPOL	Analog bias current input		30	D6	Digital output	CMOS output (2.5V/3.3V)
7	AVCC	Analog power supply	2.5V	31	D5	Digital output	CMOS output (2.5V/3.3V)
8	AGND	Analog ground	0V	32	D4	Digital output	CMOS output (2.5V/3.3V)
9	INQ	Q channel analog input		33	D3	Digital output	CMOS output (2.5V/3.3V)
10	AGND	Analog ground	0V	34	D2	Digital output	CMOS output (2.5V/3.3V)
11	INBQ	Q channel inverted analog input		35	D1	Digital output	CMOS output (2.5V/3.3V)
12	AGND	Analog ground	0V	36	D0(LSB)	Least Significant Bit output	CMOS output (2.5V/3.3V)
13	REFPQ	Q channel top reference voltage		37	NC	Non connected	
14	REFMQ	Q channel bottom reference voltage	0V	38	NC	Non connected	
15	INCMQ	Q channel input common mode		39	VCCBE	Digital Buffer power supply	2.5V/3.3V - See Application Note
16	AGND	Analog ground	0V	40	GNDBE	Digital buffer ground	0V
17	AVCC	Analog power supply	2.5V	41	VCCBI	Digital Buffer power supply	2.5V
18	DVCC	Digital power supply	2.5V	42	VCCBI	Digital Power Supply	2.5V
19	DGND	Digital ground	0V	43	OEB	Output Enable input	2.5V/3.3V CMOS input
20	CLK	Clock input	2.5V CMOS input	44	AVCC	Analog power supply	2.5V
21	SELECT	Channel selection	2.5V CMOS input	45	AVCC	Analog power supply	2.5V
22	DGND	Digital ground	0V	46	INCMI	I channel input common mode	
23	DVCC	Digital power supply	2.5V	47	REFMI	I channel bottom reference voltage	0V
24	GNDBI	Digital buffer ground	0V	48	REFPI	I channel top reference voltage	

ELECTRICAL CHARACTERISTICS

AVCC = DVCC = VCCB = 2.5 V, Fs = 20/40 Msps, Fin = 10.13 MHz, Vin@ -1 dBFS, VREFP = 0.8 V, VREFM = 0 V

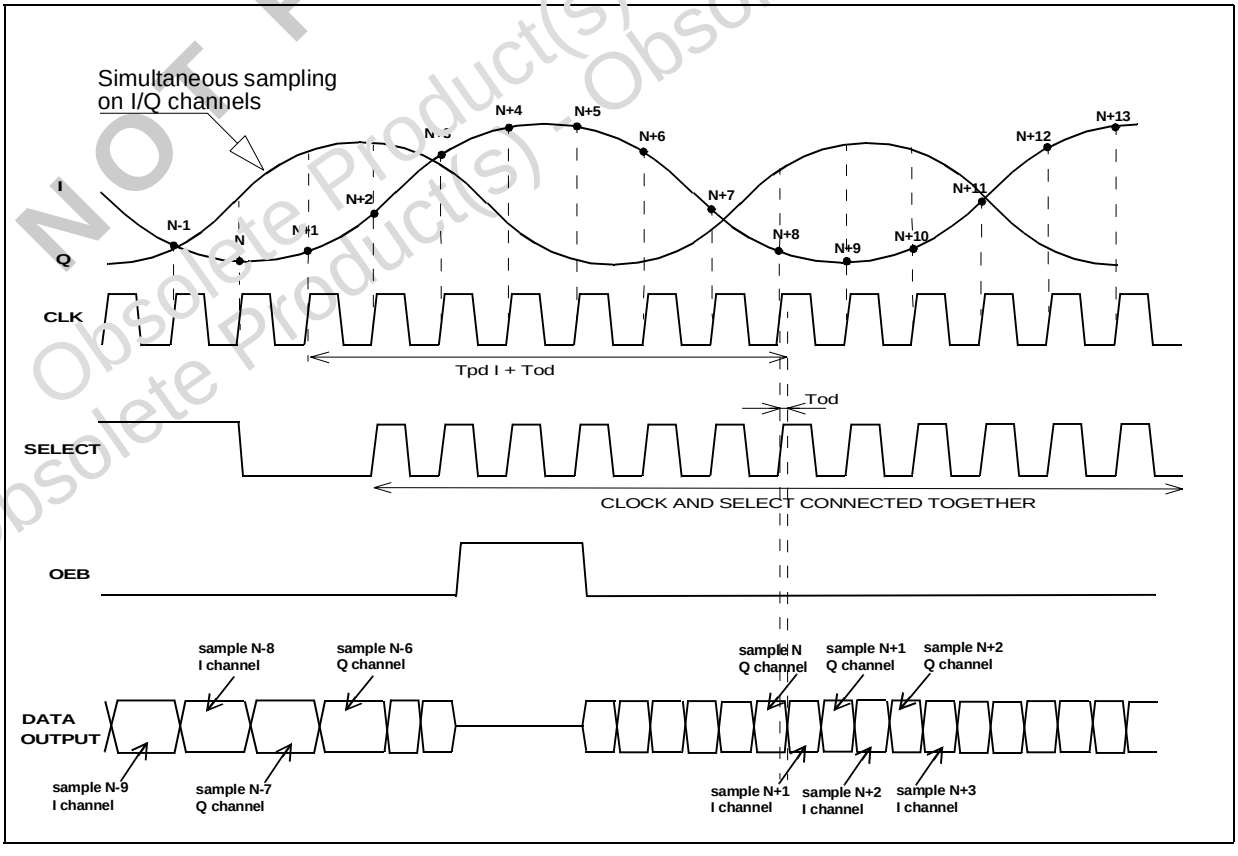
Tamb = 25 C (unless otherwise specified)

TIMING CHARACTERISTICS

Symbol	Parameter.	TSA1005-20(1)			TSA1005-40			
		Min.	Typ.	Max.	Min.	Typ.	Max.	Unit
FS	Sampling Frequency	0.5		20	0.5		40	MHz
DC	Clock Duty Cycle		50		45	50	55	%
TC1	Clock pulse width (high)		25			12.5		ns
TC2	Clock pulse width (low)		25			12.5		ns
Tod	Data Output Delay (Clock edge to Data Valid) - 10pF load capacitance		5			5		ns
Tpd I	Data Pipeline delay for I channel		7			7		cycles
Tpd Q	Data Pipeline delay for Q channel		7.5			7.5		cycles
Ton	Falling edge of OEB to digital output valid data		1			1		ns
Toff	Rising edge of OEB to digital output tri-state		1			1		ns

1 Preliminary data.

TIMING DIAGRAM



CONDITIONS

AVCC = DVCC = VCCB = 2.5V, Fs= 20/40Msps, Fin=2MHz, Vin@ -1dBFS, VREFM=0V
Tamb = 25 C (unless otherwise specified)

ANALOG INPUTS

Symbol	Parameter	TSA1005-20(1)			TSA1005-40			
		Min.	Typ.	Max.	Min.	Typ.	Max.	Unit
VIN-VINB	Full scale reference voltage	1.1	2.0	2.8	1.1	2.0	2.8	Vpp
Cin	Input capacitance		7.0			7		pF
Req	Equivalent input resistor		3.3			1.6		KΩ
BW	Analog Input Bandwidth Vin Full scale, Fs max		1000			1000		MHz
ERB	Effective Resolution Bandwidth		70			70		MHz

1 Preliminary data

DIGITAL INPUTS AND OUTPUTS

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
Clock and Select inputs						
VIL	Logic "0" voltage			0	0.8	V
VIH	Logic "1" voltage		2.0	2.5		V
OEB input						
VIL	Logic "0" voltage			0	0.25 x VCCBE	V
VIH	Logic "1" voltage		0.75 x VCCBE	VCCBE		V
Digital Outputs						
VOL	Logic "0" voltage	Iol=10µA		0	0.1 x VCCBE	V
VOH	Logic "1" voltage	Ioh=10µA	0.9 x VCCBE	VCCBE		V
IOZ	High Impedance leakage current	OEB set to VIH	-1.67	0	1.67	µA
C_L	Output Load Capacitance				15	pF

REFERENCE VOLTAGE

Symbol	Parameter	TSA1005-20(1)			TSA1005-40			
		Min.	Typ.	Max.	Min.	Typ.	Max.	Unit
VREFPI VREFPQ	Top internal reference voltage	0.81	0.88	0.94	0.81	0.88	0.94	V
VINCMI VINCMQ	Input common mode voltage	0.41	0.46	0.50	0.41	0.46	0.50	V

CONDITIONS

AVCC = DVCC = VCCB = 2.5V, Fs= 20/40Msps, Fin=2MHz, Vin@ -1dBFS, VREFP=0.8V, VREFM=0V
Tamb = 25 C (unless otherwise specified)

POWER CONSUMPTION

Symbol	Parameter	TSA1005-20(1)			TSA1005-40			
		Min.	Typ.	Max.	Min.	Typ.	Max.	Unit
ICCA	Analog Supply current		30			69.5	77.1	mA
ICCD	Digital Supply Current		4			3.5	3.77	mA
ICCBE	Digital Buffer Supply Current (10pF load)		6			6.5	7.66	mA
ICCBI	Digital Buffer Supply Current		274			131	176	µA
Pd	Power consumption in normal operation mode		100			199.5	218.6	mW
Rthja	Thermal resistance (TQFP48)		80			80		C/W

ACCURACY

Symbol	Parameter	TSA1005-20(1)			TSA1005-40			
		Min.	Typ.	Max.	Min.	Typ.	Max.	Unit
OE	Offset Error		2.97			2.97		LSB
GE	Gain Error		0.1			0.1		%
DNL	Differential Non Linearity		±0.5			±0.6		LSB
INL	Integral Non Linearity		±0.7			±1		LSB
-	Monotonicity and no missing codes	Guaranteed			Guaranteed			

DYNAMIC CHARACTERISTICS

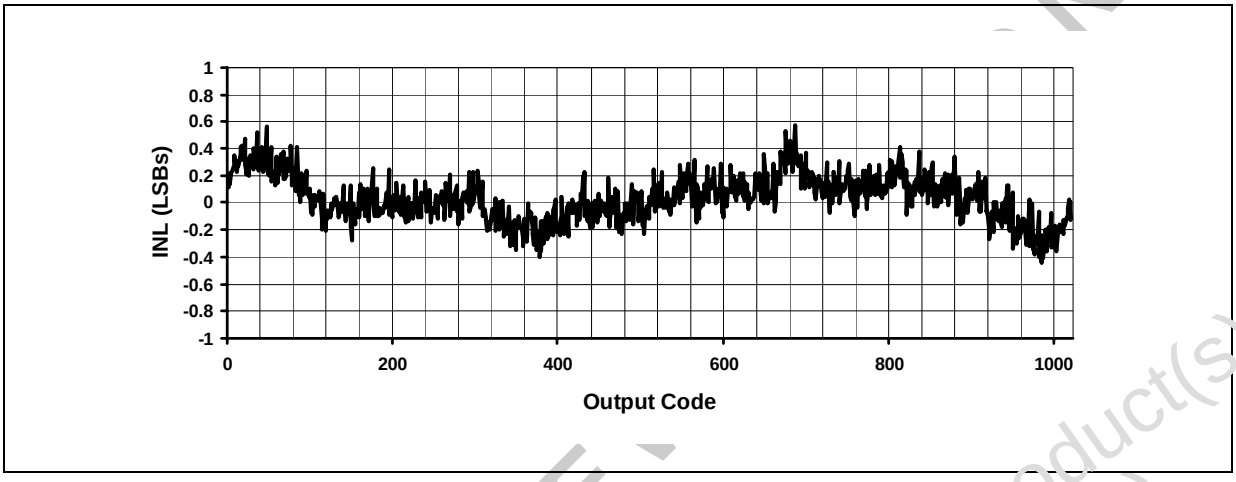
Symbol	Symbol	TSA1005-20(1)			TSA1005-40			
		Min.	Typ.	Max.	Min.	Typ.	Max.	Unit
SFDR	Spurious Free Dynamic Range		-73			-62.6	-58.1	dBc
SNR	Signal to Noise Ratio		60		57.1	59.8		dB
THD	Total Harmonics Distortion		-73			-62	-57.5	dBc
SINAD	Signal to Noise and Distortion Ratio		59		54.9	57.3		dB
ENOB	Effective number of bits		9.67		8.8	9.4		bits

MATCHING BETWEEN CHANNELS

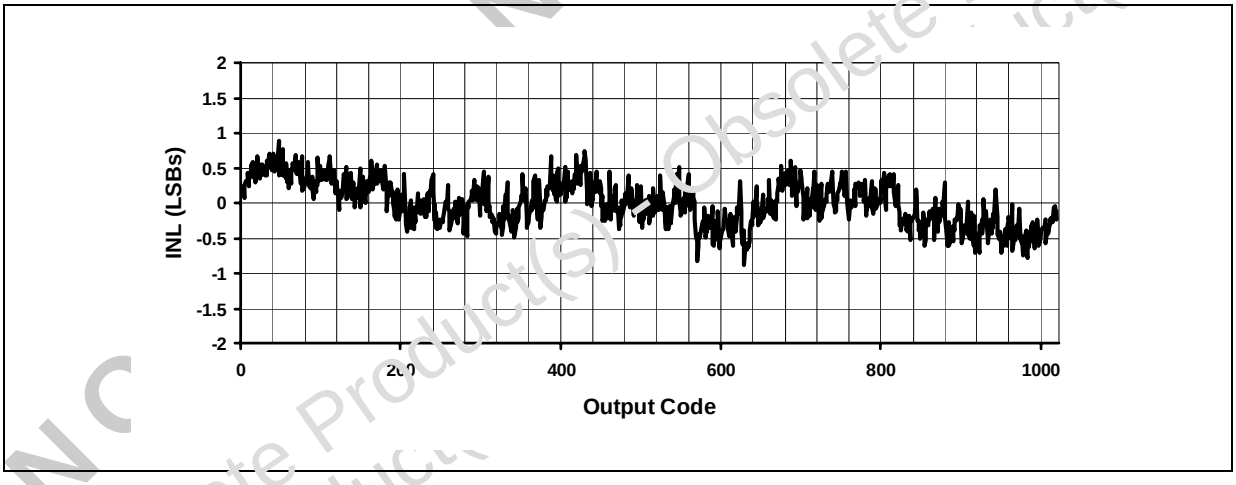
Symbol	Parameter	TSA1005-20(1)			TSA1005-40			
		Min.	Typ.	Max.	Min.	Typ.	Max.	Unit
GM	Gain match		0.04			0.04	1	%
OM	Offset match		0.5			0.5		LSB
PHM	Phase match		1			1		dg
XTLK	Crosstalk rejection		85			85		dB

1 Preliminary data

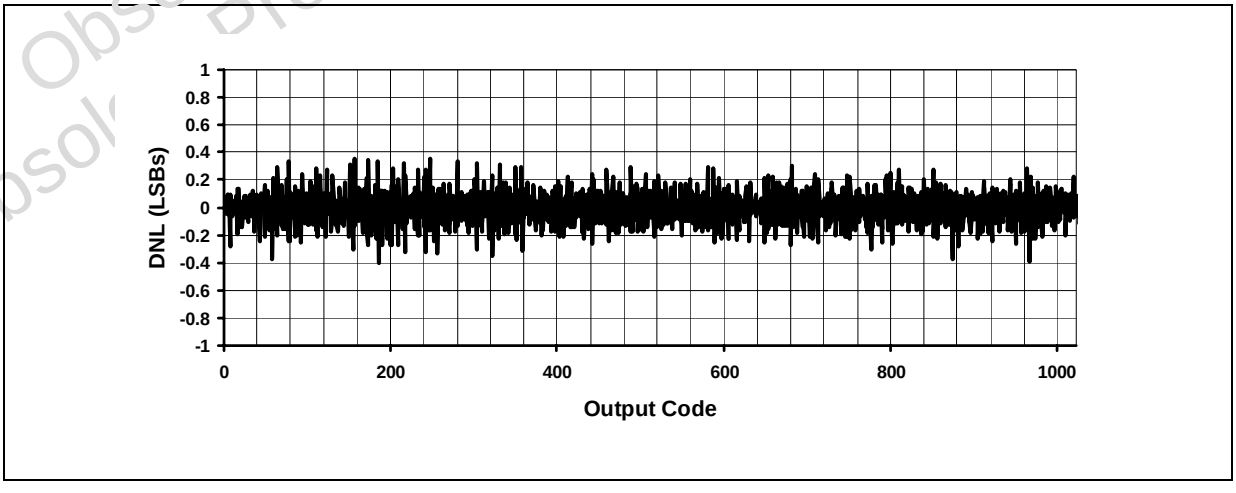
Static parameter: Integral Non Linearity
Fs=20MSPS; Icca=30mA; Fin=10MHz



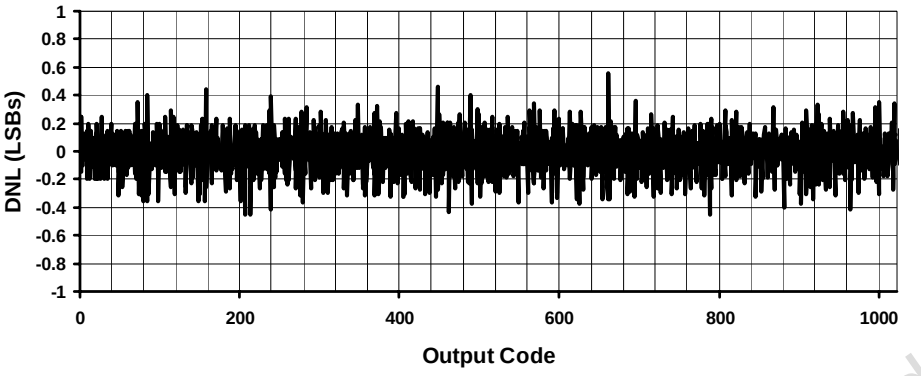
Static parameter: Integral Non Linearity
Fs=40MSPS; Icca=45mA; Fin=10MHz



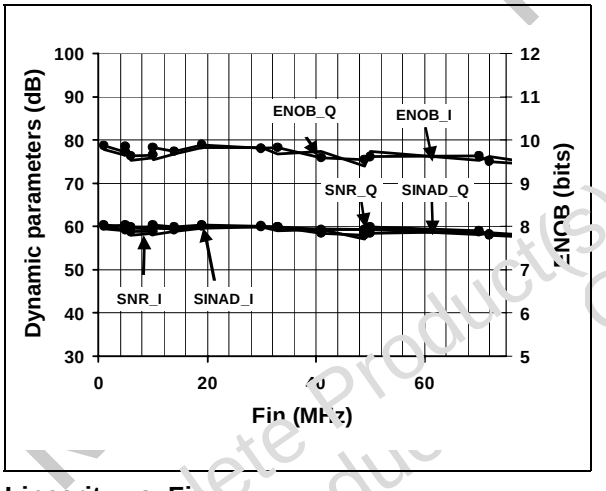
Static parameter: Differential Non Linearity
Fs=20MSPS; Icca=30mA; Fin=10MHz



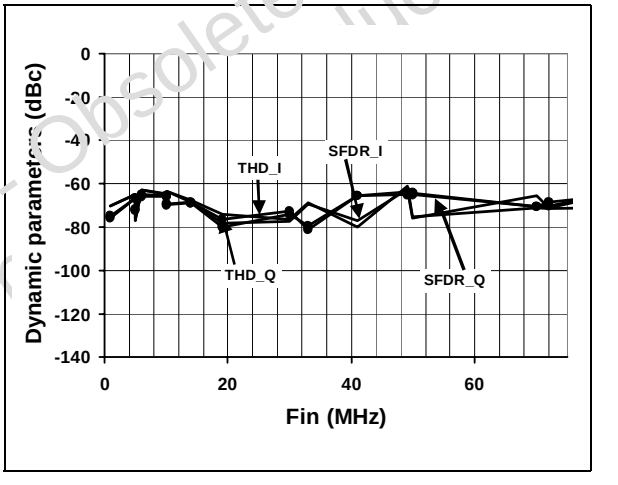
Static parameter: Differential Non Linearity
Fs=40MSPS; Icca=45mA; Fin=10MHz



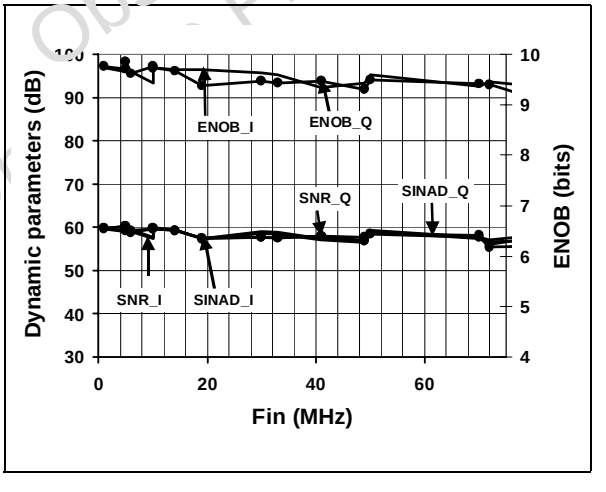
Linearity vs. Fin
Fs=20MHz; Icca=30mA



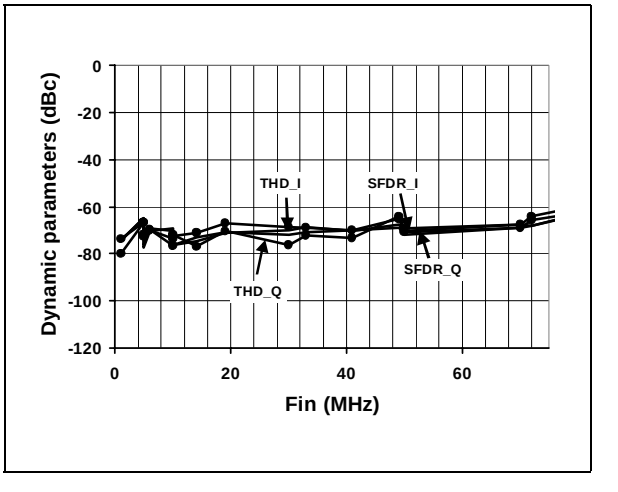
Distortion vs. Fin
Fs=20MHz; Icca=30mA



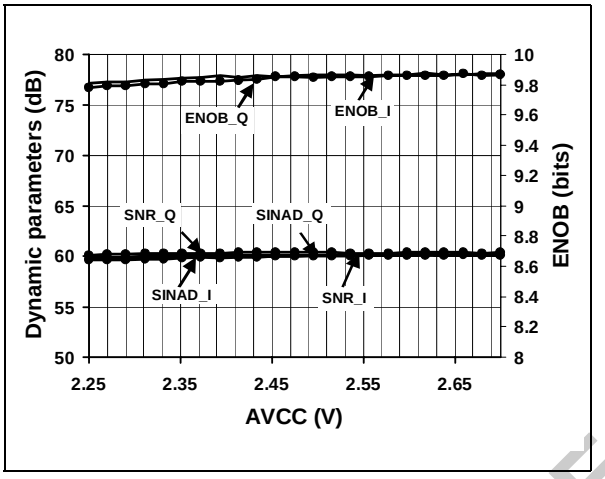
Linearity vs. Fin
Fs=40MHz; Icca=45mA



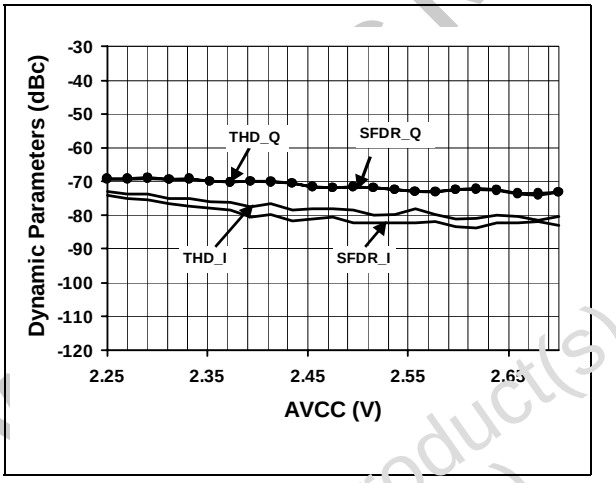
Distortion vs. Fin
Fs=40MHz; Icca=45mA



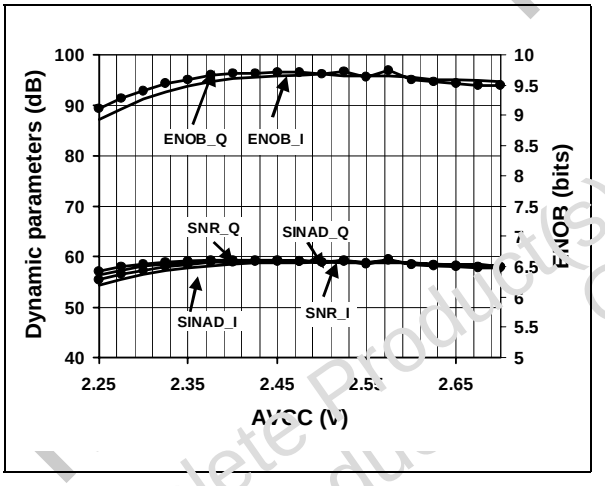
Linearity vs. AVCC
Fs=20MSPS; Icca=30mA; Fin=5MHz



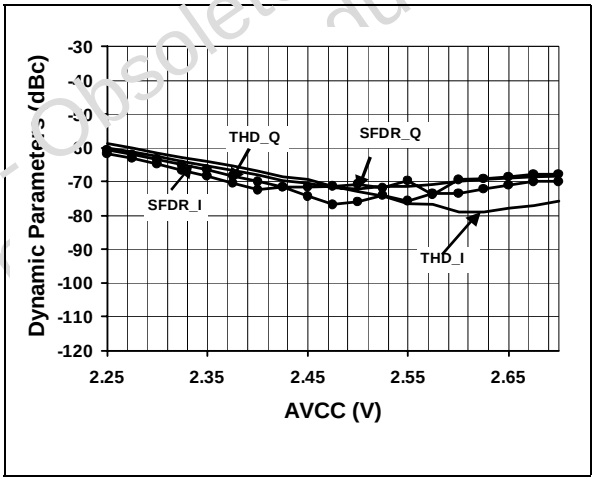
Distortion vs. AVCC
Fs=20MSPS; Icca=30mA; Fin=5MHz



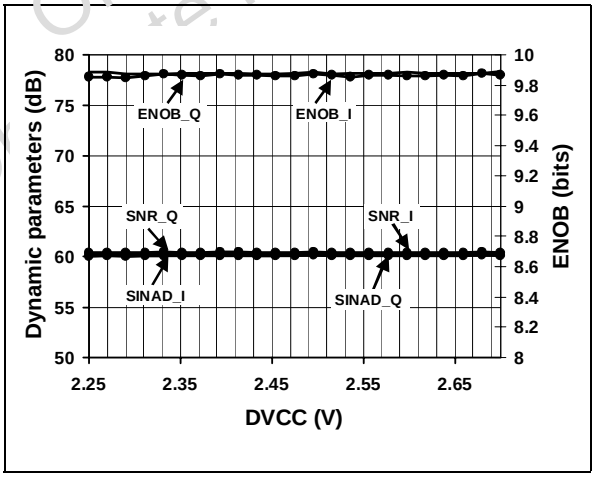
Linearity vs. AVCC
Fs=40MSPS; Icca=45mA; Fin=5MHz



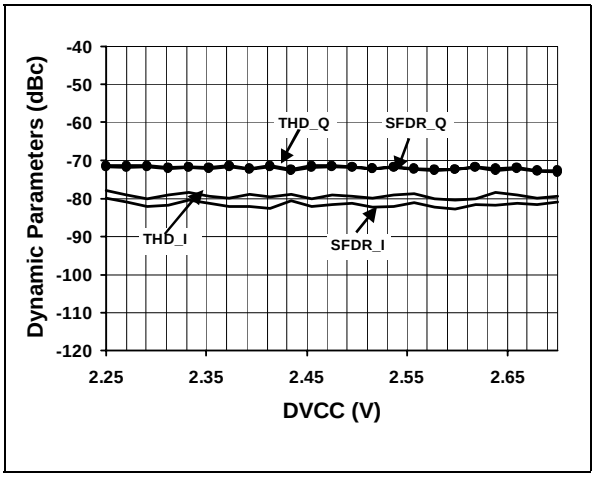
Distortion vs. AVCC
Fs=40MSPS; Icca=45mA; Fin=5MHz



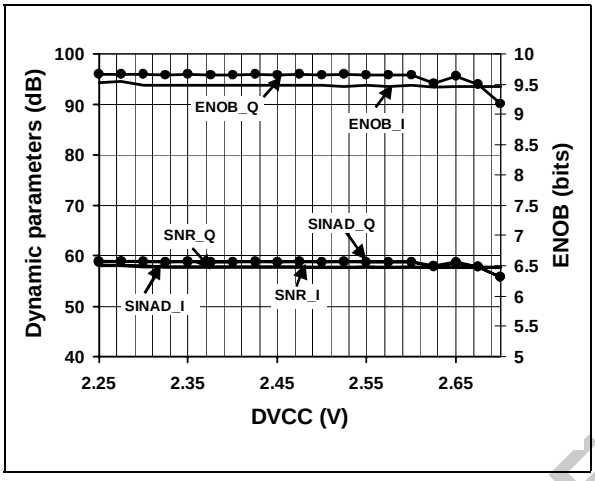
Linearity vs. DVCC
Fs=20MSPS; Icca=30mA; Fin=10MHz



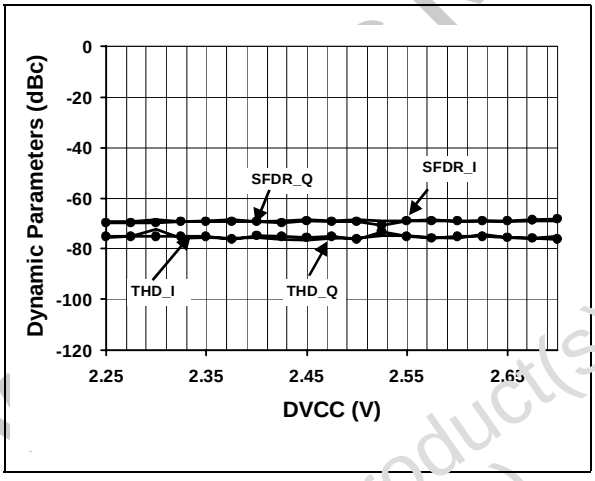
Distortion vs. DVCC
Fs=20MSPS; Icca=30mA; Fin=10MHz



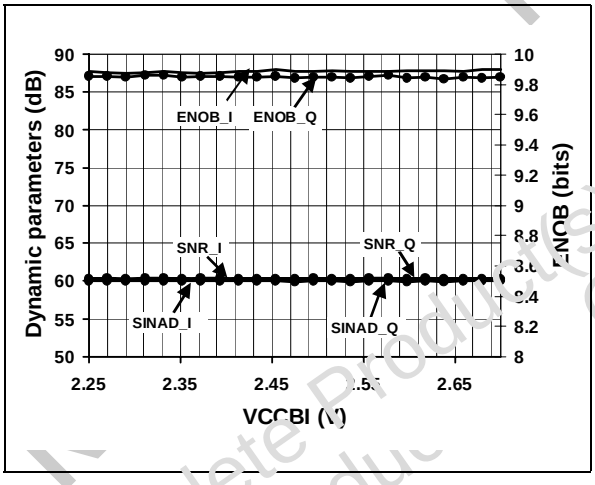
Linearity vs. DVCC
Fs=40MSPS; Icca=45mA; Fin=10MHz



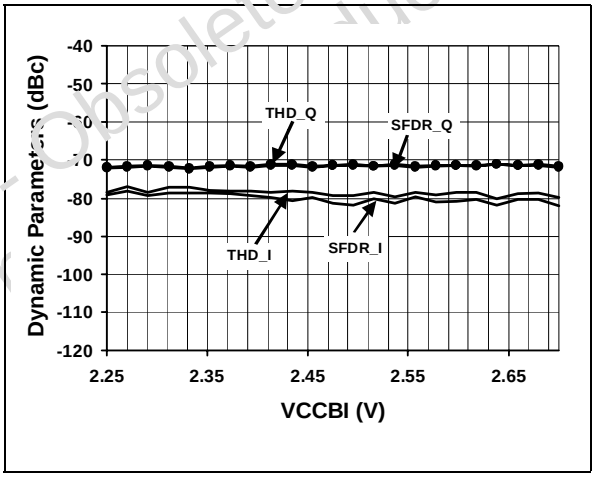
Distortion vs. DVCC
Fs=40MSPS; Icca=45mA; Fin=10MHz



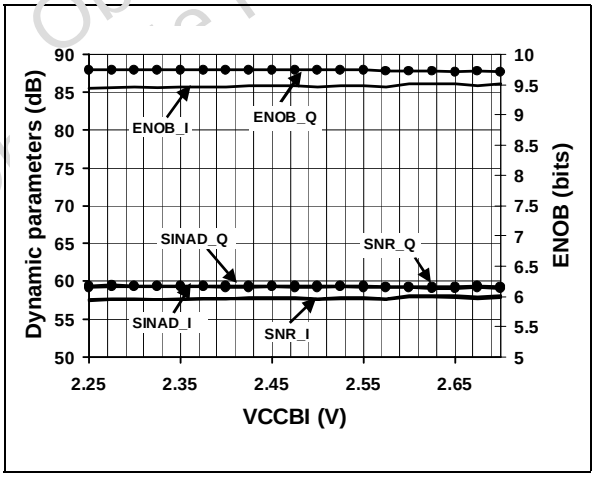
Linearity vs. VCCBI
Fs=20MSPS; Icca=30mA; Fin=10MHz



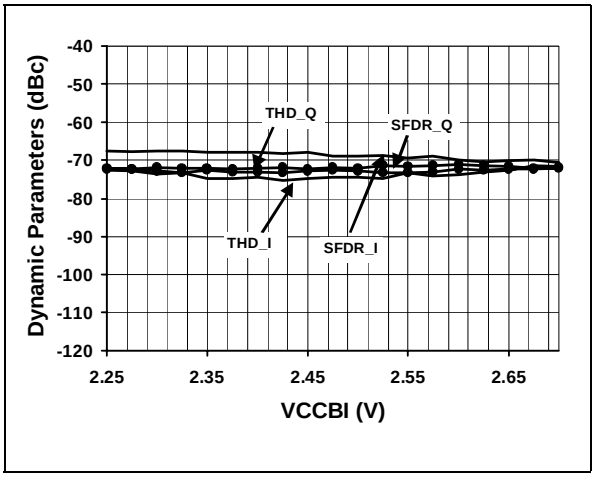
Distortion vs. VCCBI
Fs=20MSPS; Icca=30mA; Fin=10MHz



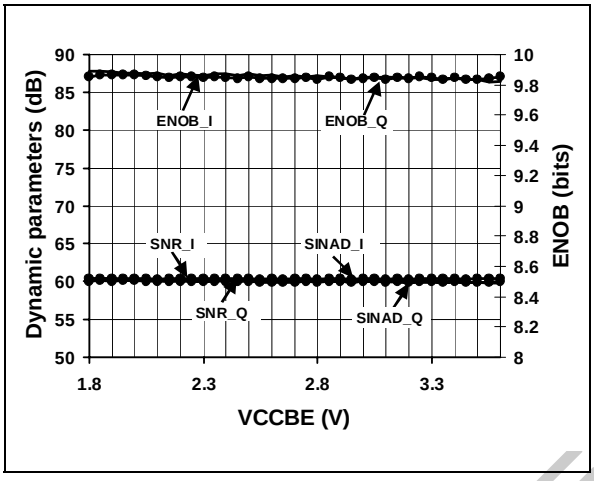
Linearity vs. VCCBI
Fs=40MSPS; Icca=45mA; Fin=10MHz



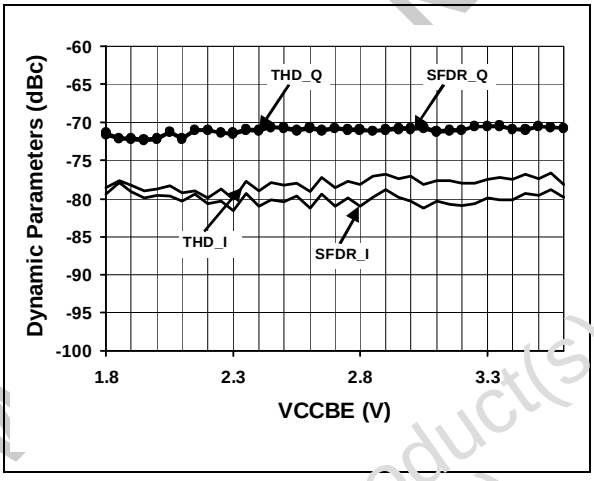
Distortion vs. VCCBI
Fs=40MSPS; Icca=45mA; Fin=10MHz



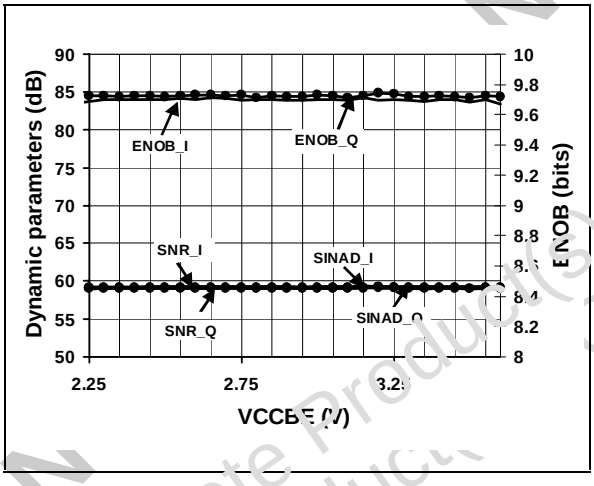
Linearity vs. VCCBE
Fs=20MSPS; Icca=30mA; Fin=10MHz



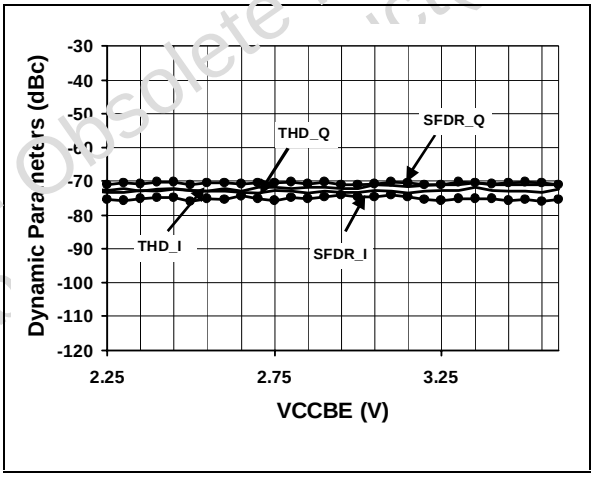
Distortion vs. VCCBE
Fs=20MSPS; Icca=30mA; Fin=10MHz



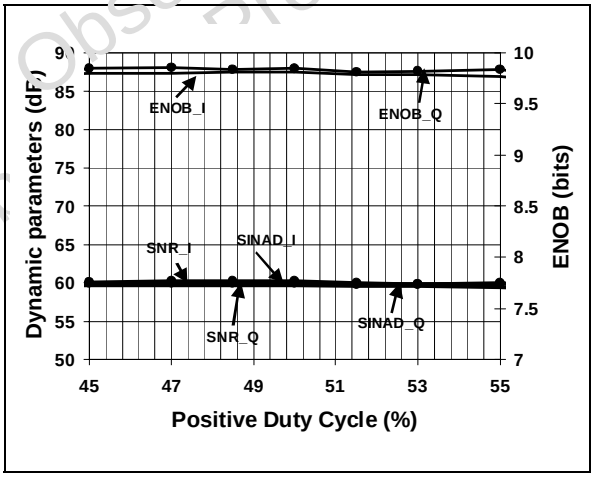
Linearity vs. VCCBE
Fs=40MSPS; Icca=45mA; Fin=10MHz



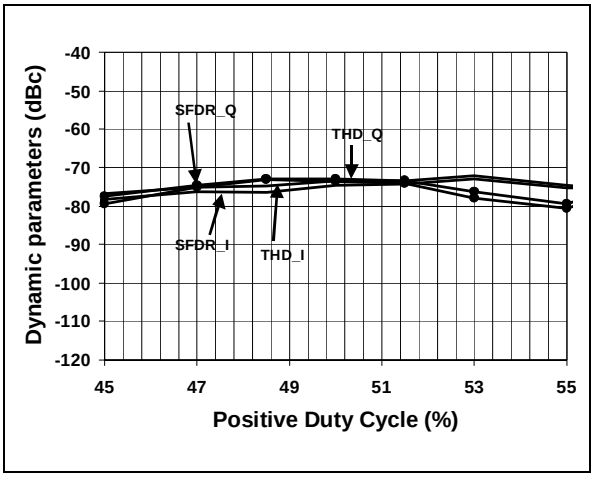
Distortion vs. VCCBE
Fs=40MSPS; Icca=45mA; Fin=10MHz



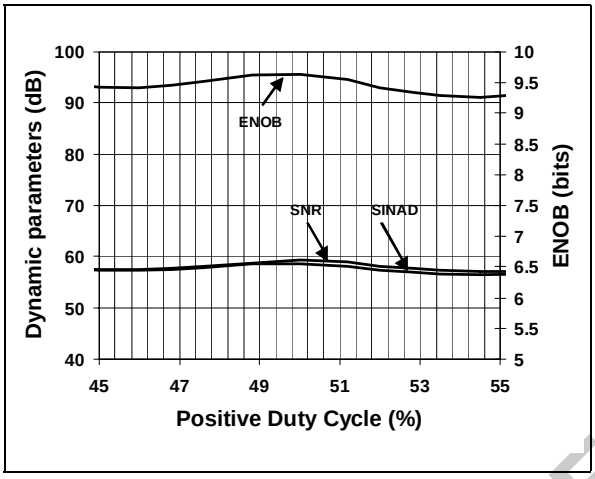
Linearity vs. Duty Cycle
Fs=20MHz; Icca=30mA; Fin=5MHz



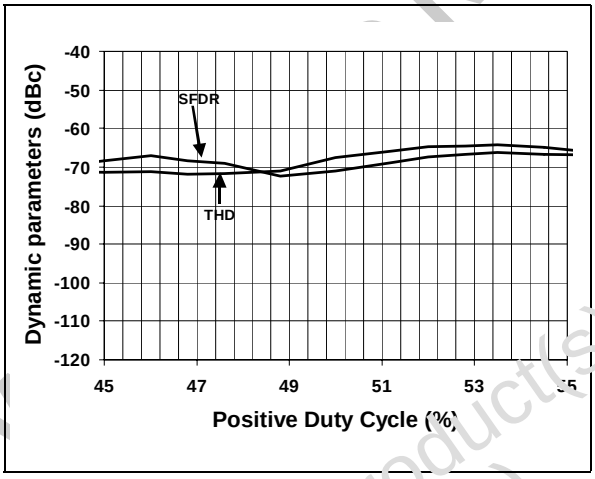
Distortion vs. Duty Cycle
Fs=20MHz; Icca=30mA; Fin=5MHz



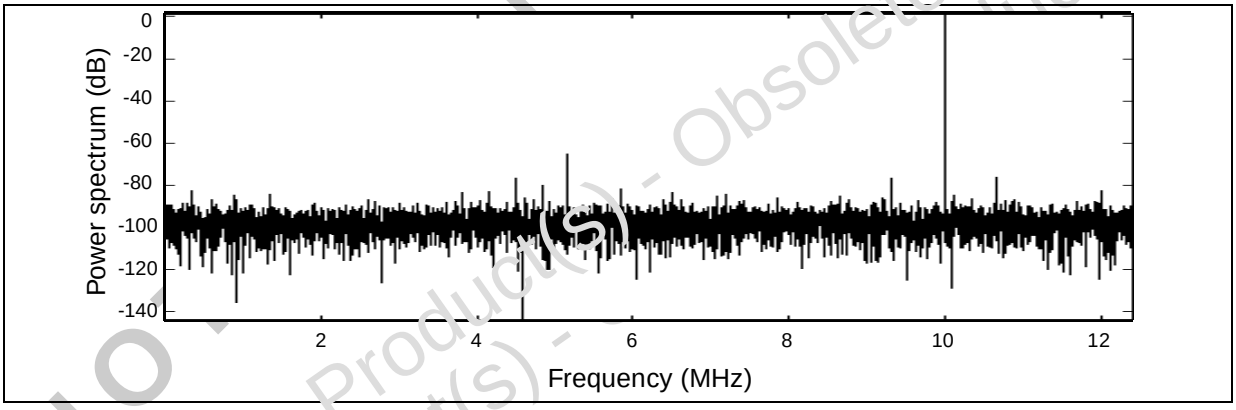
Linearity vs. Duty Cycle
Fs=40MHz; Icca=45mA; Fin=5MHz



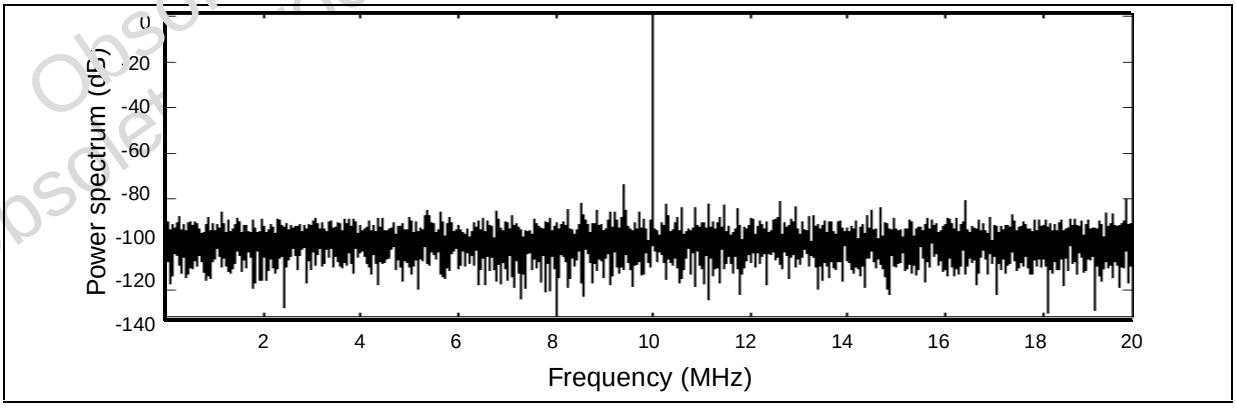
Distortion vs. Duty Cycle
Fs=40MHz; Icca=45mA; Fin=5MHz



Single-tone 8K FFT at 24.8Msps - Q Channel
Fin=10MHz; Icca=30mA, Vin@-1dBFS



Single-tone 8K FFT at 39.7Msps - Q Channel
Fin=10MHz; Icca=45mA, Vin@-1dBFS



DEFINITIONS OF SPECIFIED PARAMETERS

STATIC PARAMETERS

Static measurements are performed using a histogram method with on a 2 MHz input signal, sampled at 40 Msps, which is high enough to fully characterize the test frequency response. An input level of +1 dBFS is required to saturate the signal.

Differential Non Linearity (DNL)
The average deviation of any output code width from the ideal code width of 1 LSB.

Integral Non linearity (INL)
An ideal converter presents a transfer function as being the straight line from the starting code to the ending code. The INL is the deviation for each transition from this ideal curve.

DYNAMIC PARAMETERS

Dynamic measurements are performed by spectral analysis, applied to an input sine wave of various frequencies and sampled at 40 Msps.

The input level is -1 dBFS to measure the linear behavior of the converter. All the parameters are given without correction for the full scale amplitude performance except the calculated ENOB parameter.

Spurious Free Dynamic Range (SFDR)
The ratio between the power of the worst spurious signal (not always an harmonic) and the amplitude of fundamental tone (signal power) over the full Nyquist band. It is expressed in dBc.

Total Harmonic Distortion (THD)
The ratio of the rms sum of the first five harmonic distortion components to the rms value of the fundamental line. It is expressed in dB.

Signal to Noise Ratio (SNR)
The ratio of the rms value of the fundamental component to the rms sum of all other spectral components in the Nyquist band ($f_S/2$) excluding DC, fundamental and the first five harmonics. SNR is reported in dB.

Signal to Noise and Distortion Ratio (SINAD)
Similar ratio as for SNR but including the harmonic distortion components in the noise figure (not DC signal). It is expressed in dB.

From the SINAD, the Effective Number of Bits (ENOB) can easily be deduced using the formula:

$$SINAD = 6.02 \times ENOB + 1.76 \text{ dB}.$$

When the applied signal is not Full Scale (FS), but has an A_0 amplitude, the SINAD expression becomes:

$$SINAD_{2A_0} = SINAD_{Full\ Scale} + 20 \log (2A_0/FS)$$

$$SINAD_{2A_0} = 6.02 \times ENOB + 1.76dB + 20 \log (2A_0/FS)$$

The ENOB is expressed in bits.

Analog Input Bandwidth
The maximum analog input frequency at which the spectral response of a full power signal is reduced by 3 dB. Higher values can be achieved with smaller input levels.

Effective Resolution Bandwidth (ERB)
The band of input signal frequencies that the ADC is intended to convert without loosing linearity i.e. the maximum analog input frequency at which the SINAD is decreased by 3dB or the ENOB by 1/2 bit.

Pipeline delay
Delay between the initial sample of the analog input and the availability of the corresponding digital data output, on the output bus. Also called data latency. It is expressed as a number of clock cycles.

DETAILED INFORMATION

The TSA1005 is a dual-channel, 10-bit resolution analog to digital converter based on a pipeline structure and the latest deep sub micron CMOS process to achieve the best performances in terms of linearity and power consumption.
Each channel achieves 10-bit resolution through the pipeline structure. A latency time of 7 clock periods is necessary to obtain the digitized data on the output bus.
The input signals are simultaneously sampled on both channels on the rising edge of the clock. The output data is valid on the rising edge of the clock for I channel and on the falling edge of the clock for Q channel. The digital data out from the different stages must be time delayed depending on their order of conversion. Then a digital data correction completes the processing and ensures the validity of the ending codes on the output bus.
The structure has been specifically designed to accept differential signals.
The TSA1005 is pin to pin compatible with the dual 12bits/20Msps TSA1204 and the dual 12bits/40Msps TSA1203.

COMPLEMENTARY FUNCTIONS

Some functionalities have been added in order to simplify as much as possible the application board. These operational modes are described as followed.

Output Enable (OEB)

When set to low level (VIL), all digital outputs remain active and are in low impedance state. When set to high level (VIH), all digital outputs buffers are in high impedance state while the converter goes on sampling. When OEB is set to a low level again, the data are then present on the output with a very short Ton delay.
Therefore, this allows the chip select of the device. The timing diagram summarizes this functionality. In order to remain in the normal operating mode, this pin should be grounded through a low value of resistor.

SELECT

The digital data out from each ADC core are multiplexed together to share the same output bus. This prevents from increasing the number of pins and enables to keep the same package as single channel ADC like TSA1002.

The selection of the channel information is done through the "SELECT" pin. When set to high level (VIH), the I channel data are present on the bus D0-D9. When set to low level (VIL), the Q channel data are on the output bus D0-D9.

Connecting SELECT to CLK allows I and Q channels to be simultaneously present on D0-D9; I channel on the rising edge of the clock and Q channel on the falling edge of the clock. (see timing diagram page 2).

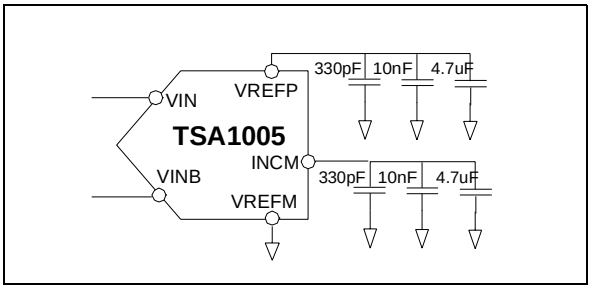
REFERENCES AND COMMON MODE CONNECTION

VREFM must be always connected externally.

Internal reference and common mode

In the default configuration, the ADC operates with its own reference and common mode voltages generated by its internal bandgap. VREFM pins are connected externally to the Analog Ground while VREFP (respectively INCM) are set to their internal voltage of 0.88V (respectively 0.46V). It is recommended to decouple the VREFP and INCM in order to minimize low and high frequency noise (refer to Figure 1)

Figure 1: Internal reference and common mode setting



External reference and common mode

Each of the voltages VREFP and INCM can be fixed externally to better fit to the application needs (Refer to table íOPERATING CONDITIONSí page 4 for min/max values).

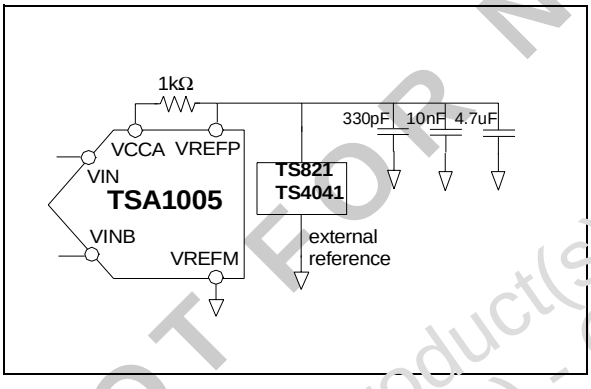
The VREFP, VREFM voltages set the analog dynamic at the input of the converter that has a full scale amplitude of 2*(VREFP-VREFM). Using internal references, the dynamic range is 1.8V.

The INCM is the mid voltage of the analog input signal.

It is possible to use an external reference voltage device for specific applications requiring even better linearity, accuracy or enhanced temperature behavior.

Using the STMicroelectronics TS821 or TS4041-1.2 Vref leads to optimum performances when configured as shown on Figure 2.

Figure 2: External reference setting



DRIVING THE DIFFERENTIAL ANALOG INPUTS

The TSA1005 has been designed to obtain optimum performances when being differentially driven. An RF transformer is a good way to achieve such performances.

Figure 3 describes the schematics. The input signal is fed to the primary of the transformer, while the secondary drives both ADC inputs. The common mode voltage of the ADC (INCM) is connected to the center-tap of the secondary of the transformer in order to bias the input signal around this common voltage, internally set to 0.46V. It determines the DC component of the analog signal. As being an high impedance input, it acts as an I/O and can be externally driven to adjust this DC component. The INCM is decoupled to maintain a low noise level on this node. Our evaluation board is mounted with a 1:1 ADT1-1WT transformer from Minicircuits. You might also use a higher impedance ratio (1:2 or 1:4) to reduce the driving requirement on the analog signal source.

Each analog input can drive a 1.4Vpp amplitude input signal, so the resultant differential amplitude is 2.8Vpp.

Figure 3: Differential input configuration with transformer

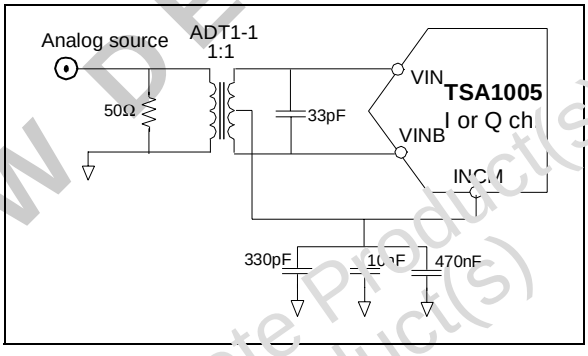


Figure 4 represents the biasing of a differential input signal in AC-coupled differential input configuration. Both inputs VIN and VINB are centered around the common mode voltage, that can be let internal or fixed externally.

Figure 4: AC-coupled differential input

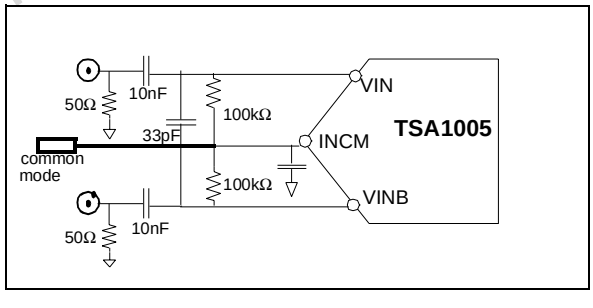
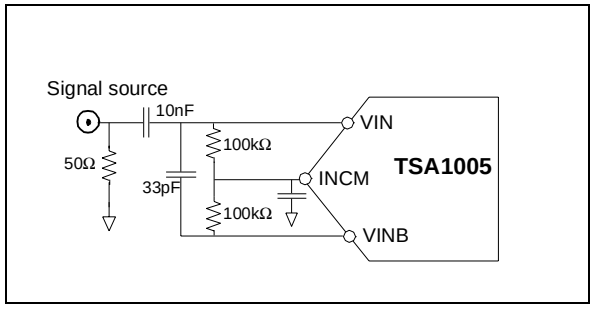


Figure 5: AC-coupled Single-ended input



Clock input

The TSA1005 performance is very dependant on your clock input accuracy, in terms of aperture jitter; the use of low jitter crystal controlled oscillator is recommended.

The duty cycle must be between 45% and 55%.

The clock power supplies must be separated from the ADC output ones to avoid digital noise modulation at the output.

It is recommended to always keep the circuit clocked, even at the lowest specified sampling frequency of 0.5Msps, before applying the supply voltages.

Power consumption

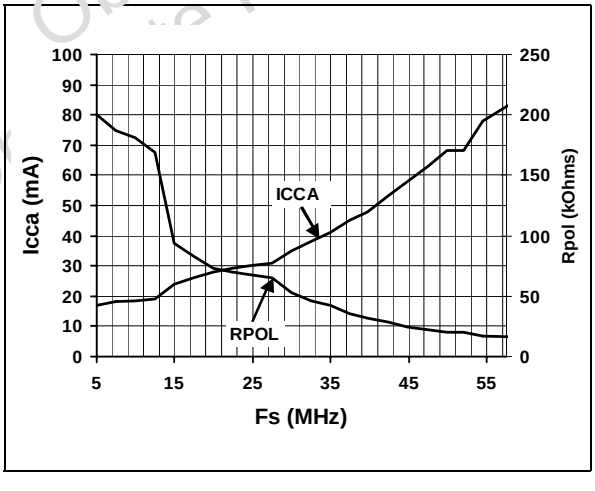
So as to optimize both performance and power consumption of the TSA1005 according the sampling frequency, a resistor is placed between IPOL and the analog Ground pins. Therefore, the total dissipation is adjustable from 5Msps up to 40Msps.

The TSA1005 will combine highest performances and lowest consumption at 20Msps when Rpol is equal to 70kΩ, at 40Msps when Rpol is equal to 35kΩ. These values are nevertheless dependant on application and environment.

At lower sampling frequency range, this value of resistor may be adjusted in order to decrease the analog current without any degradation of dynamic performances.

The figure 6 sums up the relevant data.

Figure 6: analog current consumption optimization depending on Rpol value



APPLICATION

Layout precautions

To use the ADC circuits in the best manner at high frequencies, some precautions have to be taken for power supplies:

- First of all, the implementation of 4 separate proper supplies and ground planes (analog, digital, internal and external buffer ones) on the PCB is recommended for high speed circuit applications to provide low inductance and low resistance common return.

The separation of the analog signal from the digital part is mandatory to prevent noise from coupling onto the input signal. The best compromise is to connect from one part AGND, DGND, GNDBI in a common point whereas GNDBE must be isolated. Similarly, the power supplies AVCC, DVCC and VCCBI must be separated from the VCCBE one.

- Power supply bypass capacitors must be placed as close as possible to the IC pins in order to improve high frequency bypassing and reduce harmonic distortion.

- Proper termination of all inputs and outputs must be incorporated with output termination resistors; then the amplifier load will be only resistive and the stability of the amplifier will be improved. All leads must be wide and as short as possible especially for the analog input in order to decrease parasitic capacitance and inductance.

- To keep the capacitive loading as low as possible at digital outputs, short lead lengths of routing are essential to minimize currents when the output changes. To minimize this output capacitance, buffers or latches close to the output pins will relax this constraint.

- Choose component sizes as small as possible (SMD).

Digital Interface application

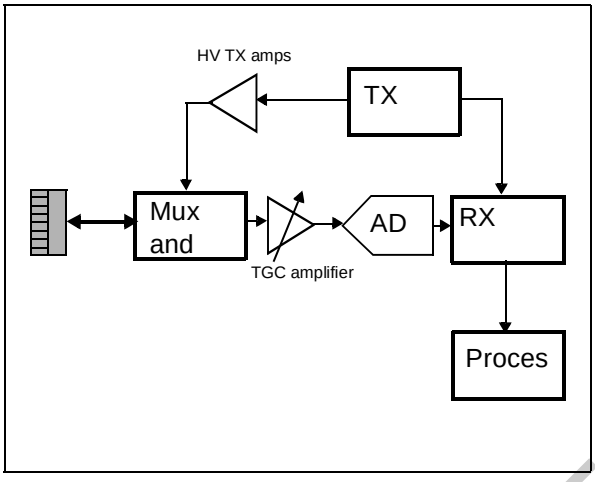
Thanks to its wide external buffer power supply range, the TSA1005 is perfectly suitable to plug in to 2.5V low voltage DSPs or digital interfaces as well as to 3.3V ones.

Medical Imaging application

Driven by the demand of the applications requiring nowadays either portability or high degree of parallelism (or both), this product has been developed to satisfy medical imaging, and telecom infrastructures needs.

As a typical system diagram shows figure 10, a narrow input beam of acoustic energy is sent into a living body via the transducer and the energy reflected back is analyzed.

Figure 7: Medical imaging application



The transducer is a piezoelectric ceramic such as zirconium titanate. The whole array can reach up to 512 channels.

The TX beam former, amplified by the HV TX amps, delivers up to 100V amplitude excitation pulses with phase and amplitude shifts.

The mux and T/R switch is a two way input signal transmitter/ output receiver.

To compensate for skin and tissues attenuation effects, The Time Gain Compensation (TGC) amplifier is an exponential amplifier that enables the amplification of low voltage signals to the ADC input range. Differential output structure with low noise and very high linearity are mandatory factors.

These applications need high speed, low power and high performance ADCs. 10-12 bit resolution is necessary to lower the quantification noise. As multiple channels are used, a dual converter is a must for room saving issues.

The input signal is in the range of 2 to 20MHz (mainly 2 to 7MHz) and the application uses mostly a 4 over-sampling ratio for Spurious Free Dynamic Range (SFDR) optimization.

The next RX beam former and processing blocks enable the analysis of the outputs channels versus the input beam.

EVAL1005/BA evaluation board

The EVAL1005/BA is a 4-layer board with high decoupling and grounding level. The schematic of the evaluation board is reported figure 11 and its top overlay view figure 10.The characterization of the board has been made with a fully ADC devoted test bench as shown on Figure 8. The analog input signal must be filtered to be very pure.

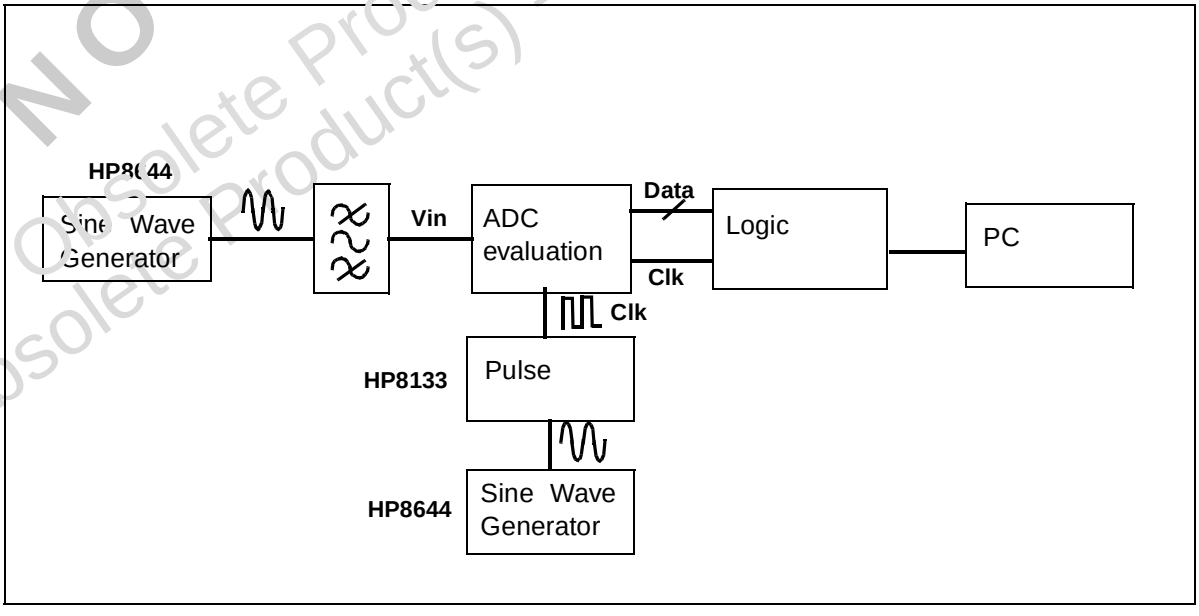
The dataready signal is the acquisition clock of the logic analyzer.

The ADC digital outputs are latched by the octal buffers 74LCX573.

All characterization measurements have been made with:

- SFSR=1dB for static parameters.
- SFSR=-1dB for dynamic parameters.

Figure 8: Analog to Digital Converter characterization bench



Operating conditions of the evaluation board:

Find below the connections to the board for the power supplies and other pins:

board notation	connection	internal voltage (V)	external voltage (V)
AV	AVCC		2.5
AG	AGND		0
RPI	REFPI	0.88	0.94 to 1.4
RMI	REFMI		0 to 0.4
CMI	INCMI	0.46	0.2 to 1
RPQ	REFPQ	0.88	0.94 to 1.4
RMQ	REFMQ		0 to 0.4
CMQ	INCMQ	0.46	0.2 to 1
DV	DVCC		2.5
DG	DGND		0
GB1	GNDBI		0
VB1	VCCBI		2.5
GB2	GNDBE		0
VB2	VCCBE		2.5/3.3
GB3	GNDB3		0
VB3	VCCB3		2.5

Care should be taken for the evaluation board considering the fact that the outputs of the converter are 2.5V/3.3V (VB2, tolerant whereas the 74LCX573 external buffers are operating up to 2.5V.
The ADC outputs on the connector J6 are D11 (MSB) to D2 (LSB).

Single and Differential Inputs:

The ADC board components are mounted to test the TSA1005 with single analog input; the ADT1-1WT transformer enables the differential drive into the converter; in this configuration, the resistors RSI6, RSI7, RSI8 for I channel (respectively RSQ6, RSQ7, RSQ8 for Q one) are connected as short circuits whereas RSI5, RSI9 (respectively RSQ5, RSQ9) are open circuits.
The other way is to test it via JI1 and JI1B differential inputs. So, the resistances RSI5, RSI9 for I channel (respectively RSQ5, RSQ9 for Q one) are connected as short circuits whereas RSI6, RSI7, RSI8 (respectively RSQ6, RSQ7, RSQ8 for Q one) are open circuits.

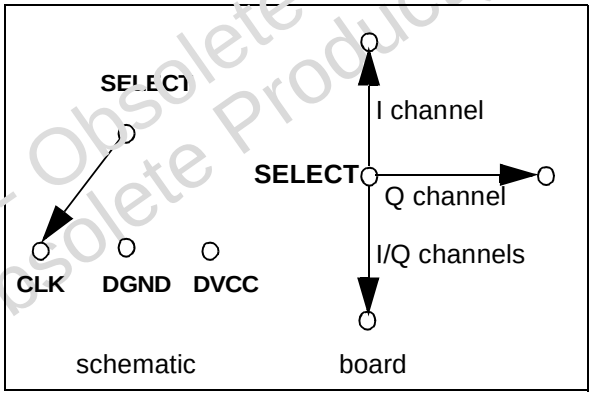
Grounding consideration

So as to better reject noise on the board, connect on the bottom overlay AG (AGND), DG(DGND), GB1(GNDBI) together from one part, and GB2(GNDBE) with GB3(GNDB3) from the other part.

Mode select

So as to evaluate a single channel or the dual ones, you have to connect on the board the relevant position for the SELECT pin.
With the strap connected:
- to the upper connectors, the I channel at the output is selected.
- horizontally, the Q channel at the output is selected.
- to the lower connectors, both channels are selected, relative to the clock edge.

Figure 9: mode select



Consumption adjustment

Before any characterization, care should be taken to adjust the Rpol (Raj1) and therefore Ipol value in function of your sampling frequency.

Figure 10: Printed circuit of evaluation board.

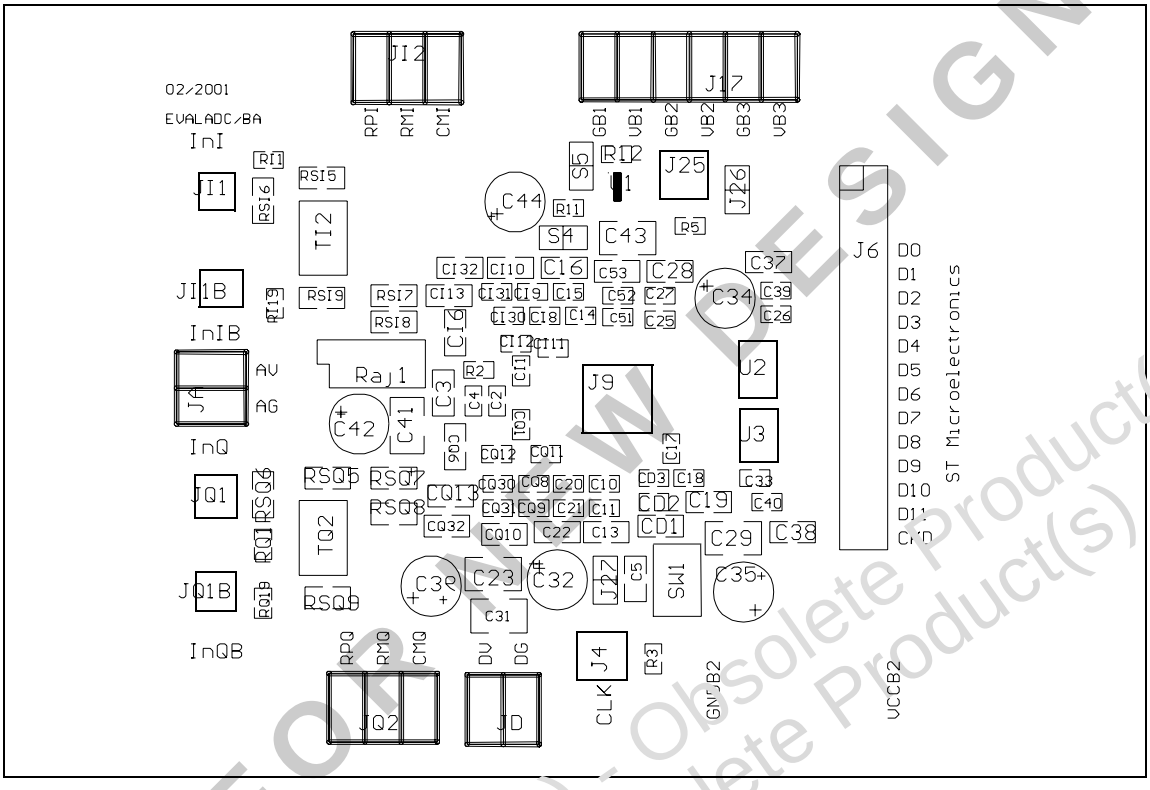


Figure 11: TSA1005 Evaluation board schematic

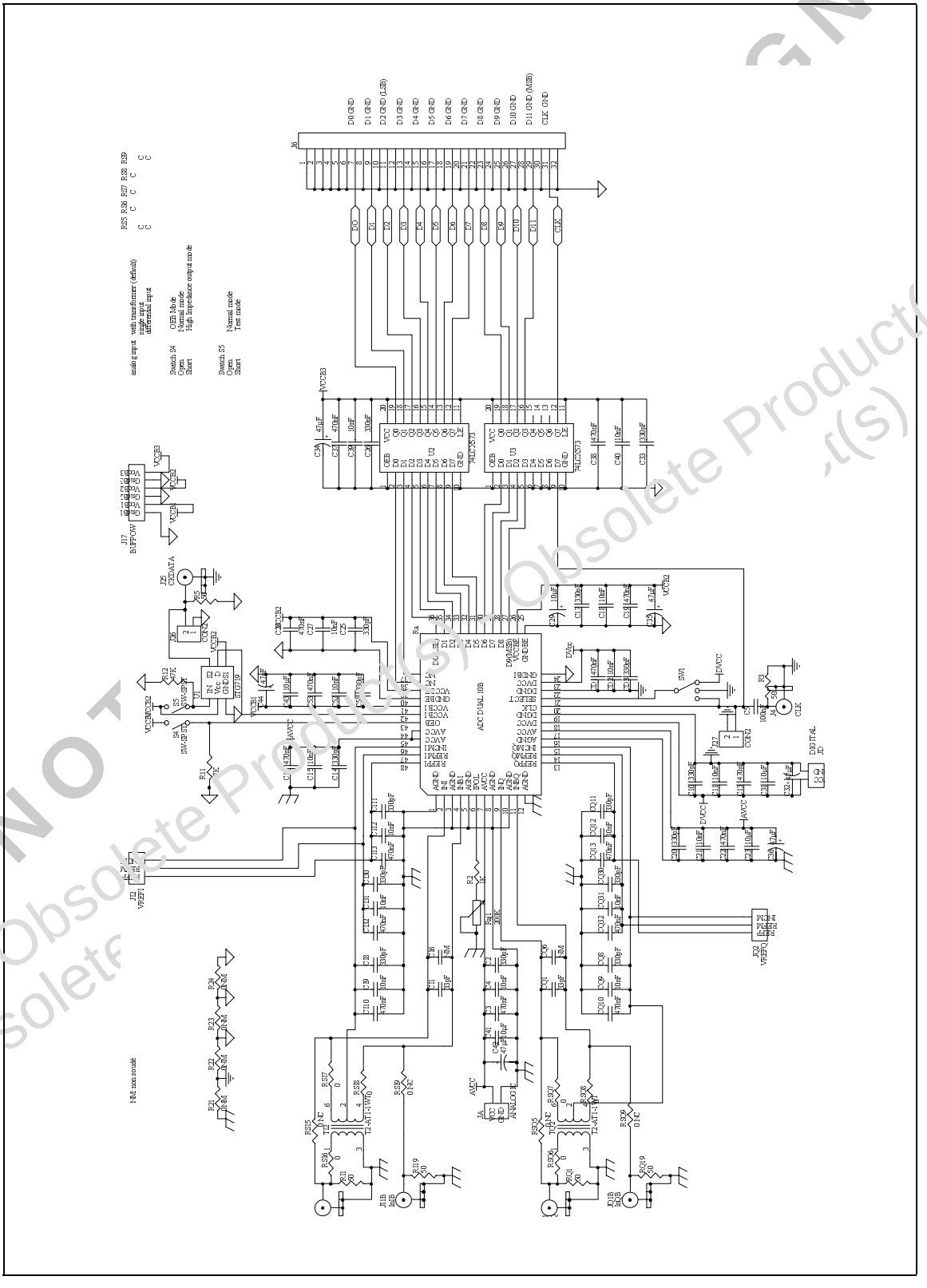


Figure 12: Printed circuit board - List of components

Name	Part Type	Footprint	Name	Part Type	Footprint	Name	Part Type	Footprint	Name	Part Type	Footprint
RSQ6	0	805	CD2	10nF	603	C26	330pF	603	CQ6	NC	805
RSQ7	0	805	C40	10nF	603	C20	330pF	603	CI6	NC	805
RSQ8	0	805	C39	10nF	603	C33	330pF	603	U2	74LCX573	TSSOP20
RSI6	0	805	CQ12	10nF	603	C25	330pF	603	U3	74LCX573	TSSOP20
RSI7	0	805	CQ9	10nF	603	CI1	33pF	603	U1	STG719	SOT23-6
RSI8	0	805	C52	10nF	603	CQ1	33pF	603	JA	ANALOGIC	connector
R3	47	603	C18	10nF	603	C34	47µF	RB.1	J17	BUFPOW	connector
R5	47	603	C21	10nF	603	C42	47µF	RB.1	J25	CKDATA	SMA
RQ19	47	603	C4	10nF	603	C35	47µF	RB.1	J4	CLK	SMA
RI1	47	603	C15	10nF	603	C44	47µF	RB.1	J27	CON2	SIP2
RQ1	47	603	C27	10nF	603	C36	47µF	RB.1	J26	CON2	SIP2
RI19	47	603	C11	10nF	603	C32	47µF	RB.1	JD	DIGITAL	connector
RSI9	0NC	805	CI9	10nF	603	C37	470nF	805	JI1	InI	SMA
RSQ5	0NC	805	CI12	10nF	603	CQ10	470nF	805	JI1B	InIB	SMA
RSQ9	0NC	805	CI31	10nF	603	C28	470nF	805	JQ1	InQ	SMA
RSI5	0NC	805	CQ31	10nF	603	CI10	470nF	805	JQ1B	InQB	SMA
R24	0NC	805	CQ30	330pF	603	CQ32	470nF	805	SW1	SWITCH	connector
R23	0NC	805	CI11	330pF	603	CQ13	470nF	805	S5	SW-SPST	connector
R21	0NC	805	C51	330pF	603	CI32	470nF	805	S4	SW-SPST	connector
R22	0NC	805	C2	330pF	603	C13	470nF	805	TI2	T2-AT1-1WT	ADT
R2	1K	603	C17	330pF	603	C53	470nF	805	TQ2	T2-AT1-1WT	ADT
R12	47K	603	CD3	330pF	603	C16	470nF	805	JI2	VREFI	connector
R11	47K	603	C10	330pF	603	C3	470nF	805	JQ2	VREFQ	connector
Raj1	200K	VR5	CQ8	330pF	603	C22	470nF	805	J6	32Pin	IDC-32
		trimmer	CQ11	330pF	603	CI13	470nF	805			connector
C23	10µF	1210	CI8	330pF	603	C38	470nF	805			
C41	10µF	1210	C14	330pF	603	CD1	470nF	805		NC: non soldered	
C29	10µF	1210	CI30	330pF	603	C19	470nF	805			

PACKAGE MECHANICAL DATA

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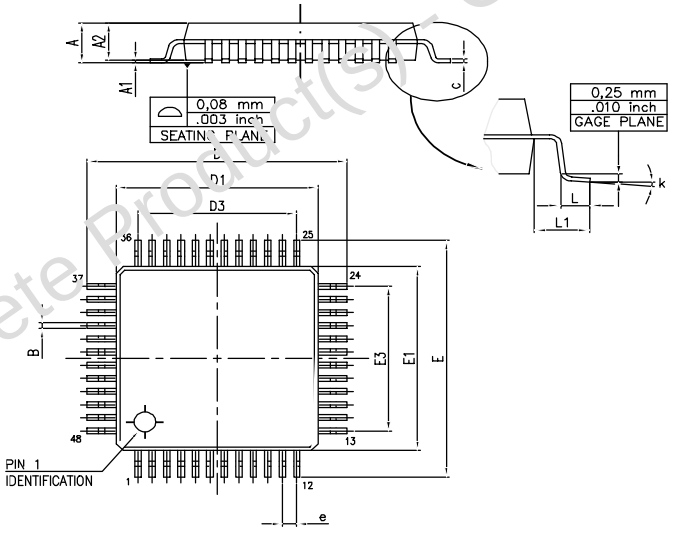

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