TEA1552

HV start-up flyback controller for DCM or QR mode; 125 kHz $f_{osc(h)}$; standby output signal

Rev. 3.1 — 21 June 2012 Product data sheet

1. General description

The GreenChipII is the second generation of green Switched Mode Power Supply (SMPS) control ICs operating directly from the rectified universal mains. A high level of integration leads to a cost effective power supply with a very low number of external components.

The special built-in green functions allow the efficiency to be optimum at all power levels. This holds for quasi-resonant operation at high power levels, as well as fixed frequency operation with valley switching at medium power levels. At low power (standby) levels, the system operates at reduced frequency and with valley detection.

The proprietary high voltage BCD800 process makes direct start-up possible from the rectified mains voltage in an effective and green way. A second low voltage BICMOS IC is used for accurate, high speed protection functions and control.

Highly efficient, reliable supplies can easily be designed using the GreenChipII control IC.

2. Features and benefits

- Distinctive features:
  - Universal mains supply operation (70 V AC to 276 V AC)
  - High level of integration, giving a very low external component count.
- Green features:
  - Valley or zero voltage switching for minimum switching losses
  - Efficient quasi-resonant operation at high power levels
  - Frequency reduction at low power standby for improved system efficiency (<3 W)
  - Cycle skipping mode at very low loads. P_i < 300 mW at no-load operation for a typical adapter application
  - On-chip start-up current source
  - Standby indication pin to indicate low output power consumption.
- Protection features:
  - Safe restart mode for system fault conditions
  - Continuous mode protection by means of demagnetization detection (zero switch-on current)
  - Accurate and adjustable overvoltage protection (latched)
  - Short winding protection
  - Undervoltage protection (foldback during overload)
  - Overtemperature protection (latched)

- Low and adjustable overcurrent protection trip level
- Soft (re)start
- Mains voltage-dependent operation-enabling level
- General purpose input for lock protection.

3. Applications

3.1 Typical application

Typical application areas are adapters and chargers (e.g. for laptops, camcorders and printers) and all applications that demand an efficient and cost-effective solution up to 250 W.

4. Ordering information

Table 1. Ordering information

Type number	Package		
	Name	Description	Version
TEA1552T	SO14	plastic small outline package; 14 leads; body width 3.9 mm	SOT108-1

5. Block diagram

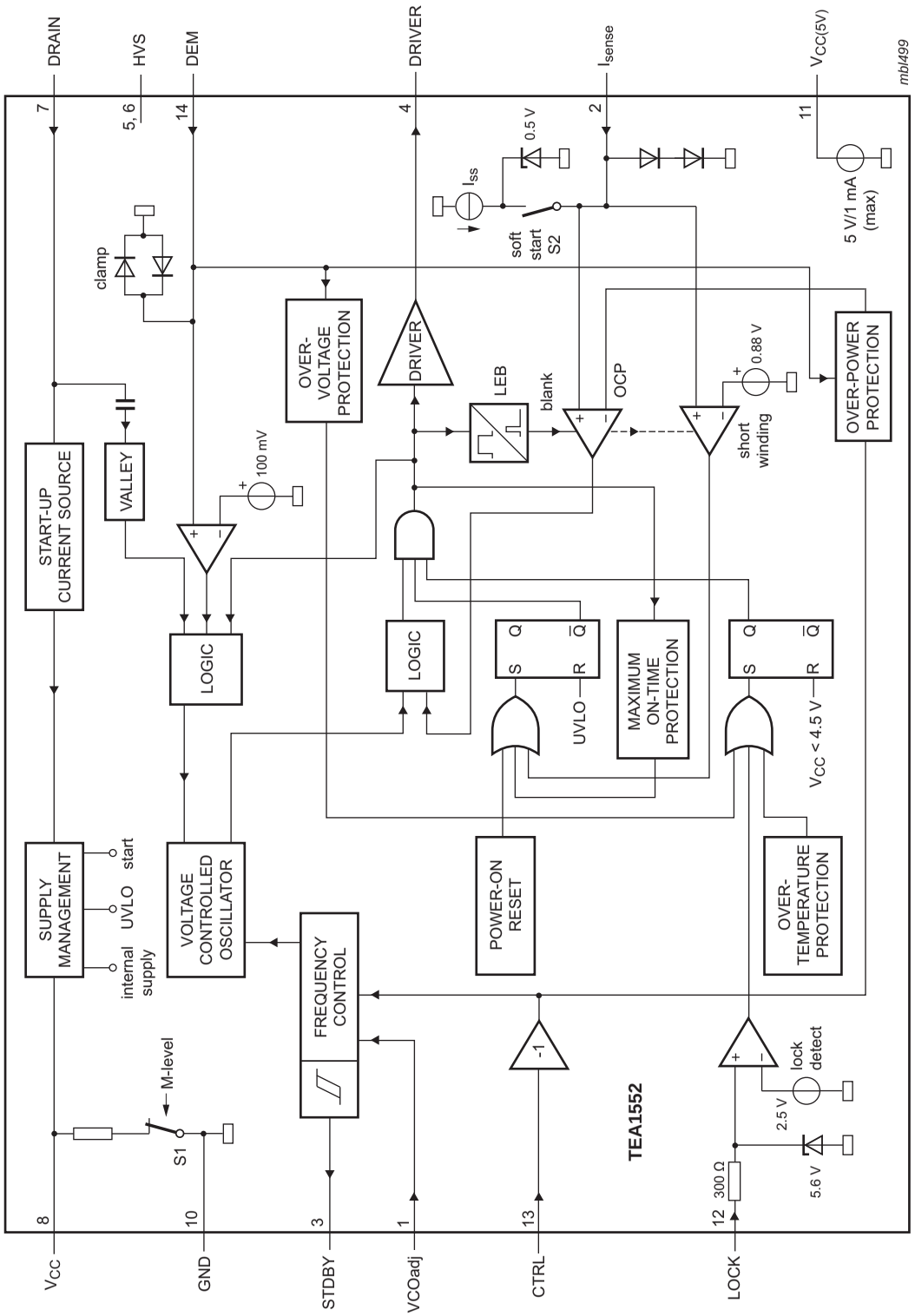


Fig 1. Block diagram

6. Pinning information

6.1 Pinning

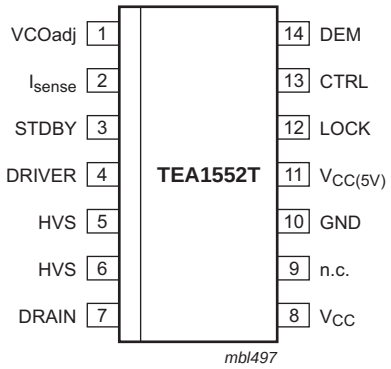


Fig 2. Pin configuration

6.2 Pin description

Table 2. Pin description

Symbol	Pin	Description
VCOadj	1	VCO adjustment input
I_{sense}	2	programmable current sense input
STDBY	3	standby indication or control output
DRIVER	4	gate driver output
HVS	5	high voltage safety spacer, not connected
HVS	6	high voltage safety spacer, not connected
DRAIN	7	drain of external MOS switch, input for start-up current and valley sensing
V_{CC}	8	supply voltage
n.c.	9	not connected
GND	10	ground
$V_{CC(5V)}$	11	5 V output
LOCK	12	lock input
CTRL	13	control input
DEM	14	input from auxiliary winding for demagnetization timing, OVP and OPP

7. Functional description

The TEA1552 is the controller of a compact flyback converter, with the IC situated at the primary side. An auxiliary winding of the transformer provides demagnetization detection and powers the IC after start-up.

The TEA1552 operates in multi modes (see Figure 3).

The next converter stroke is started only after demagnetization of the transformer current (zero current switching), while the drain voltage has reached the lowest voltage to prevent switching losses (green function). The primary resonant circuit of primary inductance and drain capacitor ensures this quasi-resonant operation. The design can be optimized in such a way that zero voltage switching can be reached over almost the complete universal mains range.

To prevent very high frequency operation at lower loads, the quasi-resonant operation changes smoothly in fixed frequency PWM control.

At very low power (standby) levels, the frequency is controlled down, via the VCO, to a minimum frequency of approximately 25 kHz.

7.1 Start-up, mains enabling operation level and undervoltage lock-out (see Figure 11 and 12)

Initially, the IC is self supplying from the rectified mains voltage via pin DRAIN. Supply capacitor C_{VCC} is charged by the internal start-up current source to a level of approximately 4 V or higher, depending on the drain voltage. Once the drain voltage exceeds the M-level (mains-dependent operation-enabling level), the start-up current source will continue charging capacitor C_{VCC} (switch S1 will be opened); see Figure 1. The IC will activate the power converter as soon as the voltage on pin V_{CC} passes the level $V_{CC(start)}$. The IC supply is taken over by the auxiliary winding as soon as the output voltage reaches its intended level and the IC supply from the mains voltage is subsequently stopped for high efficiency operation (green function).

The moment the voltage on pin V_{CC} drops below the undervoltage lock-out level V_{UVLO}, the IC stops switching and enters a safe restart from the rectified mains voltage. Inhibiting the auxiliary supply by external means causes the converter to operate in a stable, well defined burst mode.

7.2 Supply management

All (internal) reference voltages are derived from a temperature compensated, on-chip band gap circuit.

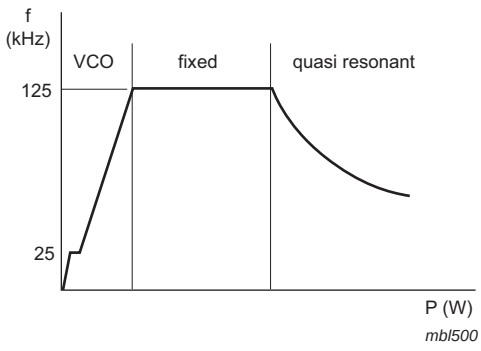


Fig 3. Multi-mode operation

7.3 Current mode control

Current mode control is used for its good line regulation behaviour.

The ‘on-time’ is controlled by the internally inverted control pin voltage, which is compared with the primary current information. The primary current is sensed across an external resistor. The driver output is latched in the logic, preventing multiple switch-on.

The internal control voltage is inversely proportional to the external control pin voltage, with an offset of 1.5 V. This means that a voltage range from 1 V to 1.5 V on pin CTRL will result in an internal control voltage range from 0.5 V to 0 V (a high external control voltage results in a low duty cycle).

7.4 Oscillator

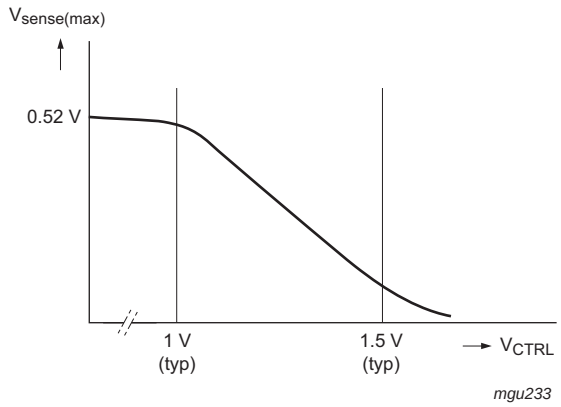


Fig 4. $V_{sense(max)}$ as a function of V_{CTRL}

The maximum fixed frequency of the oscillator is set by an internal current source and capacitor. The maximum frequency is reduced once the control voltage enters the VCO control window. Then, the maximum frequency changes linearly with the control voltage until the minimum frequency is reached (see Figure 4 and 5).

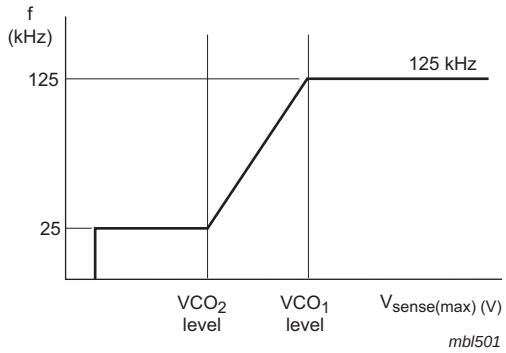


Fig 5. VCO-frequency as a function of $V_{sense(max)}$

7.5 VCO adjustment

The VCOadj pin can be used to set the VCO operation point. As soon as the peak voltage on the sense resistor is controlled below half the voltage on the VCOadj pin (VCO_1 level), frequency reduction will start. The actual peak voltage on sense will be somewhat higher

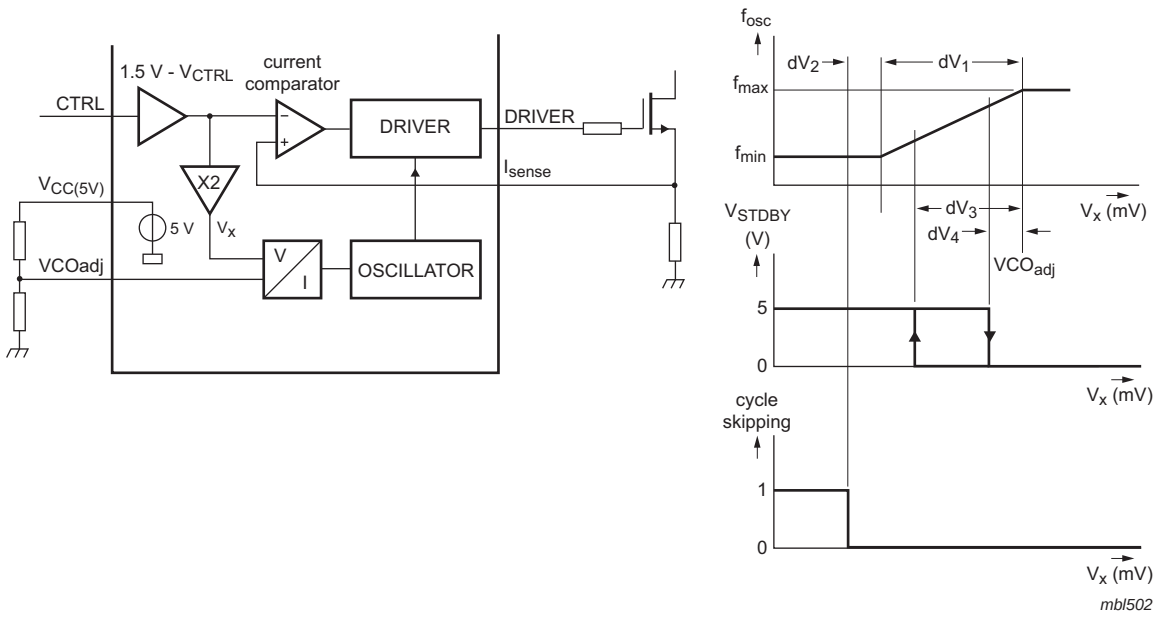
due to switch-off delay (see Figure 6). The frequency reduction will stop approximately 25 mV lower (VCO_2 level), when the minimum frequency is reached.

7.6 Cycle skipping

At very low power levels, a cycle skipping mode will be activated. A high control voltage will reduce the switching frequency to a minimum of 25 kHz. If the voltage on the control pin has raised even more, switch-on of the external power MOSFET will be inhibited until the voltage on the control pin has dropped to a lower value again <.Normal_XRef>(see Fig.6).

For system accuracy, it is not the absolute voltage on the control pin that will trigger the cycle skipping mode, but a signal derived from the internal VCO will be used.

Remark: If the no-load requirement of the system is such that the output voltage can be regulated to its intended level at a switching frequency of 25 kHz or above, the cycle skipping mode will not be activated.



The voltage levels dV_1, dV_2, dV_3 and dV_4 are fixed in the IC to typically 50 mV, 18 mV, 40 mV and 15 mV respectively.

The level at which VCO mode of operation starts or ends can be externally controlled with the VCOadj pin.

Fig 6. A functional implementation of the standby and cycle skipping circuitry.

7.7 Standby output

The STDBY output pin (V_{STDBY} = 5 V) can be used to drive an external NPN transistor or FET in order to e.g. switch-off a PFC circuit. The STDBY output is activated by the internal VCO: as soon as the VCO has reduced the switching frequency to (almost) the minimum frequency of 25 kHz, the STDBY output will be activated (see Figure 6). The STDBY output will go low again as soon as the VCO allows a switching frequency close to the maximum frequency of 125 kHz.

7.8 Demagnetization

The system will be in discontinuous conduction mode all the time. The oscillator will not start a new primary stroke until the secondary stroke has ended.

Demagnetization features a cycle-by-cycle output short-circuit protection by immediately lowering the frequency (longer off-time), thereby reducing the power level.

Demagnetization recognition is suppressed during the first time (t_{suppr}). This suppression may be necessary in applications where the transformer has a large leakage inductance and at low output voltages/start-up.

7.9 OverVoltage Protection (OVP)

An OVP mode is implemented in the GreenChip series. For the TEA1552, this works by sensing the auxiliary voltage via the current flowing into pin DEM during the secondary stroke. The auxiliary winding voltage is a well-defined replica of the output voltage. Any voltage spikes are averaged by an internal filter.

If the output voltage exceeds the OVP trip level, the OVP circuit switches off the power MOSFET. The controller then waits until the UVLO level is reached on pin V_{CC}. When V_{CC} drops to UVLO, capacitor C_{VCC} will be recharged to the V_{start} level, however the IC will not start switching again. Subsequently, V_{CC} will drop again to the UVLO level, etc.

Operation only recommences when the V_{CC} voltage drops below a level of approximately 4.5 V (practically when the V_{mains} has been disconnected for a short period).

The output voltage (V_{OVP}) at which the OVP function trips, can be set by the demagnetization resistor R_{DEM}:

$$V_{OVP} = \frac{N_s}{N_{aux}} \times [I_{OVP(DEM)} \times R_{DEM} + V_{clamp(DEM)(pos)}]$$

where N_s is the number of secondary turns and N_{aux} is the number of auxiliary turns of the transformer.

Current $I_{OVP(DEM)}$ is internally trimmed.

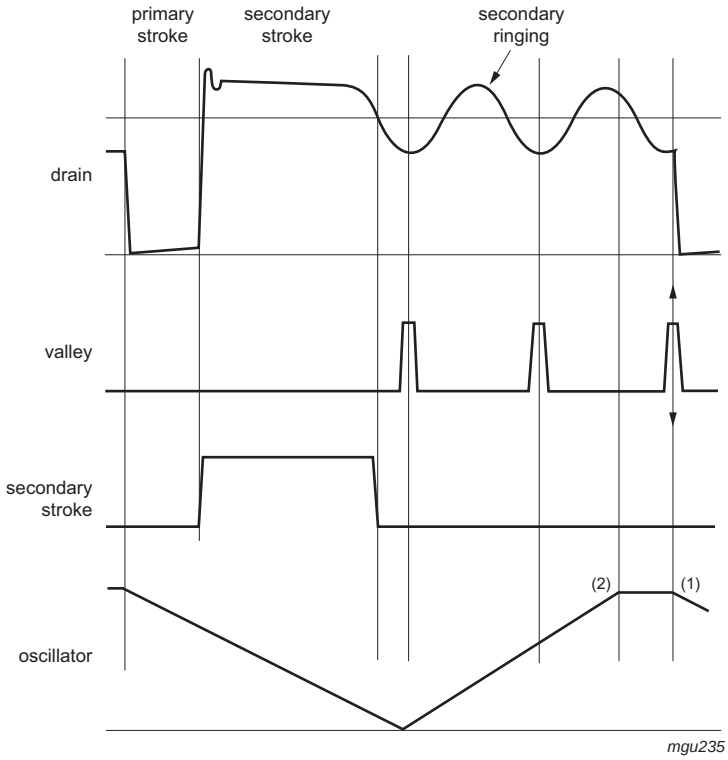
The value of the demagnetization resistor (R_{DEM}) can be adjusted to the turns ratio of the transformer, thus making an accurate OVP possible.

7.10 Valley switching (see Figure 7)

A new cycle starts when the power switch is switched on. After the ‘on-time’ (which is determined by the ‘sense’ voltage and the internal control voltage), the switch is opened and the secondary stroke starts.

After the secondary stroke, the drain voltage shows an oscillation with a frequency of approximately $\frac{1}{(2 \times \pi \times \sqrt{(L_p \times C_d)})}$

where L_p is the primary self inductance of the transformer and C_d is the capacitance on the drain node.



A: Start of new cycle at lowest drain voltage.

B: Start of new cycle in a classical PWM system at high drain voltage.

Fig 7. Signals for valley switching.

As soon as the oscillator voltage is high again and the secondary stroke has ended, the circuit waits for the lowest drain voltage before starting a new primary stroke. This method is called valley detection. Figure 7 shows the drain voltage together with the valley signal, the signal indicating the secondary stroke and the oscillator signal.

In an optimum design, the reflected secondary voltage on the primary side will force the drain voltage to zero. Thus, zero voltage switching is very possible, preventing large capacitive switching losses

$$\left(P = \frac{1}{2} \times C \times V^2 \times f\right)$$

and allowing high frequency operation, which results in small and cost effective inductors.

7.11 OverCurrent Protection (OCP)

The cycle-by-cycle peak drain current limit circuit uses the external source resistor to measure the current accurately. This allows optimum size determination of the transformer core (cost issue). The circuit is activated after the leading edge blanking time t_{leb}. The OCP protection circuit limits the ‘sense’ voltage to an internal level.

7.12 OverPower Protection (OPP)

During the primary stroke, the rectified mains input voltage is measured by sensing the current drawn from pin DEM. This current is dependent on the mains voltage, according to the following formula:

$$I_{DEM} \approx \frac{V_{aux}}{R_{DEM}} \approx \frac{N \times V_{mains}}{R_{DEM}}$$

where:

$$N = \frac{N_{aux}}{N_P}$$

The current information is used to adjust the peak drain current, which is measured via pin I_{sense}. The internal compensation is such that an almost mains independent maximum output power can be realized.

The OPP curve is given in Figure 8.

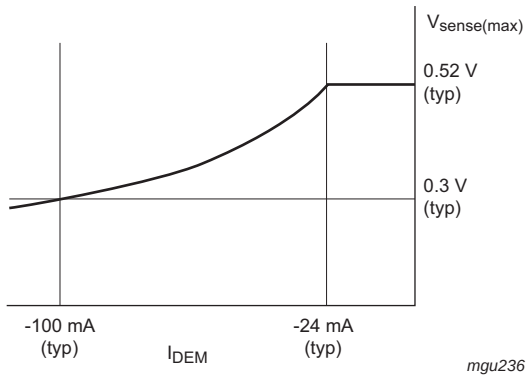


Fig 8. OPP correction curve

7.13 Minimum and maximum 'on-time'

The minimum 'on-time' of the SMPS is determined by the Leading Edge Blanking (LEB) time. The IC limits the 'on-time' to 50 µs. When the system desires an 'on-time' longer than 50 µs, a fault condition is assumed, and the IC will stop switching and enter the safe restart mode.

7.14 Short winding protection

After the leading edge blanking time, the short winding protection circuit is also activated. If the 'sense' voltage exceeds the short winding protection voltage V_{swp}, the converter will stop switching. Once V_{CC} drops below the UVLO level, capacitor C_{VCC} will be recharged and the supply will restart again. This cycle will be repeated until the short-circuit is removed (safe restart mode).

The short winding protection will also protect in case of a secondary diode short-circuit.

7.15 Lock input

Pin LOCK is a general purpose (high-impedance) input pin, which can be used to switch off the IC. As soon as the voltage on this pin is raised above 2.5 V, switching will stop immediately. The voltage on the V_{CC} pin will cycle between $V_{CC(start)}$ and $V_{CC(UVLO)}$, but the IC will not start switching again until the latch function is reset. The latch is reset as soon as the V_{CC} drops below 4.5 V (typical value). The internal OVP and OTP will also trigger this latch Figure 1.

The detection level of this input is related to the $V_{CC(5V)}$ pin voltage in the following way: $0.5 \times V_{CC(5V)} \pm 4\%$. An internal Zener diode clamp of 5.6 V will protect this pin from excessive voltages. No internal filtering is done on this input.

7.16 Overtemperature Protection (OTP)

An accurate temperature protection is provided in the circuit. When the junction temperature exceeds the thermal shutdown temperature, the IC will stop switching. When V_{CC} drops to UVLO, capacitor C_{VCC} will be recharged to the V_{start} level, however the IC will not start switching again. Subsequently, V_{CC} will drop again to the UVLO level, etc.

Operation only recommences when the V_{CC} voltage drops below a level of approximately 4.5 V (practically when the V_{mains} has been disconnected for a short period).

7.17 Soft start-up

To prevent transformer rattle during hiccup, the transformer peak current is slowly increased by the soft start function. This can be achieved by inserting a resistor and a capacitor between pin I_{sense} and the sense resistor (see Figure 9). An internal current source charges the capacitor to $V = I_{SS} \times R_{SS}$, with a maximum of approximately 0.5 V.

The start level and the time constant of the increasing primary current level can be adjusted externally by changing the values of R_{SS} and C_{SS}.

$$I_{primary(max)} = \frac{V_{ocp} - (I_{SS} \times R_{SS})}{R_{sense}}$$

$$\tau = R_{SS} \times C_{SS}$$

The charging current I_{SS} will flow as long as the voltage on pin I_{sense} is below approximately 0.5 V. If the voltage on pin I_{sense} exceeds 0.5 V, the soft start current source will start limiting the current I_{SS}. At the $V_{CC(start)}$ level, the I_{SS} current source is completely switched off.

Since the soft start current I_{SS} is subtracted from pin V_{CC} charging current, the R_{SS} value will affect the V_{CC} charging current level by a maximum of 60 µA (typical value).

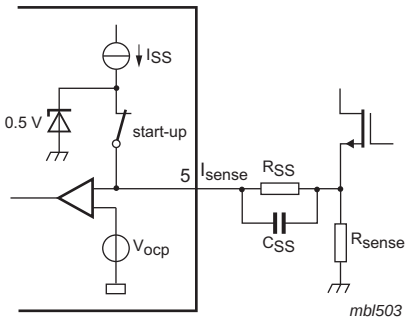


Fig 9. Soft start-up

7.18 5 V output

Pin $V_{CC(5V)}$ can be used for supplying external circuitry. The maximum output current must be limited to 1 mA. If higher peak currents are required, an external RC combination should limit the current drawn from this pin to 1 mA maximum.

The 5 V output voltage will be available as soon as the start-up voltage is reached. As the high voltage supply can not supply the 5 V pin during start-up and/or shutdown, during latched shutdown (via pin LOCK or other latched protection such as OVP or OTP), the voltage is switched to zero.

7.19 Driver

The driver circuit to the gate of the power MOSFET has a current sourcing capability of typically 170 mA and a current sink capability of typically 700 mA. This permits fast turn-on and turn-off of the power MOSFET for efficient operation. A low driver source current has been chosen to limit the $\Delta V/\Delta t$ at switch-on. This reduces Electro Magnetic Interference (EMI) and also limits the current spikes across R_{sense}.

8. Limiting values

Table 3. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).[1]

Symbol	Parameter	Conditions	Min	Max	Unit
Voltages					
V_{VCOadj}	voltage on pin VCOadj	continuous	–0.4	+5	V
V_{sense}	voltage on pin I_{sense}	current limited	–0.4	–	V
V_{DRAIN}	voltage on pin DRAIN		–0.4	+650	V
V_{CC}	supply voltage	continuous	–0.4	+20	V
V_{LOCK}	voltage on pin LOCK	continuous	–0.4	+7	V
V_{CTRL}	voltage on pin CTRL		–0.4	+5	V
V_{DEM}	voltage on pin DEM	current limited	–0.4	–	V
Currents					
I_{sense}	current on pin I_{sense}		–1	+10	mA
I_{STDBY}	current on pin STDBY		–1	-	mA
I_{DRIVER}	current on pin DRIVER	d < 10 %	–0.8	+2	A
I_{DRAIN}	current on pin DRAIN		-	+5	mA
$I_{CC(5V)}$	current on pin $V_{CC(5V)}$		–1	0	mA
I_{CTRL}	current on pin CTRL		-	+5	mA
I_{DEM}	current on pin DEM		–250	+250	µA
General					
P_{tot}	total power dissipation	T_{amb} < 70 °C	-	0.75	W
T_{stg}	storage temperature		–55	+150	°C
T_j	junction temperature		–20	+145	°C
ESD					
V_{esd}	electrostatic discharge voltage				
	pins 1 to 6 and pins 9 to 14	HBM class 1 [2]	-	2000	V
	pin 7	HBM class 1 [2]	-	1500	V
	on any other pin	MM [3]	-	400	V

[1] All voltages are measured with respect to ground; positive currents flow into the chip; pin V_{CC} may not be current driven. The voltage ratings are valid provided other ratings are not violated; current ratings are valid provided the maximum power rating is not violated.

[2] Equivalent to discharging a 100 pF capacitor through a 1.5 kΩ serie resistor.

[3] Equivalent to discharging a 200 pF capacitor through a 0.75 µH coil and a 10 Ω resistor.

9. Thermal characteristics

Table 4. Thermal characteristics

Symbol	Parameter	Conditions		Typ	Unit
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air	[1]	100	K/W

[1] With pin GND connected to sufficient copper area on the printed-circuit board.

10. Characteristics

Table 5. Characteristics

T_{amb} = 25 °C; V_{CC} = 15 V; all voltages are measured with respect to ground; currents are positive when flowing into the IC; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Start-up current source (pin DRAIN)						
I_{DRAIN}	supply current from pin DRAIN	V_{CC} = 0 V; V_{DRAIN} > 100 V	1.0	1.2	1.4	mA
		with auxiliary supply; V_{DRAIN} > 100 V	-	100	300	µA
BV_{DSS}	breakdown voltage		650	-	-	V
M-level	mains-dependent operation-enabling level		60	-	100	V
Supply voltage management (pin V_{CC})						
$V_{CC(start)}$	start-up voltage on V_{CC}		10.3	11	11.7	V
$V_{CC(UVLO)}$	undervoltage lock-out on V_{CC}		8.1	8.7	9.3	V
$V_{CC(hys)}$	hysteresis voltage on V_{CC}	$V_{CC(start)} - V_{CC(UVLO)}$	2.0	2.3	2.6	V
$I_{CC(h)}$	pin V_{CC} charging current (high)	V_{DRAIN} > 100 V; V_{CC} < 3V	–1.2	–1	–0.8	mA
$I_{CC(l)}$	pin V_{CC} charging current (low)	V_{DRAIN} > 100 V; 3 V < V_{CC} < $V_{CC(UVLO)}$	–1.2	–0.75	–0.45	mA
$I_{CC(restart)}$	pin V_{CC} restart current	V_{DRAIN} > 100 V; $V_{CC(UVLO)}$ < V_{CC} < $V_{CC(start)}$	–650	–550	–450	µA
$I_{CC(oper)}$	supply current under normal operation	no load on pin DRIVER	1.1	1.3	1.5	mA
Demagnetization management (pin DEM)						
$V_{th(DEM)}$	demagnetization comparator threshold voltage on pin DEM		50	100	150	mV
$I_{prot(DEM)}$	protection current on pin DEM	V_{DEM} = 50 mV	–50[1]	-	–10	nA
$V_{clamp(DEM)(neg)}$	negative clamp voltage on pin DEM	I_{DEM} = –150 µA	–0.5	–0.25	–0.05	V
$V_{clamp(DEM)(pos)}$	positive clamp voltage on pin DEM	I_{DEM} = 250 µA	0.5	0.7	0.9	V
t_{suppr}	suppression of transformer ringing at start of secondary stroke		1.1	1.5	1.9	µs
Pulse width modulator						
$t_{on(min)}$	minimum on-time		-	t_{leb}	-	ns
$t_{on(max)}$	maximum on-time	latched	40	50	60	µs
Oscillator						
$f_{osc(l)}$	oscillator low fixed frequency	V_{CTRL} > 1.5 V	20	25	30	kHz
$f_{osc(h)}$	oscillator high fixed frequency	V_{CTRL} < 1 V	100	125	150	kHz
$V_{vco(start)}$	peak voltage on pin I_{sense}, where frequency reduction starts	see Figure 5 and Figure 6	-	VCO[1]	–	mV
$V_{vco(max)}$	peak voltage on pin I_{sense}, where the frequency is equal to $f_{osc(l)}$		-	VCO[1] – 25	–	mV

Table 5. Characteristics *…continued*

T_{amb} = 25 °C; V_{CC} = 15 V; all voltages are measured with respect to ground; currents are positive when flowing into the IC; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Duty cycle control (pin CTRL)						
$V_{CTRL(min)}$	minimum voltage on pin CTRL for maximum duty cycle		-	1.0	-	V
$V_{CTRL(max)}$	maximum voltage on pin CTRL for minimum duty cycle		-	1.5	-	V
5 V output (pin $V_{CC(5V)}$)						
$V_{CC(5V)}$	output voltage	I_O = 1 mA	4.75	5.0	5.25	V
$I_{CC(5V)}$	current capability of pin $V_{CC(5V)}$		–1.0	-	-	mA
LOCK input (pin LOCK)						
V_{LOCK}	LOCK trip level		2.37	2.5	2.63	V
$V_{CC(reset)}$	voltage level on pin V_{CC} which resets the latch	V_{LOCK} < 2.3 V	-	4.5	-	V
$REL_{LOCK,5V}$	relation to 5 V output (pin $V_{CC(5V)}$)	$V_{LOCK} = 0.5 \times V_{CC(5V)}$	–4	-	+4	%
Valley switch (pin DRAIN)						
$\Delta V/\Delta t_{valley}$	valley recognition voltage change		–85	-	+85	V/µs
$t_{valley\text{-}swon}$	delay from valley recognition to switch-on		-	150[1]	-	ns
Overcurrent and short winding protection (pin I_{sense})						
$V_{sense(max)}$	maximum source voltage OCP	$\Delta V/\Delta t$ = 0.1 V/µs	0.48	0.52	0.56	V
t_{PD}	propagation delay from detecting $V_{sense(max)}$ to switch-off	$\Delta V/\Delta t$ = 0.5 V/µs	–	140	185	ns
V_{swp}	short winding protection voltage		0.83	0.88	0.96	V
t_{leb}	blanking time for current and short winding protection		300	370	440	ns
I_{SS}	soft start current	V_{sense} < 0.5 V	45	60	75	µA
Overvoltage protection (pin DEM)						
$I_{OVP(DEM)}$	OVP level on pin DEM	set by resistor R_{DEM}; see Section 7.9	54	60	66	µA
Overpower protection (pin DEM)						
$I_{OPP(DEM)}$	OPP current on pin DEM to start OPP correction	set by resistor R_{DEM}; see Section 7.12	–	–24	–	µA
$I_{OPP50\%(DEM)}$	OPP current on pin DEM, where maximum source voltage is limited to 0.3 V		–	–100	–	µA
Standby output (pin STDBY)						
V_{STDBY}	standby output voltage		4.75	5.0	5.25	V
I_{source}	source current capability	V_{STDBY} = 1 V	20	22	24	µA
I_{sink}	sink current capability	V_{STDBY} = 1.2 V	2	-		mA

Table 5. Characteristics *…continued*

T_{amb} = 25 °C; V_{CC} = 15 V; all voltages are measured with respect to ground; currents are positive when flowing into the IC; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Driver (pin Driver)						
I_{source}	source current capability of driver	V_{CC} = 9.5 V; V_{DRIVER} = 2 V	-	–170	–88	mA
I_{sink}	sink current capability of driver	V_{CC} = 9.5 V; V_{DRIVER} = 2 V	-	300	-	mA
		V_{CC} = 9.5 V; V_{DRIVER} = 9.5 V	400	700	-	mA
$V_{o(driver)(max)}$	maximum output voltage of driver	V_{CC} > 12 V	-	11.5	12	V
Temperature protection						
$T_{prot(max)}$	maximum temperature protection level		130	140	150	°C
$T_{prot(hys)}$	hysteresis for the temperature protection level	[1]	-	8	-	°C

[1] Guaranteed by design.

11. Application information

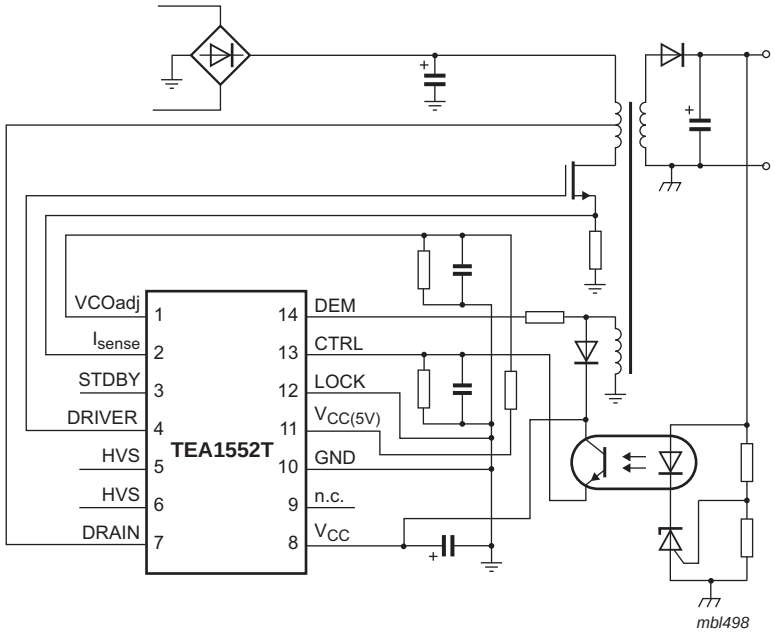
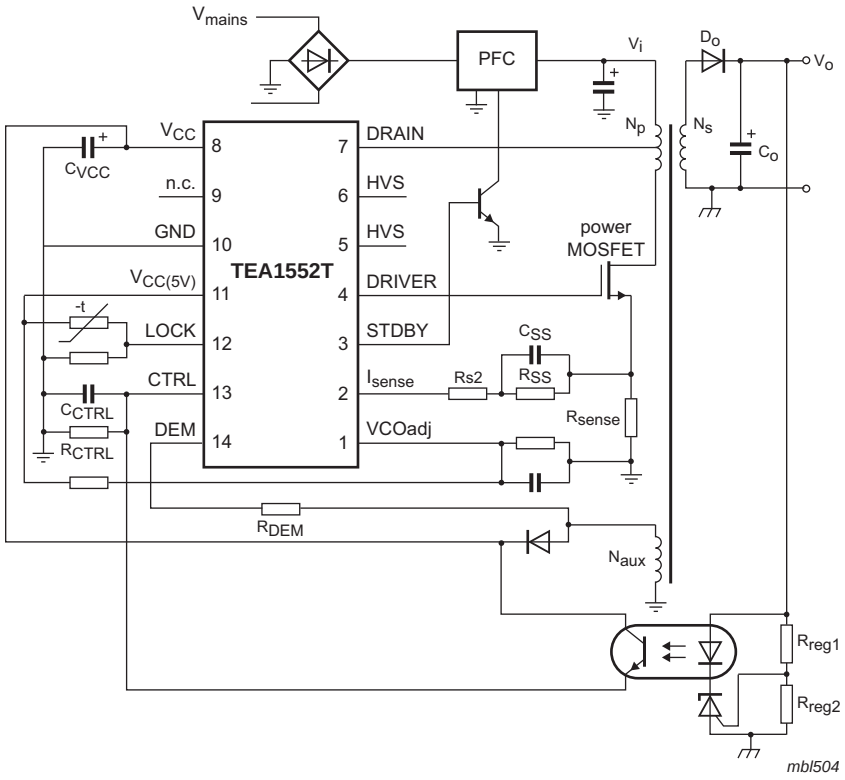


Fig 10. Basic application

A converter with the TEA1552 consists of an input filter, a transformer with a third winding (auxiliary), and an output stage with a feedback circuit.

Capacitor C_{VCC} (at pin V_{CC}) buffers the supply voltage of the IC, which is powered via the high voltage rectified mains during start-up and via the auxiliary winding during operation.

A sense resistor converts the primary current into a voltage at pin I_{sense}. The value of this sense resistor defines the maximum primary peak current.



Pin LOCK is used in this example for an additional external overtemperature protection.

If pin LOCK is not used, it must be tied to ground.

Fig 11. Configuration with controlled PFC.

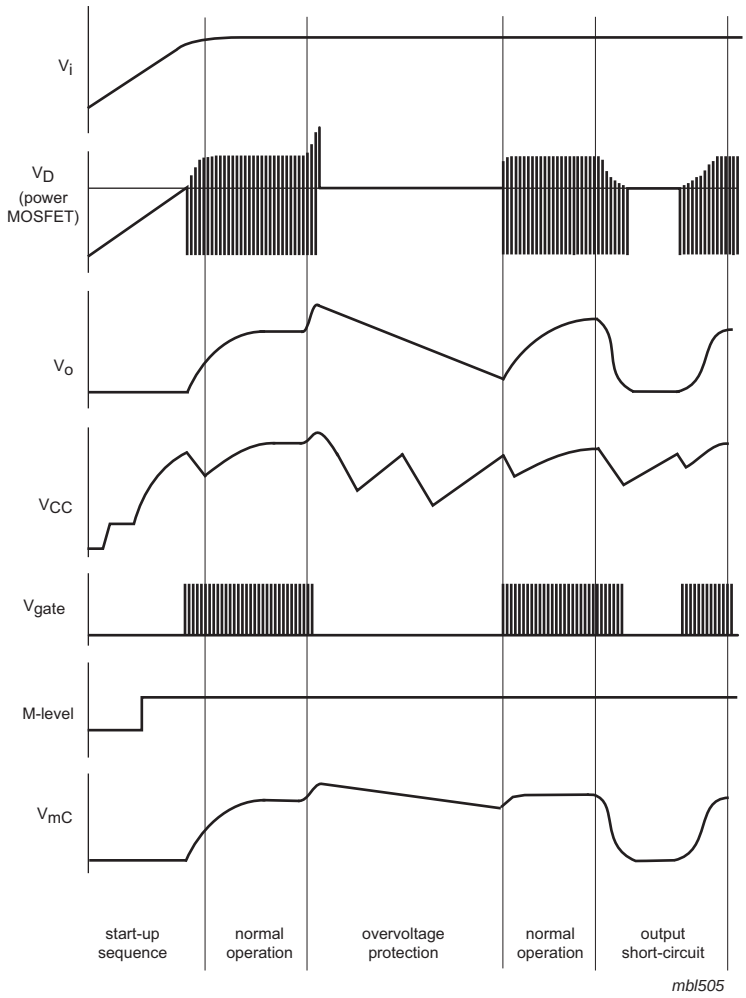
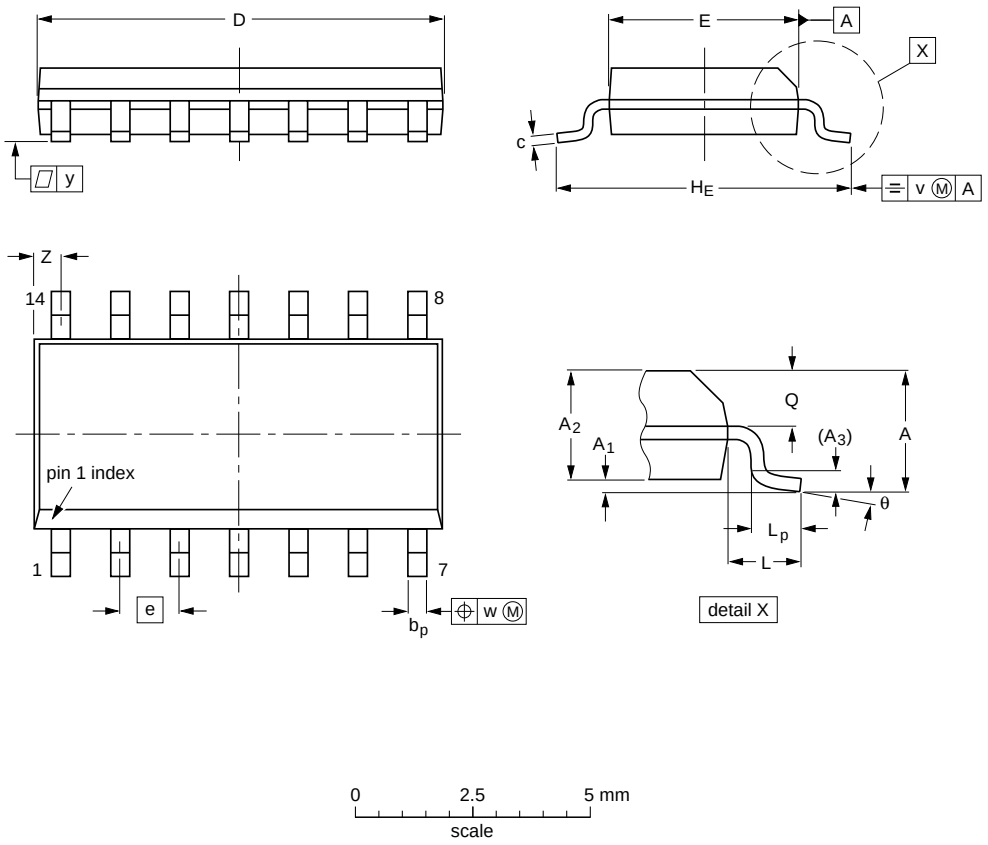


Fig 12. Typical waveforms.

12. Package outline

SO14: plastic small outline package; 14 leads; body width 3.9 mm **SOT108-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	1.75	0.25 0.10	1.45 1.25	0.25	0.49 0.36	0.25 0.19	8.75 8.55	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8^o 0^o
inches	0.069	0.010 0.004	0.057 0.049	0.01	0.019 0.014	0.0100 0.0075	0.35 0.34	0.16 0.15	0.05	0.244 0.228	0.041	0.039 0.016	0.028 0.024	0.01	0.01	0.004	0.028 0.012	

Note

1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT108-1	076E06	MS-012				~~99-12-27~~ 03-02-19

Fig 13. Package outline SOT108-1 (SO14)

13. Soldering of SMD packages

This text provides a very brief insight into a complex technology. A more in-depth account of soldering ICs can be found in Application Note *AN10365 "Surface mount reflow soldering description"*.

13.1 Introduction to soldering

Soldering is one of the most common methods through which packages are attached to Printed Circuit Boards (PCBs), to form electrical circuits. The soldered joint provides both the mechanical and the electrical connection. There is no single soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and Surface Mount Devices (SMDs) are mixed on one printed wiring board; however, it is not suitable for fine pitch SMDs. Reflow soldering is ideal for the small pitches and high densities that come with increased miniaturization.

13.2 Wave and reflow soldering

Wave soldering is a joining technology in which the joints are made by solder coming from a standing wave of liquid solder. The wave soldering process is suitable for the following:

- Through-hole components
- Leaded or leadless SMDs, which are glued to the surface of the printed circuit board

Not all SMDs can be wave soldered. Packages with solder balls, and some leadless packages which have solder lands underneath the body, cannot be wave soldered. Also, leaded SMDs with leads having a pitch smaller than ~0.6 mm cannot be wave soldered, due to an increased probability of bridging.

The reflow soldering process involves applying solder paste to a board, followed by component placement and exposure to a temperature profile. Leaded packages, packages with solder balls, and leadless packages are all reflow solderable.

Key characteristics in both wave and reflow soldering are:

- Board specifications, including the board finish, solder masks and vias
- Package footprints, including solder thieves and orientation
- The moisture sensitivity level of the packages
- Package placement
- Inspection and repair
- Lead-free soldering versus SnPb soldering

13.3 Wave soldering

Key characteristics in wave soldering are:

- Process issues, such as application of adhesive and flux, clinching of leads, board transport, the solder wave parameters, and the time during which components are exposed to the wave
- Solder bath specifications, including temperature and impurities

13.4 Reflow soldering

Key characteristics in reflow soldering are:

- Lead-free versus SnPb soldering; note that a lead-free reflow process usually leads to higher minimum peak temperatures (see Figure 14) than a SnPb process, thus reducing the process window
- Solder paste printing issues including smearing, release, and adjusting the process window for a mix of large and small components on one board
- Reflow temperature profile; this profile includes preheat, reflow (in which the board is heated to the peak temperature) and cooling down. It is imperative that the peak temperature is high enough for the solder to make reliable solder joints (a solder paste characteristic). In addition, the peak temperature must be low enough that the packages and/or boards are not damaged. The peak temperature of the package depends on package thickness and volume and is classified in accordance with Table 6 and 7

Table 6. SnPb eutectic process (from J-STD-020C)

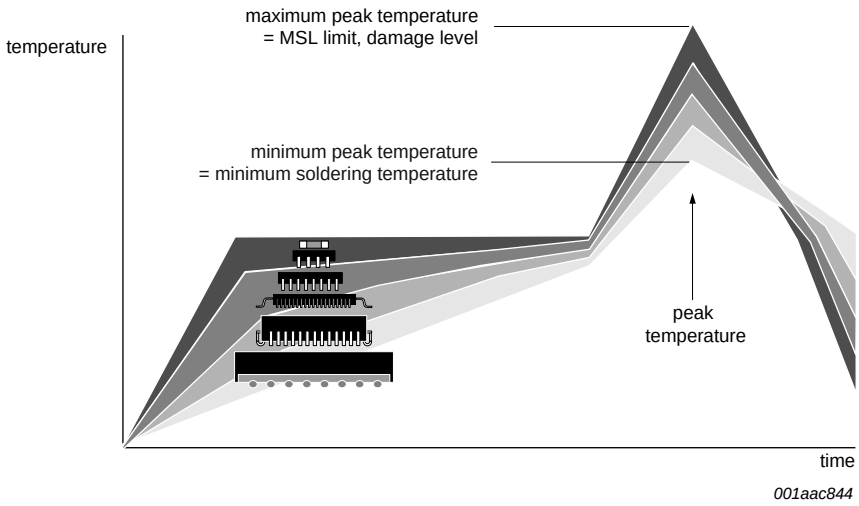
Package thickness (mm)	Package reflow temperature (°C)	
	Volume (mm^3)	
	< 350	≥ 350
< 2.5	235	220
≥ 2.5	220	220

Table 7. Lead-free process (from J-STD-020C)

Package thickness (mm)	Package reflow temperature (°C)		
	Volume (mm^3)		
	< 350	350 to 2000	> 2000
< 1.6	260	260	260
1.6 to 2.5	260	250	245
> 2.5	250	245	245

Moisture sensitivity precautions, as indicated on the packing, must be respected at all times.

Studies have shown that small packages reach higher temperatures during reflow soldering, see Figure 14.



MSL: Moisture Sensitivity Level

Fig 14. Temperature profiles for large and small components

For further information on temperature profiles, refer to Application Note *AN10365 "Surface mount reflow soldering description"*.

14. Abbreviations

Table 8. Abbreviations

Acronym	Description
BiCMOS	Bipolar Complementary Metal-Oxide Semiconductor
DMOS	Diffusion Metal-Oxide Semiconductor
ESR	Equivalent Series Resistance
EZ-HV SOI	Easy High Voltage Silicon-On-Insulator
FET	Field-Effect Transistor
PWM	Pulse Width Modulation
SMPS	Switched Mode Power Supply
SOPS	Self-Oscillating Power Supply

15. Revision history

Table 9. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
TEA1552 v.3.1	20120621	Product data sheet	-	TEA1552 v.3
Modifications:	• Data sheet title changed. • Table 1 "Ordering information" on page 2 updated.			
TEA1552 v.3	20120418	Product data sheet	-	TEA1552 v.2
TEA1552 v.2	20020827	Product specification	-	TEA1552 v.1
TEA1552 v.1	20020703	Product specification	-	-

16. Legal information

16.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

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18. Contents

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