N-Channel Depletion-Mode DMOS FET

Features

- Free from secondary breakdown
- Low power drive requirement
- Ease of paralleling
- Excellent thermal stability
- Integral source-drain diode
- High input impedance and low C_{ISS}
- ESD gate protection

General Description

The LND250 is a high voltage N-channel depletion mode (normally-on) transistor utilizing Supertex's lateral DMOS technology. The gate is ESD protected.

The LND250 is ideal for high voltage applications in the areas of normally-on switches, precision constant current sources, voltage ramp generation and amplification.

Applications

- Solid state relays
- Normally-on switches
- Converters
- Power supply circuits
- Constant current sources
- Input protection circuits

Ordering Information

Part Number	Package Options	Packing
LND250K1-G*	TO-236AB (SOT-23)	3000/Reel

-G denotes a lead (Pb)-free / RoHS compliant package

** Part is not recommended for new designs. Please refer to LND150K1-G.*

Product Summary

BV_{DSX}/BV_{DGX} (V)	$R_{DS(ON)}$ (max)	I_{DSS} (min)
500	1.0kΩ	1.0mA

Absolute Maximum Ratings

Parameter	Value
Drain-to-source	BV_{DSX}
Drain-to-gate	BV_{DGX}
Gate-to-source	±20V
Operating and storage temperature	-55°C to +150°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied. Continuous operation of the device at the absolute rating level may affect device reliability. All voltages are referenced to device ground.

Pin Configuration

TO-236AB (SOT-23)

Product Marking

W = Code for Week Sealed
_____ = "Green" Packaging

TO-236AB (SOT-23)

Packages may or may not include the following marks: Si or

Thermal Characteristics

Package	I_D (continuous)† (mA)	I_D (pulsed) (mA)	Power Dissipation @T_A = 25°C (W)	θ_{ja} (°C/W)	I_{DR} (mA)	I_{DRM}† (mA)
TO-236AB (SOT-23)	13	30	0.36	203	13	30

Notes:

† I_D *(continuous) is limited by max rated* T_j.

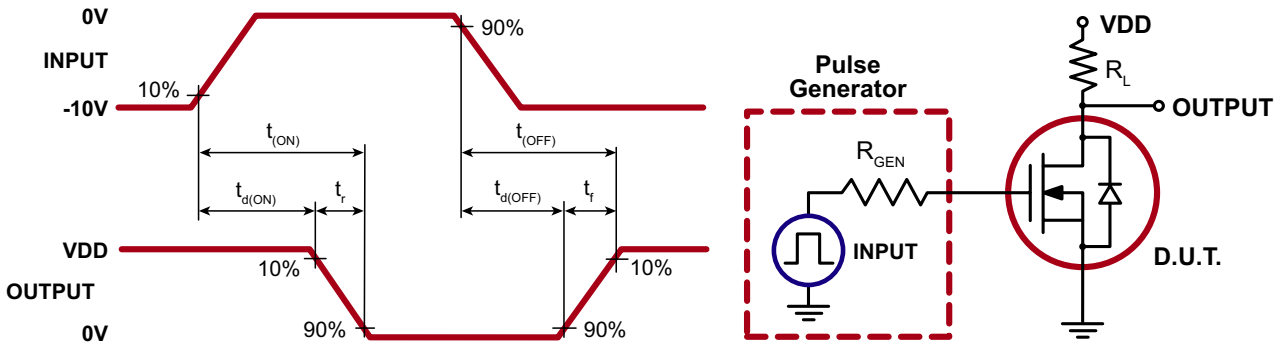
Electrical Characteristics (T_A = 25°C unless otherwise specified)

Sym	Parameter	Min	Typ	Max	Units	Conditions
BV_{DSX}	Drain-to-source breakdown voltage	500	-	-	V	V_{GS} = -10V, I_D = 1.0mA
$V_{GS(OFF)}$	Gate-to-source off voltage	-1.0	-	-3.0	V	V_{GS} = 25V, I_D = 100nA
$\Delta V_{GS(OFF)}$	Change in $V_{GS(OFF)}$ with temperature	-	-	5.0	mV/°C	V_{GS} = 25V, I_D = 100nA
I_{GSS}	Gate body leakage current	-	-	100	nA	V_{GS} = ± 20V, V_{DS} = 0V
$I_{D(OFF)}$	Drain-to-source leakage current	-	-	100	nA	V_{GS} = -10V, V_{DS} = 450V
		-	-	100	µA	V_{DS} = 0.8V Max Rating, V_{GS} = -10V, T_A = 125°C
I_{DSS}	Saturated drain-to-source current	1.0	-	3.0	mA	V_{GS} = 0V, V_{DS} = 25V
$R_{DS(ON)}$	Static drain-to-source on-state resistance	-	850	1000	Ω	V_{GS} = 0V, I_D = 0.5mA
$\Delta R_{DS(ON)}$	Change in $R_{DS(ON)}$ with temperature	-	-	1.2	%/°C	V_{GS} = 0V, I_D = 0.5mA
G_{FS}	Forward transductance	1.0	2.0	-	mmho	V_{DS} = 0V, I_D = 1.0mA
C_{ISS}	Input capacitance	-	7.5	10	pF	V_{GS} = -10V, V_{DS} = 25V, f = 1.0MHz
C_{OSS}	Common source output capacitance	-	2.0	3.5		
C_{RSS}	Reverse transfer capacitance	-	0.5	1.0		
$t_{d(ON)}$	Turn-on delay time	-	0.09	-	µs	V_{DD} = 25V, I_D = 1.0mA, R_{GEN} = 25Ω
t_r	Rise time	-	0.45	-		
$t_{d(OFF)}$	Turn-off delay time	-	0.1	-		
t_f	Fall time	-	1.3	-		
V_{SD}	Diode forward voltage drop	-	-	0.9	V	V_{GS} = -10V, I_{SD} = 1.0mA
t_{rr}	Reverse recovery time	-	200	-	ns	V_{GS} = -10V, I_{SD} = 1.0mA

Notes:

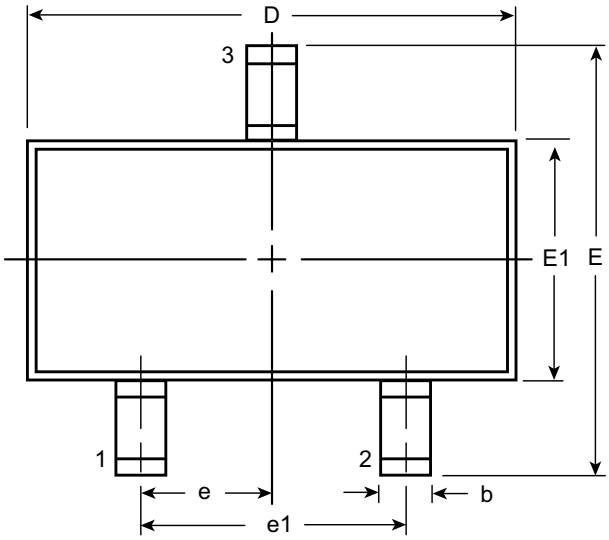
1. *All D.C. parameters 100% tested at 25°C unless otherwise stated. (Pulse test: 300µs pulse, 2% duty cycle.)*
2. *All A.C. parameters sample tested.*

Switching Waveforms and Test Circuit

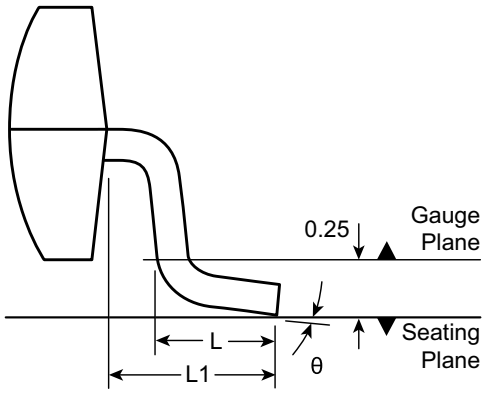


3-Lead TO-236AB (SOT-23) Package Outline (K1)

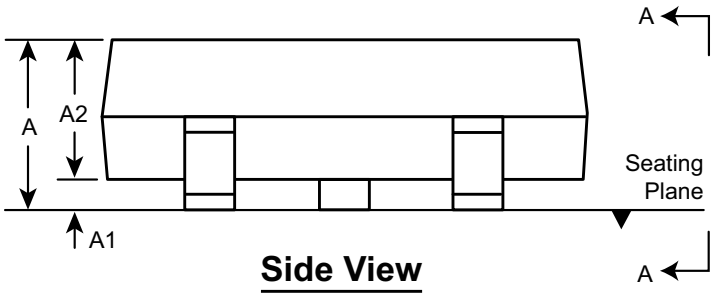
2.90x1.30mm body, 1.12mm height (max), 1.90mm pitch



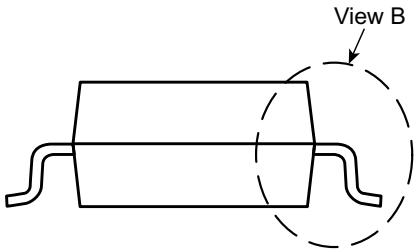
Top View



View B



Side View



View A - A

Symbol		A	A1	A2	b	D	E	E1	e	e1	L	L1	θ
Dimension (mm)	MIN	0.89	0.01	0.88	0.30	2.80	2.10	1.20	0.95 BSC	1.90 BSC	0.20†	0.54 REF	0°
	NOM	-	-	0.95	-	2.90	-	1.30			0.50		-
	MAX	1.12	0.10	1.02	0.50	3.04	2.64	1.40			0.60		8°

JEDEC Registration TO-236, Variation AB, Issue H, Jan. 1999.
† This dimension differs from the JEDEC drawing.
Drawings not to scale.
Supertex Doc.#: *DSPD-3TO236ABK1, Version C041309.*

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to http://www.supertex.com/packaging.html.)

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