PIC18F2455/2550/4455/4550 Rev. A3 Silicon Errata

The PIC18F2455/2550/4455/4550 parts you have received conform functionally to the Device Data Sheet (DS39632**D**), except for the anomalies described below. Any Data Sheet Clarification issues related to the PIC18F2455/2550/4455/4550 will be reported in a separate Data Sheet errata. Please check the Microchip web site for any existing issues.

The following silicon errata apply only to PIC18F2455/2550/4455/4550 devices with these Device/Revision IDs:

Part Number	Device ID	Revision ID
PIC18F2455	0001 0010 011	0 0010
PIC18F2550	0001 0010 010	0 0010
PIC18F4455	0001 0010 001	0 0010
PIC18F4550	0001 0010 000	0 0010

The Device IDs (DEVID1 and DEVID2) are located at addresses 3FFFFEh:3FFFFFh in the device's configuration space. They are shown in binary in the format "DEVID2 DEVID1".

1. Module: EUSART

When performing back-to-back transmission in 9-bit mode (TX9D bit in the TXSTA register is set), an ongoing transmission's timing can be corrupted if the TX9D bit (for the next transmission) is not written immediately following the setting of TXIF. This is because any write to the TXSTA register results in a reset of the Baud Rate Generator which will effect any ongoing transmission.

Work around

Load TX9D just after TXIF is set, either by polling TXIF or by writing TX9D at the beginning of the Interrupt Service Routine, or only write to TX9D when a transmission is not in progress (TRMT = 1).

Date Codes that pertain to this issue:

All engineering and production devices.

2. Module: Timer1/Timer3

When Timer1/Timer3 is operating in 16-bit mode and the prescale setting is not 1:1, a write to the TMR1H/TMR3H Buffer registers may lengthen the duration of the period between the increments of the timer for the period in which TMR1H/TMR3H were written.

Work around

Two work arounds are available: 1) Stop Timer1/Timer3 before writing the TMR1H/TMR3H registers; 2) Write TMR1L/TMR3L immediately after writing TMR1H/TMR3H.

Date Codes that pertain to this issue:

All engineering and production devices.

3. Module: MSSP

In Slave Transmit mode, when a transmission is initiated, the SSPBUF register may be written for up to 10 TCY before additional writes are blocked. The data transfer may be corrupted if SSPBUF is written during this time.

The WCOL bit is set any time an SSPBUF write occurs during a transfer.

Work around

Avoid writing SSPBUF until the data transfer is complete, indicated by the setting of the SSPIF bit (PIR1<3>).

Verify the WCOL bit (SSPCON1<7>) is clear after writing SSPBUF to ensure any potential transfer in progress is not corrupted.

Date Codes that pertain to this issue:

All engineering and production devices.

4. Module: Interrupts

If an interrupt occurs during a two-cycle instruction that modifies the STATUS, BSR or WREG register, the unmodified value of the register will be saved to the corresponding Fast Return (Shadow) register and upon a fast return from the interrupt, the unmodified value will be restored to the STATUS, BSR or WREG register.

For example, if a high priority interrupt occurs during the instruction, `MOVFF TEMP, WREG`, the `MOVFF` instruction will be completed and WREG will be loaded with the value of `TEMP` before branching to ISR. However, the previous value of WREG will be saved to the Fast Return register during ISR branching. Upon return from the interrupt with a fast return, the previous value of WREG in the Fast Return register will be written to WREG. This results in WREG containing the value it had before execution of `MOVFF TEMP, WREG`.

Affected instructions are:

`MOVFF Fs, Fd`
where `Fd` is WREG, BSR or STATUS;

`MOVSF Zs, Fd`
where `Fd` is WREG, BSR or STATUS; and

`MOVSS [Zs], [Zd]`
where the destination is WREG, BSR or STATUS.

Work around

1. Assembly Language Programming:

a) If any two-cycle instruction is used to modify the WREG, BSR or STATUS register, do not use the `RETFIE FAST` instruction to return from the interrupt. Instead, save/restore WREG, BSR and STATUS via software per Example 9-1 in the Device Data Sheet. Alternatively, in the case of `MOVFF`, use the `MOVF` instruction to write to WREG instead. For example, use:

```
MOVF   TEMP, W
MOVWF  BSR
```

instead of: `MOVFF TEMP, BSR`.

b) As another alternative, the following work around shown in Example 1 can be used. This example overwrites the Fast Return register by making a dummy call to `Foo` with the fast option in the high priority service routine.

Date Codes that pertain to this issue:

All engineering and production devices.

EXAMPLE 1:

```
ISR @ 0x0008
  CALL Foo, FAST; store current value of WREG, BSR, STATUS for a second time
Foo:
  POP         ; clears return address of Foo call
  :           ; insert high priority ISR code here
  :
  RETFIEFAST
```

2. C Language Programming: The exact work around depends on the compiler in use. Please refer to your C compiler documentation for details.

   If using the Microchip MPLAB® C18 C Compiler, define both high and low priority interrupt handler functions as “low priority” by using the `pragma interruptlow` directive. This directive instructs the compiler to not use the `RETFIE FAST` instruction. If the proper high priority interrupt bit is set in the IPRx register, then the interrupt is treated as high priority in spite of the `pragma interruptlow` directive.

   The code segment shown in Example 2 demonstrates the work around using the C18 compiler:

EXAMPLE 2:

```
#pragma interruptlow MyLowISR
void MyLowISR(void)
{
   // Handle low priority interrupts.
}

// Although MyHighISR is a high priority interrupt, use interruptlow pragma so that
// the compiler will not use retfie FAST.

#pragma interruptlow MyHighISR
void MyHighISR(void)
{
   // Handle high priority interrupts.
}

#pragma code highVector=0x08
void HighVector (void)
{
   _asm goto MyHighISR _endasm
}
#pragma code /* return to default code section */

#pragma code lowVector=0x18
void LowVector (void)
{
   _asm goto MyLowISR _endasm
}
#pragma code /* return to default code section */
```

An optimized C18 version is also provided in Example 3. This example illustrates how it reduces the instruction cycle count from 10 cycles to 3:

EXAMPLE 3:

```
#pragma code high_vector_section=0x8
void high_vector (void)
{
  _asm
    CALL high_vector_branch, 1
  _endasm
}

void high_vector_branch (void)
{
  _asm
    POP
    GOTO high_isr
  _endasm
}

#pragma interrupt high_isr
void high_isr (void)
{
  ...
}
```

5. Module: ECCP

When monitoring a shutdown condition using a bit test on the ECCPASE bit (ECCP1AS<7>), or performing a bit operation on the ECCPASE bit, the device may produce unexpected results.

Work around

Before performing a bit test or bit operation on the ECCPASE bit, copy the ECCP1AS register to the working register and perform the operation there.

By avoiding these operations on the ECCPASE bit in the ECCP1AS register, the module will operate normally.

In Example 4, ECCPASE bit operations are performed on the W register.

EXAMPLE 4:

```
MOVF    ECCP1AS, W
BTFSC   WREG, ECCPASE
BRA     SHUTDOWN_ROUTINE
```

Date Codes that pertain to this issue:

All engineering and production devices.

6. Module: ECCP

When the CCP1 auto-shutdown feature is configured for automatic restart by setting the PRSEN bit (ECCP1DEL<7>), the pulse terminates immediately in a shutdown event. In addition, the pulse may restart within the period if the shutdown condition expires. This may result in the generation of short pulses on the PWM output(s).

Work around

Configure the auto-shutdown for software restart by clearing the PRSEN bit (ECCP1DEL<7>). The PWM can be re-enabled by clearing the ECCPASE bit (ECCP1AS<7>) after the shutdown condition expires.

Date Codes that pertain to this issue:

All engineering and production devices.

7. Module: ECCP

When operating either Timer1 or Timer3 as a counter with a prescale value other than 1:1 and operating the ECCP in Compare mode with the Special Event Trigger (CCP1CON bits, CCP1M3:CCP1M0 = 1011), the Special Event Trigger Reset of the timer occurs as soon as there is a match between TMRxH:TMRxL and CCPR1H:CCPR1L.

This differs from the PIC18F452, where the Special Event Trigger Reset of the timer occurs on the next rollover of the prescale counter after the match between TMRxH:TMRxL and CCPR1H:CCPR1L.

Work around

To achieve the same timer Reset period on the PIC18F4550 family as the PIC18F452 family for a given clock source, add 1 to the value in CCPR1H:CCPR1L. In other words, if CCPR1H:CCPR1L = x for the PIC18F452, to achieve the same Reset period on the PIC18F4550 family, CCPR1H:CCPR1L = x + 1, where the prescale is 1, 2, 4 or 8 depending on the T1CKPS1:T1CKPS0 bit values.

Date Codes that pertain to this issue:

All engineering and production devices.

8. Module: A/D

The A/D offset is greater than the specified limit in Table 28-28 of the Device Data Sheet. The updated conditions and limits are shown in **bold** text in Table 1.

Work around

Three work arounds exist.

1. Configure the A/D to use the VREF+ and VREF- pins for the voltage references. This is done by setting the VCFG<1:0> bits (ADCON1<5:4>).
2. Perform a conversion on a known voltage reference voltage and adjust the A/D result in software.
3. Increase system clock speed to 48 MHz and adjust A/D settings accordingly. Higher system clock frequencies decrease offset error.

Date Codes that pertain to this issue:

All engineering and production devices.

TABLE 1: A/D CONVERTER CHARACTERISTICS: PIC18F2455/2550/4455/4550 (INDUSTRIAL) PIC18LF2455/2550/4455/4550 (INDUSTRIAL)

Param No.	Symbol	Characteristic	Min	Typ	Max	Units	Conditions
A06A	**EOFF**	**Offset Error**	**—**	**—**	**<±2.0**	**LSb**	**VREF = VREF+ and VREF-**
A06	EOFF	Offset Error	—	—	**<±3.5**	LSb	**VREF = VSS and VDD**

9. Module: DC Characteristics (BOR)

The values for parameter D005 (VBOR) in **Section 28.1 "DC Characteristics"** of the Device Data Sheet, when the trip point for BORV1:BORV0 = 11, are not applicable as the device may reset below the minimum operating voltage for the device.

Work around

None.

Date Codes that pertain to this issue:

All engineering and production devices.

10. Module: USB

When an IN endpoint is owned by USB SIE and the UCON register PKTDIS bit is set, if a USB NAK event occurs on the IN endpoint before the PKTDIS bit is clear, then after the PKTDIS is clear, the pending IN endpoint will send out more bytes than expected. For example, if configured to send out 8 bytes, the SIE would actually send out 12 bytes of data.

Work around

The PKTDIS bit is set when a USB control transfer setup packet is received. Clear this bit as soon as possible, and clear it before turning over any IN endpoint ownership to the SIE.

In the distributed C18 version of the USB library, the following change should be made:

File: `usbctrltrf.c`, version 1.0, dated 11/19/04

Function:
`void USBCtrlEPServiceComplete(void)`

Required Modification:

Move `UCONbits.PKTDIS = 0`, which is located at the end of the function, to the start of the function instead.

Date Codes that pertain to this issue:

All engineering and production devices.

11. Module: PORTD

Each of the PORTD pins has a weak internal pull-up. A single control bit, RDPU (PORTE<7>), can turn on all the pull-ups. After the pull-up has been enabled (PORTE<7> = 1), any access to the PORTE register would cause the RDPU control bit to clear, except those that write a '1' to PORTE<7>.

Work around

Reassert RDPU after each and every access to the PORTE register, except those that write a '1' to PORTE<7>, or use external pull-ups.

Date Codes that pertain to this issue:

All engineering and production devices.

12. Module: Module: MSSP

The I^2C™ slave address masking feature is not supported, therefore, SSPCON2 register bits, ADMSK<5:1>, do not exist in I^2C Slave mode.

Work around

None.

Date Codes that pertain to this issue:

All engineering and production devices.

13. Module: EUSART

In the BAUDCON register, bits RXDTP and TXCKP do not exist. BAUDCON bit 4 is defined instead as SCKP and has the following definition:

bit 4 **SCKP**: Synchronous Clock Polarity Select bit
Asynchronous mode:
Unused in this mode.
Synchronous mode:
1 = Idle state for clock (CK) is a high level
0 = Idle state for clock (CK) is a low level

Work around

None.

Date Codes that pertain to this issue:

All engineering and production devices.

14. Module: USB

The Ping-Pong Buffer mode in which the ping-pong buffers are enabled for Endpoints 1 to 15 (UCFG<PPB1:PPB0> = 11) is not supported.

Work around

Use other Ping-Pong Buffer modes.

Date Codes that pertain to this issue:

All engineering and production devices.

15. Module: MSSP

The MSSP configured in SPI Slave mode will generate a write collision if SSPBUF is updated and the previous SSPBUF contents have not been transferred to the shift register.

Re-initializing the MSSP by clearing and setting the SSPEN (SSPCON1<5>) bit prior to rewriting SSPBUF will not prevent the error condition.

Work around

Prior to updating the SSPBUF register with a new value, verify whether the previous contents were transferred by reading the BF (SSPSTAT<0>) bit. If the previous byte has not been transferred, update SSPBUF and clear the WCOL (SSPCON1<7>) bit if necessary.

Date Codes that pertain to this issue:

All engineering and production devices.

16. Module: MSSP

In SPI mode, the SDO output may change after the inactive clock edge of the bit '0' output. This may affect some SPI components that read data over 300 ns after the inactive edge of SCK.

Work around

None

Date Codes that pertain to this issue:

All engineering and production devices.

17. Module: MSSP

It has been observed that following a Power-on Reset, I^2C mode may not initialize properly by just configuring the SCL and SDA pins as either inputs or outputs. This has only been seen in a few unique system environments.

A test of a statistically significant sample of pre-production systems, across the voltage and current range of the application's power supply, should indicate if a system is susceptible to this issue.

Work around

Before configuring the module for I^2C operation:

1. Configure the SCL and SDA pins as outputs by clearing their corresponding TRIS bits.
2. Force SCL and SDA low by clearing the corresponding LAT bits.
3. While keeping the LAT bits clear, configure SCL and SDA as inputs by setting their TRIS bits.

Once this is done, use the SSPCON1 and SSPCON2 registers to configure the proper I^2C mode as before.

Date Codes that pertain to this issue:

All engineering and production devices.

18. Module: MSSP

When the MSSP is configured for SPI mode, the Buffer Full bit, BF (SSPSTAT<0>), should not be polled in software to determine when the transfer is complete.

Work around

Copy the SSPSTAT register into a variable and perform the bit test on the variable. In Example 5, SSPSTAT is copied into the working register where the bit test is performed.

EXAMPLE 5:

```
loop_MSB:
   MOVF   SSPSTAT, W
   BTFSS  WREG, BF
   BRA    loop_MSB
```

A second option is to poll the Master Synchronous Serial Port Interrupt Flag bit, SSPIF (PIR1<3>). This bit can be polled and will set when the transfer is complete.

Date Codes that pertain to this issue:

All engineering and production devices.

19. Module: EUSART

In rare situations, one or more extra zero bytes have been observed in a packet transmitted by the module operating in Asynchronous mode. The actual data is not lost or corrupted; only unwanted (extra) zero bytes are observed in the packet.

This situation has only been observed when the contents of the transmit buffer, TXREG, are transferred to the TSR during the transmission of a Stop bit. For this to occur, three things must happen in the same instruction cycle:

- TXREG is written to;
- the baud rate counter overflows (at the end of the bit period); and
- a Stop bit is being transmitted (shifted out of TSR).

Work around

If possible, do not use the module's double-buffer capability. Instead, load the TXREG register when the TRMT bit (TXSTA<1>) is set, indicating the TSR is empty.

If double-buffering is used and back-to-back transmission is performed, then load TXREG immediately after TXIF is set, or wait 1-bit time after TXIF is set. Both solutions prevent writing TXREG while a Stop bit is transmitted. Note that TXIF is set at the beginning of the Stop bit transmission.

If transmission is intermittent, then do the following:

- Wait for the TRMT bit to be set before loading TXREG.
- Alternatively, use a free timer resource to time the baud period. Set up the timer to overflow at the end of Stop bit, then start the timer when you load the TXREG. Do not load the TXREG when timer is about to overflow.

Date Codes that pertain to this issue:

All engineering and production devices.

20. Module: EUSART

In 9-Bit Asynchronous Full-Duplex Receive mode, the received data may be corrupted if the TX9D bit (TXSTA<0>) is not modified immediately after the RCIDL bit (BAUDCON<6>) is set.

Work around

Write to TX9D only when a reception is not in progress (RCIDL = 1). Since there is no interrupt associated with RCIDL, it must be polled in software to determine when TX9D can be updated.

Date Codes that pertain to this issue:

All engineering and production devices.

21. Module: EUSART

After the last received byte has been read from the EUSART receive buffer, RCREG, the value is no longer valid for subsequent read operations.

Work around

The RCREG register should only be read once for each byte received. After each byte is received from the EUSART, store the byte into a user variable. To determine when a byte is available to read from RCREG, poll the RCIDL bit (BAUDCON<6>) for a low-to-high transition, or use the EUSART Receive Interrupt Flag, RCIF (PIR1<5>).

Date Codes that pertain to this issue:

All engineering and production devices.

22. Module: EUSART

With the auto-wake-up option enabled by setting the WUE bit (BAUDCON<1>), the RCIF (PIR1<5>) bit will become set on a high-to-low transition on the RX pin. However, the WUE bit may not clear within 1 TCY of a low-to-high transition on RX. While the WUE bit is set, reading the receive buffer, RCREG, will not clear the RCIF interrupt flag. Therefore, the first opportunity to automatically clear RCIF by reading RCREG may take longer than expected.

Note:	RCIF can only be cleared by reading RCREG.

Work around

There are two workarounds available:

1. Clear the WUE bit in software, after the wake-up event has occurred, prior to reading the receive buffer, RCREG.
2. Poll the WUE bit and read RCREG after the WUE bit is automatically cleared.

Date Codes that pertain to this issue:

All engineering and production devices.

23. Module: Timer1

In 16-Bit Asynchronous Counter mode (with or without use of the Timer1 oscillator), the TMR1H and TMR3H buffers do not update when TMRxL is read.

This issue only affects reading the TMRxH registers. The timers increment and set the interrupt flags as expected. The timer registers can also be written as expected.

Work around

1. Use 8-bit mode by clearing the RD16 bit (T1CON<7>).
2. Use the internal clock synchronization option by clearing the $\overline{\text{T1SYNC}}$ bit (T1CON<2>).

Date Codes that pertain to this issue:

All engineering and production devices.

24. Module: Reset

This version of silicon does not support the functionality described in Note 1 of parameter D002 in **Section 28.1 "DC Characteristics: Supply Voltage"** of the data sheet. The RAM content may be altered during a Reset event if the following conditions are met.

- Device is accessing RAM.
- Asynchronous Reset (i.e., WDT, BOR or $\overline{\text{MCLR}}$) occurs when a write operation is being executed (start of a Q4 cycle) or if a RESET instruction is executed and immediately followed by a RETURN instruction.

Work around

None

Date Codes that pertain to this issue:

All engineering and production devices.

25. Module: ECCP (PWM Mode)

When configured for half-bridge operation with dead band (CCPxCON<7:6> = 10), the PWM output may be corrupted for certain values of the PWM duty cycle. This can occur when these additional criteria are also met:

- a non-zero dead-band delay is specified (PDC6:PDC0 > 0); and
- the duty cycle has a value of 0 through 3, or 4n + 3 (n ≥ 1).

Work around

None.

Date Codes that pertain to this issue:

All engineering and production devices.

26. Module: MSSP

With MSSP in SPI Master mode, FOSC/64 or Timer2/2 clock rate and CKE = 0, a write collision may occur if SSPBUF is loaded immediately after the transfer is complete. A delay may be required after the MSSP Interrupt Flag bit, SSPIF, is set or the Buffer Full bit, BF, is set, and before writing SSPBUF. If the delay is insufficiently short, a write collision may occur as indicated by the WCOL bit being set.

Work around

Add a software delay of one SCK period after detecting the completed transfer and prior to updating the SSPBUF contents. Verify the WCOL bit is clear after writing SSPBUF. If the WCOL is set, clear the bit in software and rewrite the SSPBUF register.

Date Codes that pertain to this issue:

All engineering and production devices.

27. Module: MSSP

In an I^2C system with multiple slave nodes, an unaddressed slave may respond to bus activity when data on the bus matches its address. The first occurrence will set the BF bit. The second occurrence will set the BF and the SSPOV bits. In both situations, the SSPIF bit is not set and an interrupt will not occur. The device will vector to the Interrupt Service Routine only if the interrupt is enabled and an address match occurs.

Work around

The I^2C slave must clear the SSPOV bit after each I^2C event to maintain normal operation.

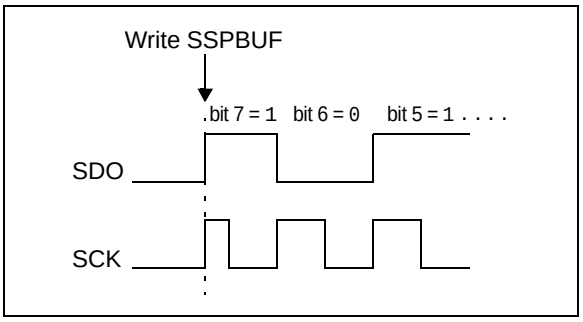
Date Codes that pertain to this issue:

All engineering and production devices.

28. Module: MSSP (SPI Mode)

When the SPI is using Timer2/2 as the clock source, a shorter than expected SCK pulse may occur on the first bit of the transmitted/received data (Figure 1).

FIGURE 1: SCK PULSE VARIATION USING TIMER2/2



Work around

To avoid producing the short pulse, turn off Timer2 and clear the TMR2 register, load the SSPBUF with the data to transmit and then turn Timer2 back on. Refer to Example 6 for sample code.

EXAMPLE 6: AVOIDING THE INITIAL SHORT SCK PULSE

```
LOOP BTFSSPIR1, SSPIF    ;Data received?
                         ;(Xmit complete?)
    BRA LOOP             ;No
    BCF PIR1, SSPIF;Clear flag
    MOVFSSPBUF, W        ;W = SSPBUF
    MOVWFRXDATA    ;Save in user RAM
    MOVFTXDATA, W  ;W = TXDATA
    BCF T2CON, TMR2ON;Timer2 off
    CLRFTMR2       ;Clear Timer2
    MOVWFSSPBUF    ;Xmit New data
```

Date Codes that pertain to this issue:

All engineering and production devices.

29. Module: EUSART

The EUSART auto-baud feature may periodically measure the incoming baud rate incorrectly. The rate of incorrect baud-rate measurements will depend on the frequency of the incoming synchronization byte and the system clock frequency.

Work around

None.

Date Codes that pertain to this issue:

All engineering and production devices.

30. Module: ADC

When the A/D clock source is selected as 2 TOSC or RC (when ADCS2:ADCS0 = 000 or x11), in extremely rare cases, the EIL (Integral Linearity Error) and EDL (Differential Linearity Error) may exceed the data sheet specification at codes 511 and 512 only.

Work around

Select a different A/D clock source (4 TOSC, 8 TOSC, 16 TOSC, 32 TOSC, 64 TOSC) and avoid selecting the 2 TOSC or RC modes.

Date Codes that pertain to this issue:

All engineering and production devices.

31. Module: Brown-out Reset (BOR)

If either the HLVD or USB modules are enabled, clearing the SBOREN bit (RCON<6>) when the software controlled BOR feature is enabled (BOREN1:BOREN0 = 01) may cause a Brown-out Reset (BOR) event.

Work around

Before clearing the SBOREN bit, temporarily disable the HLVD and USB modules.

Date Codes that pertain to this issue:

All engineering and production devices.

32. Module: MSSP

When operated in I^2C™ Master mode, the I^2C baud rate may be somewhat slower than predicted by the following formula:

$$I^2C \text{ Master mode, clock} = \frac{F_{OSC}}{4 \bullet (SSPADD + 1)}$$

Work around

If the target application is sensitive to the baud rate and requires more precision, the SSPADD value can be adjusted to compensate.

If this work around is going to be used, it is recommended that the firmware first check the Revision ID by reading the DEVID1 value at address 3FFFFEh. Silicon revisions B6 and B7 will match the I^2C baud rate predicted by the given formula.

Date Codes that pertain to this issue:

All engineering and production devices.

REVISION HISTORY

Rev A Document (11/2004)
Original version of this document. Includes silicon issues 1 (EUSART), 2 (Timer1/Timer3), 3 (MSSP), 4 (Interrupts), 5-7 (ECCP), 8 (A/D) and 9 (DC Characteristics (BOR)).

Rev B Document (07/2005)
Added silicon issue 10 (USB).

Rev C Document (11/2005)
Updated issue 4 (Interrupts) and added silicon issue 11 (PORTD).

Rev D Document (03/2006)
Added silicon issues 12 (MSSP), 13 (EUSART) and 14 (USB).

Rev E Document (05/2006)
Updated existing silicon issues with Date Code information. Updated work around for silicon issue 2 (Timer1/Timer3), added Example 3 in silicon issue 4 (Interrupts), updated text in silicon issue 6 (ECCP) and updated work around in silicon issue 8 (A/D). Added silicon issues 15-18 (MSSP), 19-22 (EUSART), 23 (Timer1) and 24 (Reset).

Rev F Document (10/2006)
Added silicon issues 25 (ECCP – PWM Mode), 26-27 (MSSP) and 28 (MSSP – SPI Mode).

Rev G Document (07/2007)
Added silicon issues 29 (EUSART) and 30 (ADC).

Rev H Document (03/2008)
Added silicon issue 31 (Brown-out Reset – BOR).

Rev J Document (09/2008)
Revised issue 24 (Reset) and added issue 32 (MSSP).

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