UM10837

PTN3356 (e)DP to VGA Bridge IC Application Board User's Manual

Rev. 1 — 19 January 2015 User manual

Document information

Info	Content
Keywords	PTN3356, DisplayPort, eDP, VGA, bridge, application board
Abstract	This user manual presents the demonstration / application board capability of interfacing an (embedded) DisplayPort source to VGA output. The application board is intended for use as an evaluation and customer demonstration tool, as well as a reference design.

Revision history

Rev	Date	Description
1	20150119	Initial version

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1. Introduction

The PTN3356 is a small package low power DisplayPort to VGA bridge IC optimized primarily for motherboard applications, to convert a DisplayPort signal from the chip set to an analog video signal that directly connects to the VGA connector. The PTN3356 consumes approximately 200 mW of power for video streaming in WUXGA resolution and 410 μW of power in low-power mode. The VGA output is powered down when there is no valid DisplayPort source data being transmitted. The PTN3356 is packaged in HVQFN 32 pin, with dimension of 5 mm x 5 mm x 0.85 mm, 0.5 mm pitch.

The PTN3356 is powered from 3.3 V power source, and generated 1.5 V through an internal step-down switch regulator and buck converter for internal core usage and DAC usage.

For cost saving, the external inductor for the buck converter can be removed, the internal LDO can supply 1.5 V for core usage and DAC usage without any re-work. However, using an LDO will consume twice as much power as the buck converter, about 400 mW.

UM10837 provides information including:

- Overall PCB connectors, jumpers, and power supplies
- Equipment/Tools that this board will be interfacing with for board testing
- System level connections such as cables and connectors that this board will be plugged into

This application board is intended to demonstrate the bridging capabilities of the PTN3356 in a low power DP to VGA conversion application.

1.1 Purposes

1.1.1 Engineers

For engineers to evaluate the performance of the PTN3356 and to develop firmware, including collecting and verifying system level features/performances/functionalities such as:

- Verify power management schemes
- Power sequence
- Power consumption measurement during various operating modes
- Allow access to test points and jumpers for measurement and configuration purposes
- Flash over AUX and MS_I2C
- Programming and debug test via MS_I2C

1.1.2 Marketing

For marketing to demonstrate Ultra small DP-VGA features to customers in the field, such as:

- Functional and interoperability test
- This board should be connected to a DP or an eDP source
- This board can be powered three ways, as detailed in Section 6 "Power options"

1.1.3 Customers

For customers to evaluate the PTN3356 and to:

- Use I2C to change configuration

2. General description

2.1 Layout of the PTN3356

This application board is designed to evaluate the PTN3356 specifically. An HVQFN32 socket footprint is reserved in preparation for socket installation to test and program ICs.

Due to the bulky socket footprint, the bulk converter design has to be placed on the back side to be close to the PTN3356.

Hence the layout is not optimal as if only the PTN3356 is placed without the socket.

The placement can be dramatically improved in a real application.

2.2 Block diagram

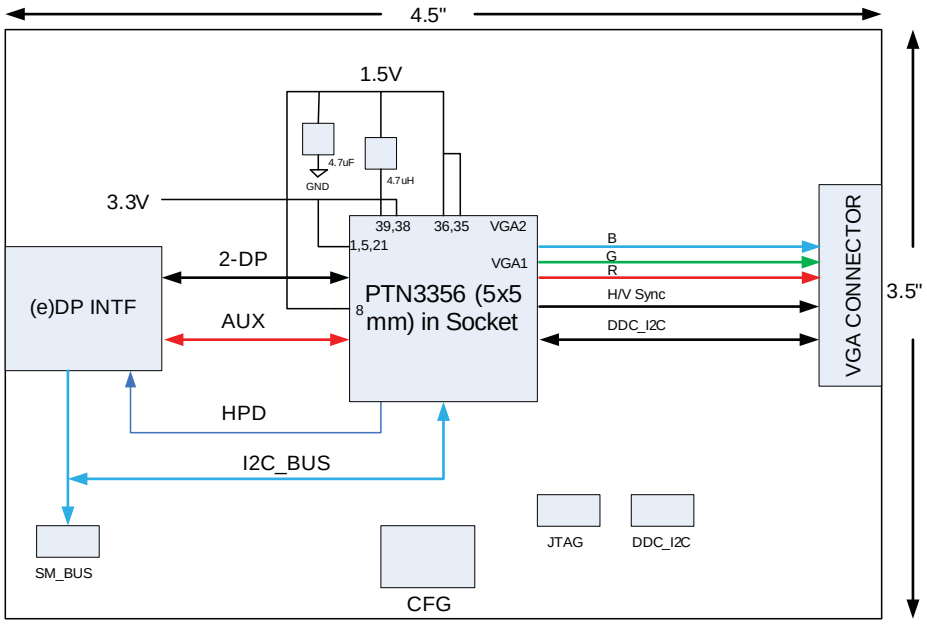


Fig 1. Small ULT DP-VGA application board block diagram

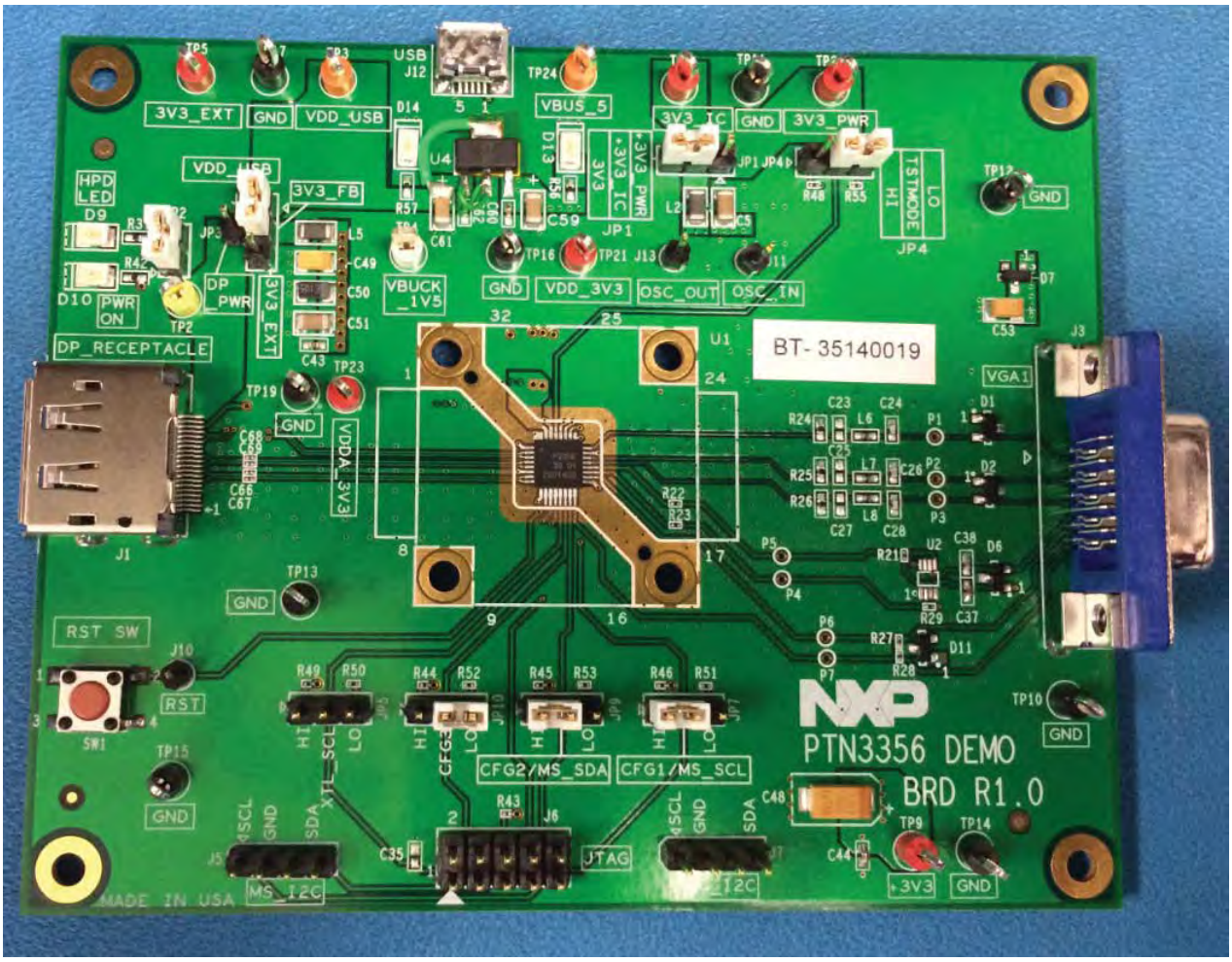


Fig 2. PTN3356 application board

2.3 PTN3356 demo board feature list

- Groups of jumpers for pin configuration
- Other jumpers for test options
- One reset button
- Power LED (Red)
- HPD LED (Green)
- USB 5 V LED (Orange)
- USB 3V3 LED (Orange)
- One I2C header bringing out I2C pins (SCL, SDA, GND) to interface with a I2C-Bird dongle to program (Flash over I2C) and debug
- One I2C header for DDC control
- One JTAG for FW download
- One micro-USB connector to bring in 5 V

- Test point for external power supplies 3.3 V (1A)
- Option to power from DP connector (need to use DP 1.0 cable)
- Jumper to select between 3 power sources

3. Hardware requirements

1. (e)DP sources of Intel, AMD, Apple
2. VTG5225-DP or DPT-200, DP sources with DP 1.1 or DP1.0 cable
3. DPA-400 AUX analyzer
4. Different native resolution monitors
5. FS2 with 2x5 JTAG connection for FW download
6. I2C Bird with 1x4 header connection for slave I2C

4. Board specifications

4.1 PCB description

- Layers: 4 layers expected - trace, ground, VCC, trace
- Size: 3.5" x 4.5"
- Material: FR4
- Thickness: 62 mil
- Impedance: 50 ohm single-end, 75 ohm single-end RGB, 100 ohm differential on DP and AUX signal pairs.

4.2 PCB stack ups

Stack Up

PCB Stack Up				Impedance			
Layer	Type	Thickness (mil)					
Top side solder mask			0.50 mils	Single		DIFF	
L1	TOP	copper+plating	1.50 mils	9.55 mils , 50Ω±10% 3.55 mils , 75Ω±10%	50.19 Ω 74.65 Ω	5.9/5.5/5.9 mils , 100Ω±10%	95.43 Ω
		Prepreg	5.50 mils				
L2	GND	copper	1.40 mils				
		core	47.00 mils				
L3	GND	copper	1.40 mils				
		Prepreg	5.50 mils				
L4	Bottom	copper+plating	1.50 mils			5.9/5.5/5.9 mils , 100Ω±10%	97.26 Ω
Bottom side solder mask			0.50 mils				
TOTAL			64.80 mils 1.65 mm				

Fig 3. Small ULT DP-VGA application board PCB stack up

4.3 Top assembly drawing of the PTN3356 application board

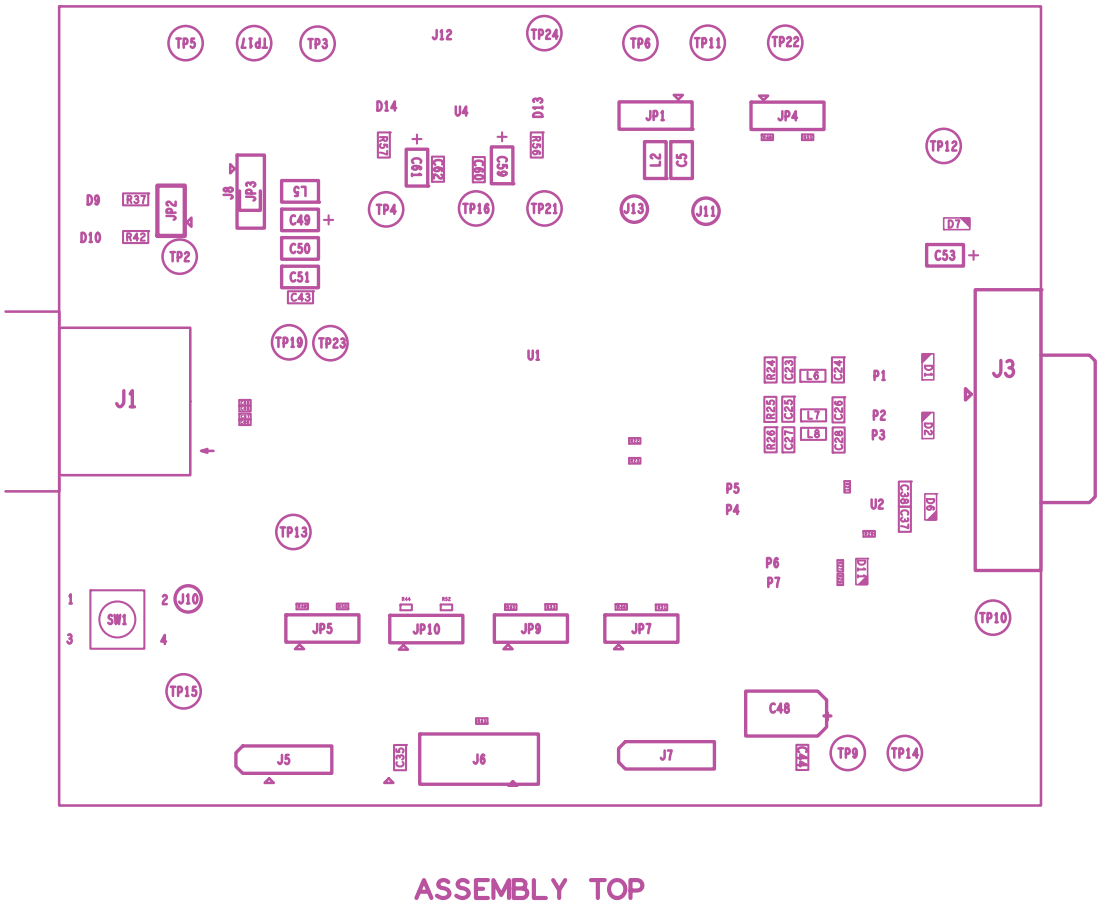


Fig 4. PTN3356 application board top assembly drawing

4.4 Bottom assembly drawing of the PTN3356 application board

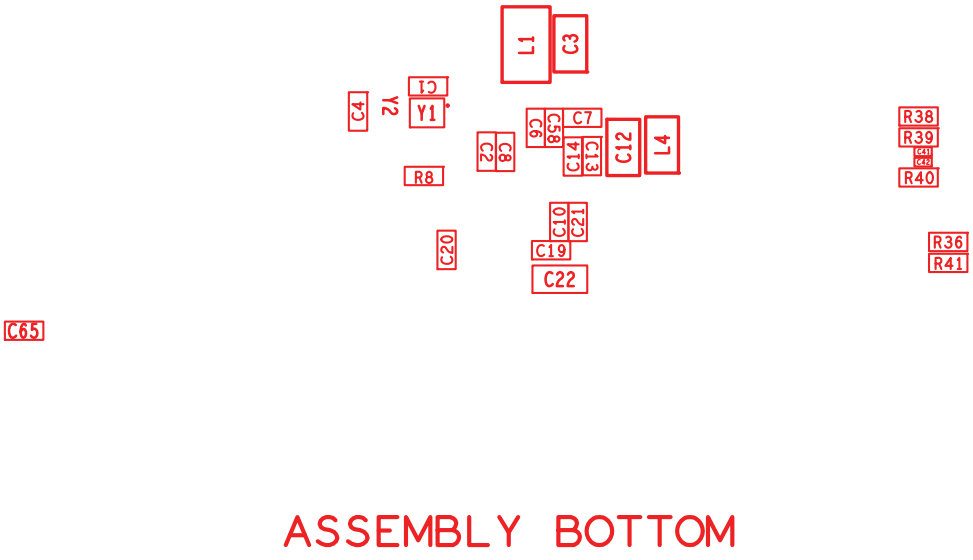


Fig 5. PTN3356 application board bottom assembly drawing

5. Connector specifications

5.1 Connectors and jumpers

Table 1. Connectors and jumpers list

Reference	Value	Description	Manufacturer	Manufacturer number
J1	DP CONN SINK	DP RCPT 20 POS	Molex	47272-0001
J12	Micro-USB	CONN RCPT STD MICRO USB TYPE B	FCI	10103594-0001LF
J3,J4	VGA_CONN	CONN D-SUB RCPT 15POS HD R/A	EDAC	634-015-274-992
J5,J7	HEADER 4	CONN HEADER .100 SINGL STR 4POS	Sullins	PBC04SAAN
J6	HEADER, 2x5	CONN HEADER .100 DUAL STR 10POS	Sullins	PBC05DAAN
J8,J10,J11,J13	CON1	CONN HEADER .100 SINGL STR 1POS	Sullins	PBC01SAAN
JP1,JP3,JP4,JP5,JP7, JP9,JP10	HEADER 3	CONN HEADER .100 SINGL STR 3POS	Sullins	PBC03SAAN
JP2	HEADER 2	CONN HEADER .100 SINGL STR 2POS	Sullins	PBC02SAAN

5.2 Jumper settings

Table 2. Jumper settings

Jumper #	Signal names	Jumper settings	Default setting
JP1	+3V3_IC	1-2, select external power to measure IC 2-3, select 3 to 1 power source (JP3 & J8)	2-3
JP2	HPD_ON	1-2 Enable HPD LED OPEN: Disable HPD LED	1-2
JP3 & J8	+3V3_FB	2-1, Select 3V3 from USB source 2-3, Select external power supply JP3-2 to J8-1, Select DP power	1-2
JP4	TESTMODE	1-2 HIGH, CFG[5:1] = JTAG PINS 2-3 LOW, CFG[5:1] = CONFIG PINS. I2C = 40H OPEN, CFG[5:1] = CONFIG PINS. I2C = C0H	2-3
JP5	CFG5_TCK	1-2 HIGH, 24 MHZ XTAL is used OPEN, 27 MHZ XTAL is used 2-3 LOW, 25 MHZ XTAL is used	OPEN
JP7	CFG1-MS_SCL/TDI	CFG1, CFG2: 11: Compliant HPD behavior, MS Bus is used 10: Non-compliant HPD behavior	2-3
JP9	CFG2-MS_SDA/TMS	01: Non-compliant HPD behavior 00: Compliant HPD behavior, MS bus is not used	2-3
JP10	CFG3-SPARE	RESERVED	OPEN

5.3 Test points

Table 3. Test points listing

Test point number	Color	Signal names
J10	HDR_1X1	RST_N
J11	HDR_1X1	OSC_IN
J13	HDR_1X1	OSC_OUT
TP2	YELLOW	DP_PWR
TP3	ORANGE	VSS_USB
TP4	WHITE	VBUCK_1V5
TP5	RED	3V3_EXT
TP6	RED	+3V3_IC
TP9	RED	+3V3
TP10,TP11-TP17,TP19	BLACK	GND
TP21	RED	VDD_3V3
TP22	RED	+3V3_PWR
TP23	RED	VDDA_3V3
TP24	ORANGE	VBUS_5

5.4 Cables

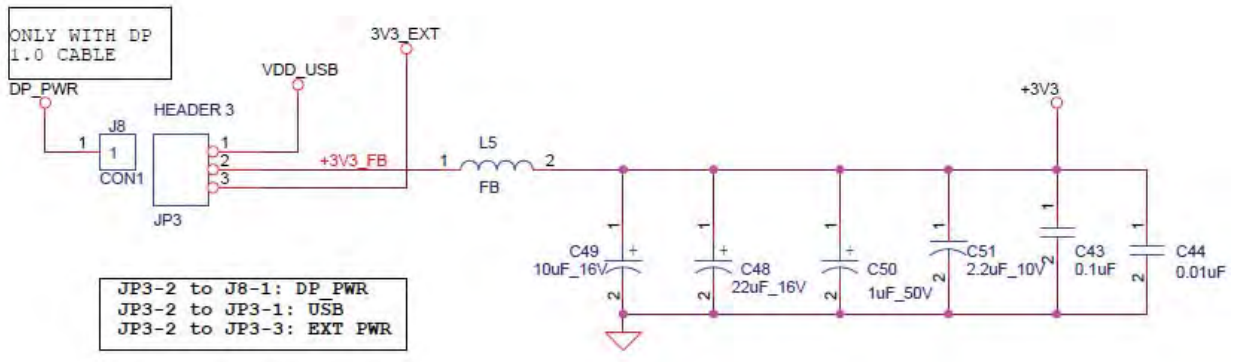
- DP 1.0 cable to power the application board
- DP 1.1 cable for DP communication only
- VGA cable
- Micro-USB cable

6. Power options

The PTN3356 application board can be powered by three different methods, selected via JP3 and J8:

1. Micro-USB cable that carries 5 V power
2. External power supplies with +3.3V (1A)
3. DP 1.0 cable that carries 3V3 power

See schematic below for jumper settings.



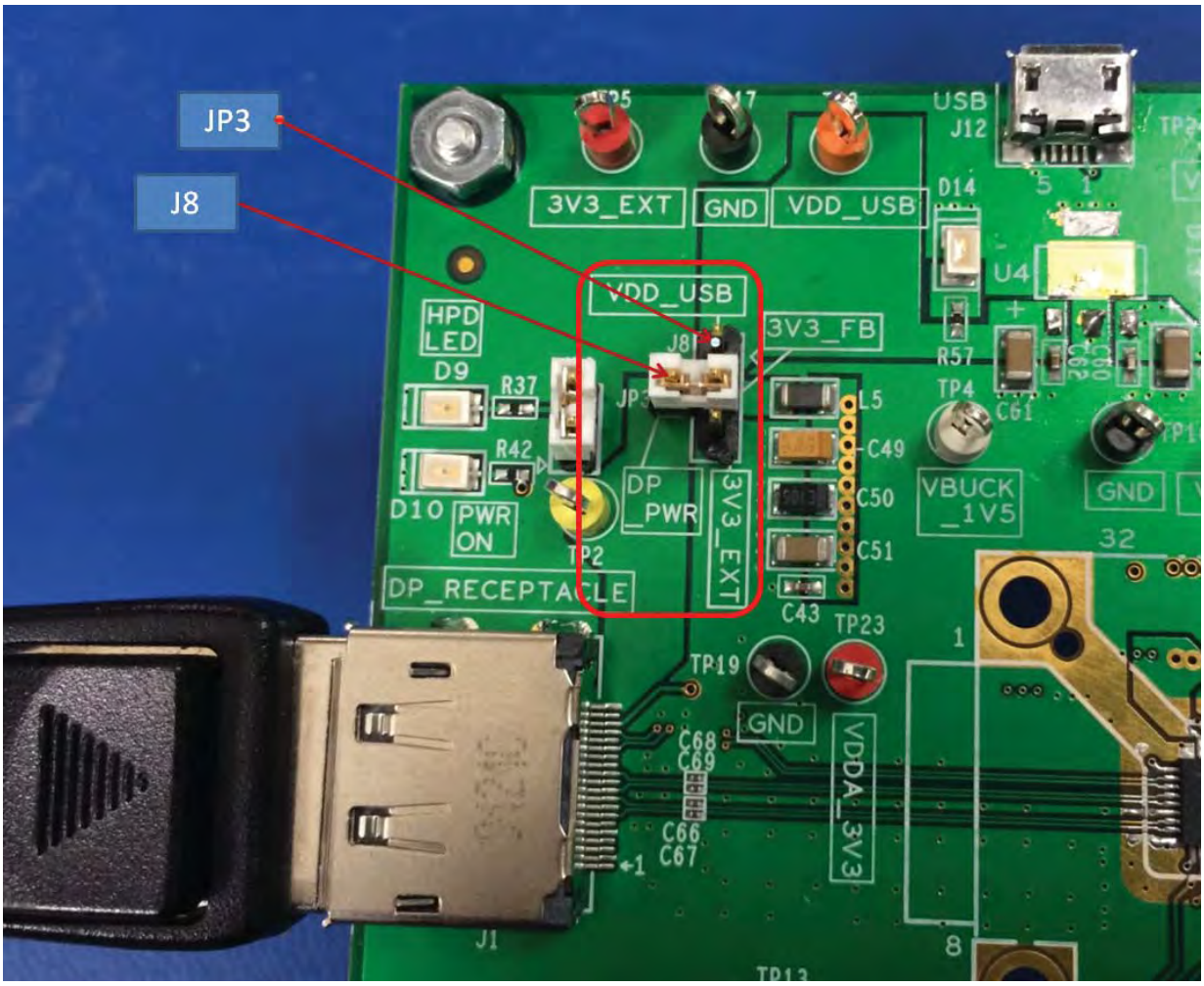


Fig 6. Power 3-way selection jumper JP3 and J8

6.1 DP 1.0 cable

Set JP3-2 to J8-1 to select DP power.

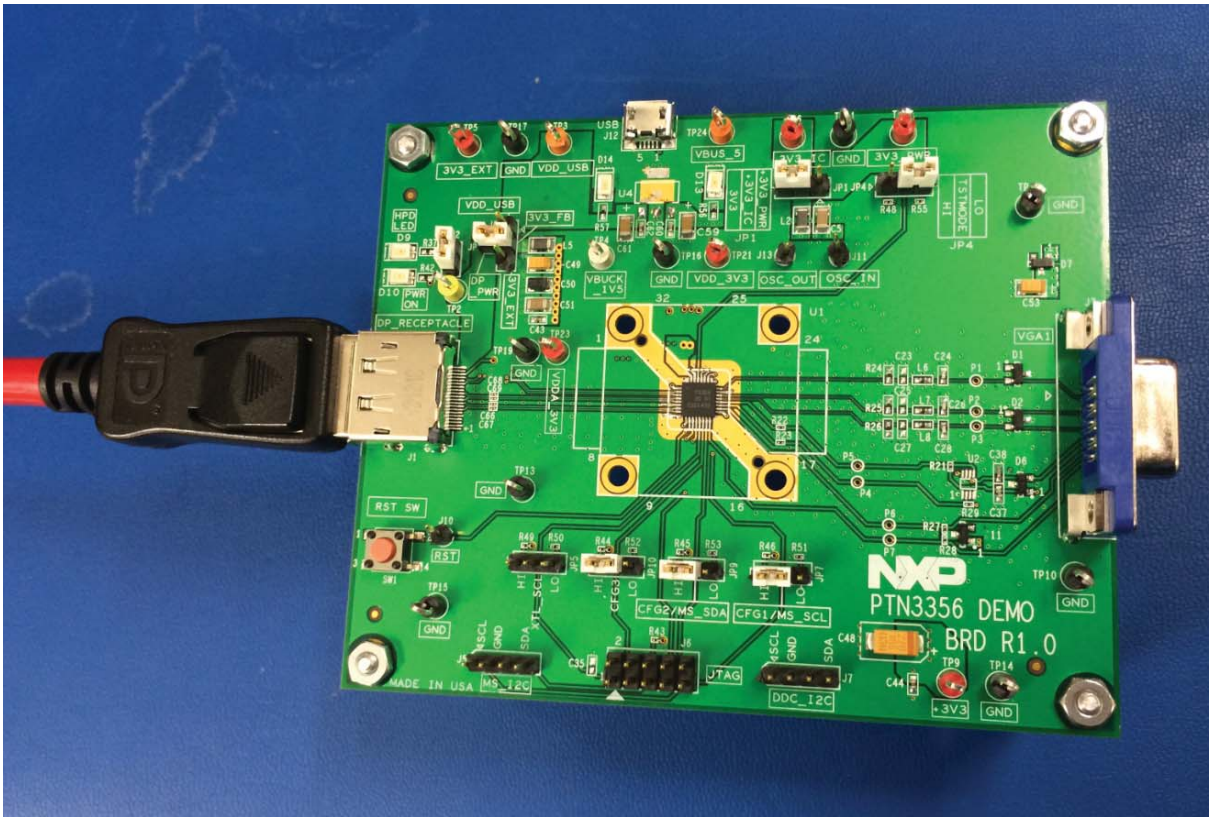


Fig 7. Power by DP 1.0 cable

6.2 5 V micro-USB

Set JP3 pin 2 to pin 1 to select 3V3 from USB source (5 V steps down to 3V3 via U4).

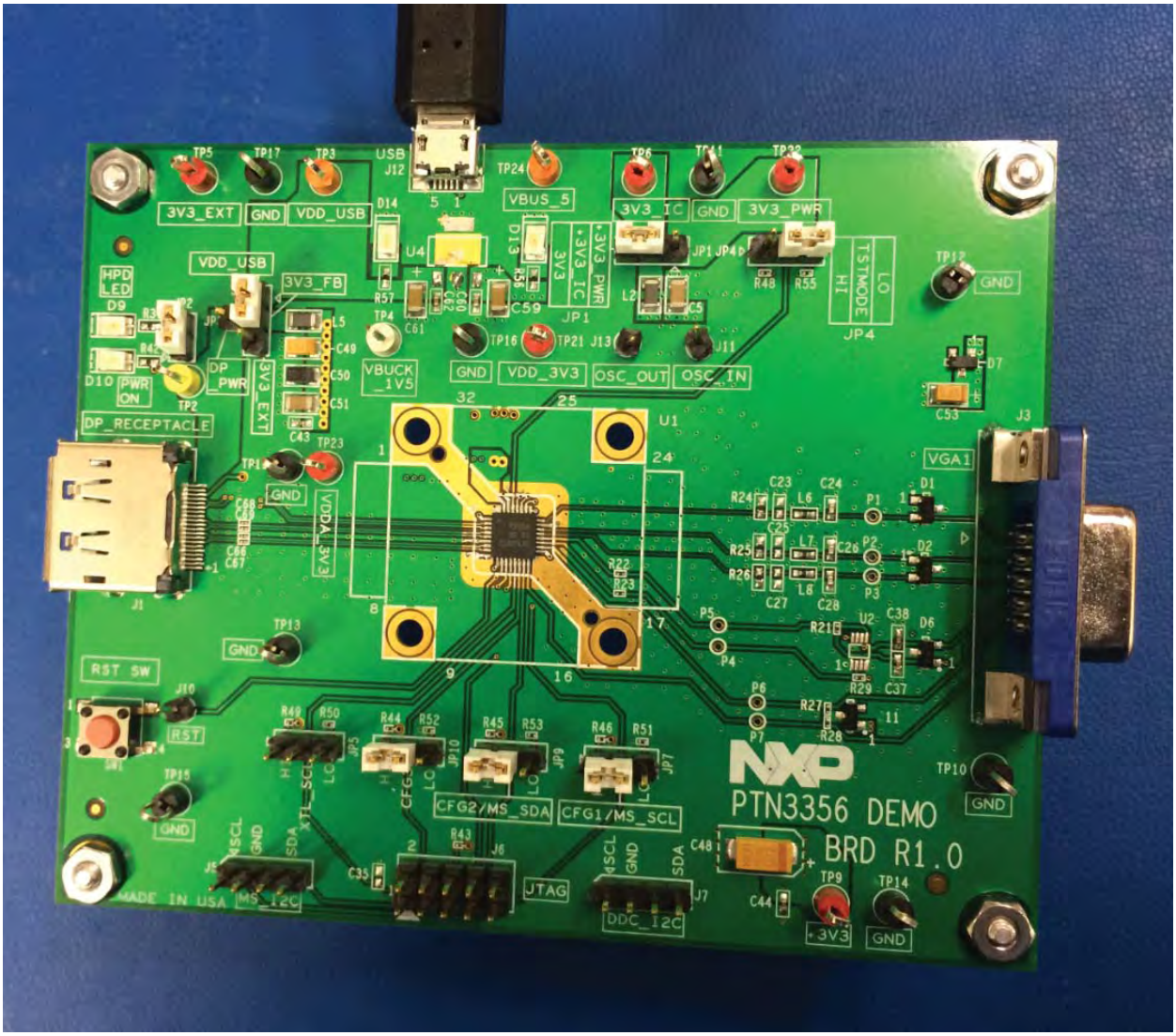


Fig 8. Power by micro-USB

6.3 External power source

Set JP3 pin 2 to pin 3 to select external 3.3 V power supply.

Clip 3.3 V power lead to TP5, and clip ground lead to GND test point.

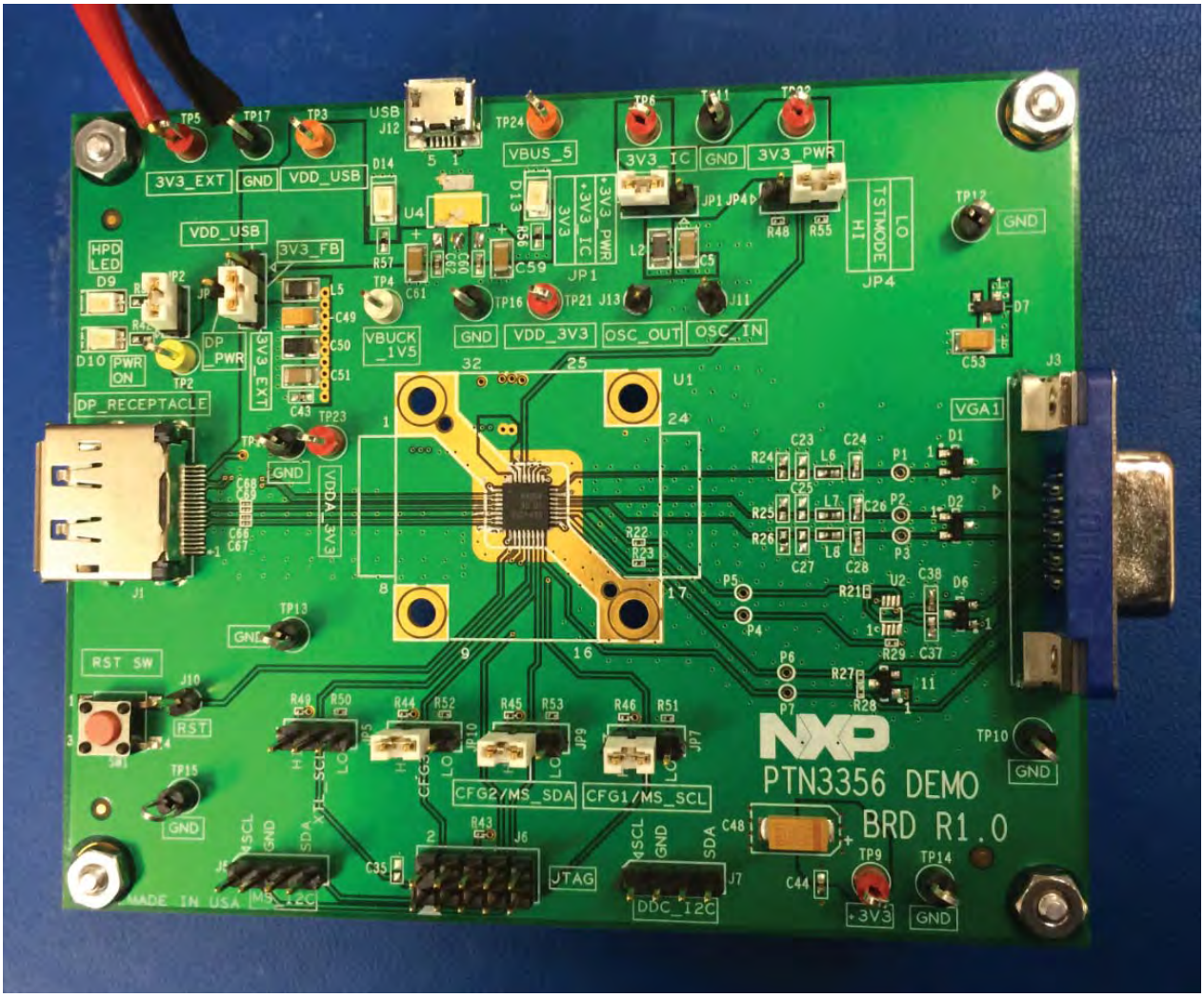


Fig 9. Power by external 3.3 V power supply

7. Operation mode

The PTN3356 can be operated in two different modes. The trade-off is power vs. BOM cost.

Buck Converter mode saves power, while LDO mode saves BOM cost.

The microprocessor inside the PTN3356 is responsible for switching on the Buck converter.

This is done after the DP source finishes link training.

LDO to Buck hand over is done when the voltage set point is higher than that of the LDO.

LDO pulls up the voltage at its output. By switching on the Buck at 1.5 V and lowering the LDO set point to 1.4 V, the LDO stops sourcing current, hence the Buck takes over.

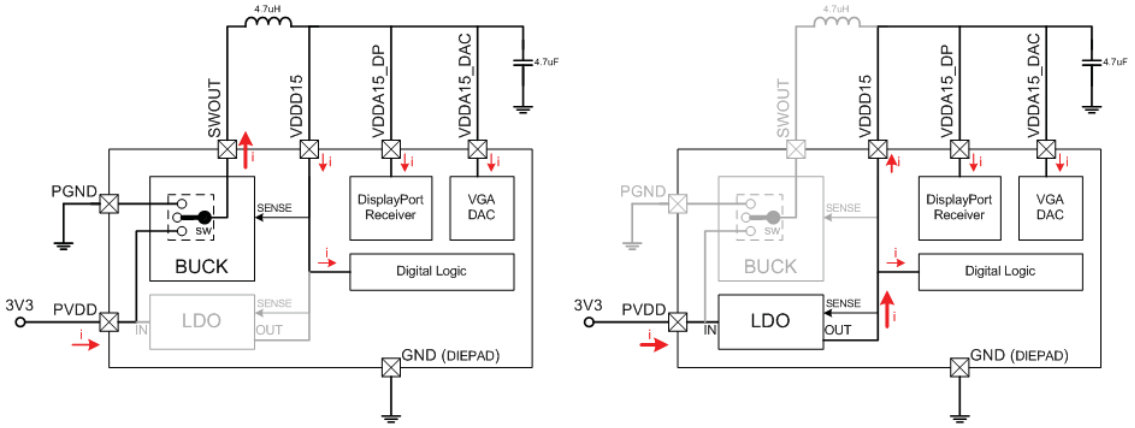


Fig 10. PTN3356 Buck vs LDO modes

7.1 Buck converter mode

Voltage input pin: PVDD33

Current output pin: SWOUT

Buck output pin: One 4.7 μH inductor is connected to SWOUT pin, Buck out pin is the other end of 4.7 μH which is connected directly to VDDD15 pin. SWOUT pin

Buck voltage sensing input VDDD15 (very important, if VDD15 is not connected to the inductor the buck converter cannot work at all. It does work fine if either VDDA15_* pins aren't connected)

1.5 V input pins: VDDD15, VDDA15_DP, VDDA15_DAC

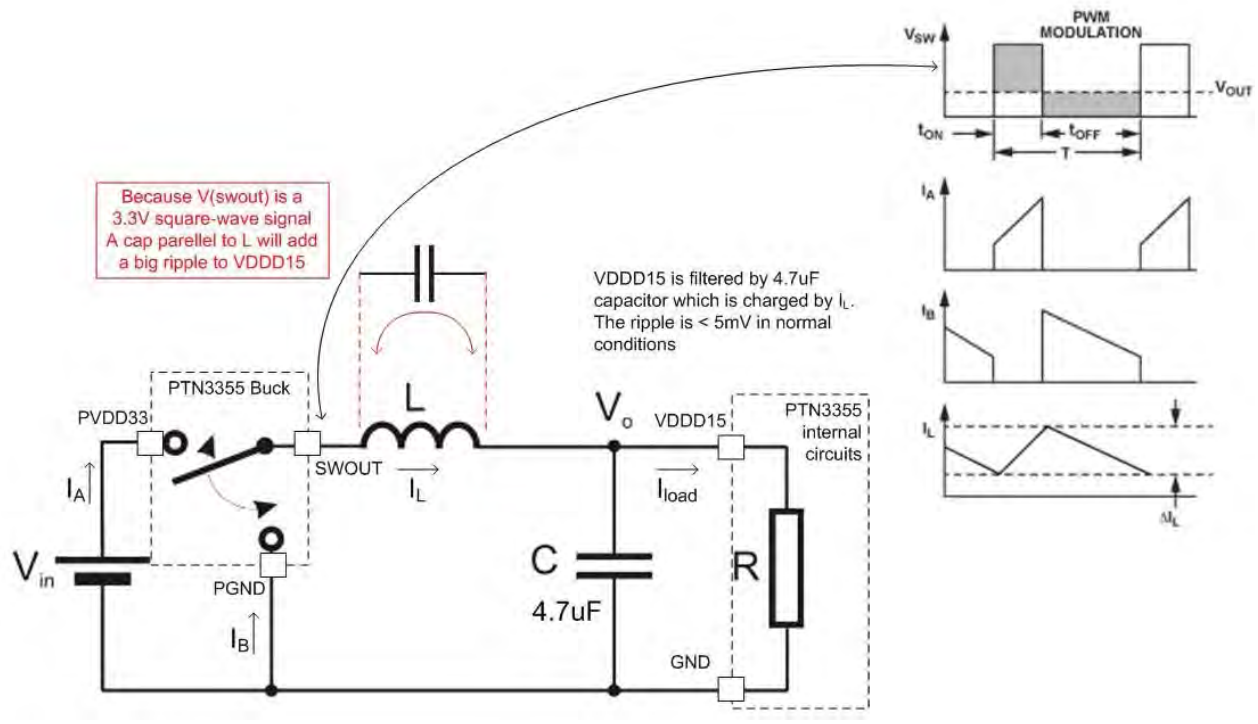


Fig 11. Buck converter operation

7.2 LDO mode

Voltage input pin: PVDD33

Voltage output pin: VDDD15

1.5 V input pins: VDDA15_DP, VDDA15_DAC

VDDD15 pin is a regulated supply output in LDO mode and it combines the Buck voltage-sense input with core supply input functions while in Buck mode

8. References

[1] Data Specification, PTN3356_CONFIDENTIAL.pdf, Aug. 2014

[2] Schematic, PTN3356 rev10.pdf

[3] BOM, PTN3356 REV10 BOM.xls

[4] AN11590-PTN3356 Layout Guideline rev1.pdf

[5] Allegro layout, QDS5874_NXP_PTN3356_DEMO_BOARD_REV1_PCB_FINAL-5.brd

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