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Kind regards,

Team Nexperia

# 74ABT16240A

## 16-bit inverting buffer/line driver; 3-state

Rev. 6 — 3 November 2011 Product data sheet

## 1. General description

The 74ABT16240A high-performance BiCMOS device combines low static and dynamic power dissipation with high speed and high output drive.

The 74ABT16240A is an inverting 16-bit buffer that is ideal for driving bus lines. The device features four output enable inputs ($1\overline{OE}$, $2\overline{OE}$, $3\overline{OE}$, $4\overline{OE}$), each controlling four of the 3-state outputs.

## 2. Features and benefits

- 16-bit bus interface
- Multiple $V_{CC}$ and GND pins minimize switching noise
- Power-up 3-state
- 3-state buffers
- TTL input and output switching levels
- Input and output interface capability to systems at 5 V supply
- Output capability: +64 mA and –32 mA
- Live insertion and extraction permitted
- Latch-up protection exceeds 500 mA per JESD78 class II level A
- ESD protection:
  - HBM JESD-A114E exceeds 2000 V
  - CDM JESD22-C101-C exceeds 1000 V

## 3. Ordering information

**Table 1. Ordering information**

| Type number | Package | | | |
|---|---|---|---|---|
| | Temperature range | Name | Description | Version |
| 74ABT16240ADGG | –40 °C to +85 °C | TSSOP48 | plastic thin shrink small outline package; 48 leads; body width 6.1 mm | SOT362-1 |
| 74ABT16240ADL | –40 °C to +85 °C | SSOP48 | plastic shrink small outline package; 48 leads; body width 7.5 mm | SOT370-1 |

## 4. Functional diagram

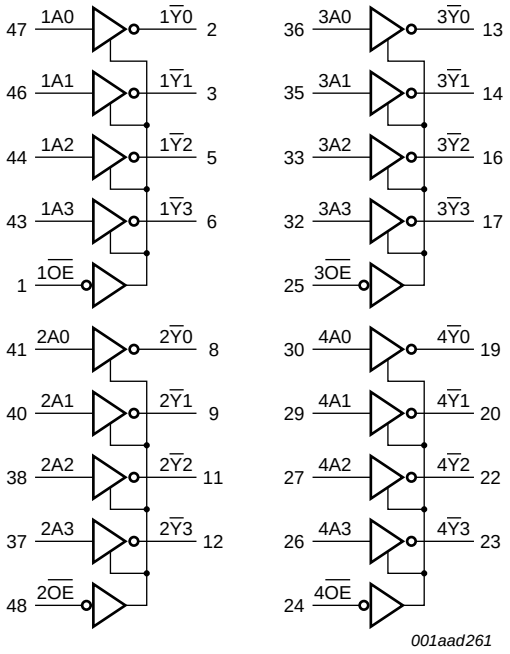



**Fig 1. Logic symbol**

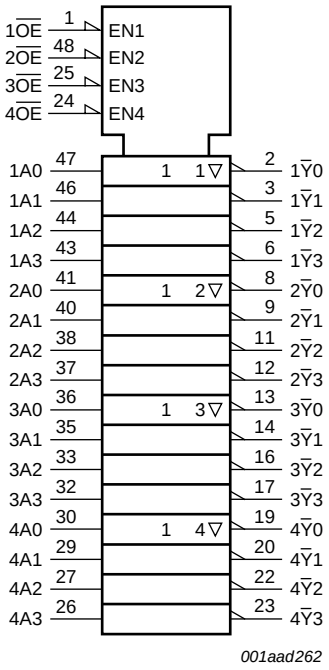



**Fig 2. IEC logic symbol**

# 5. Pinning information

## 5.1 Pinning

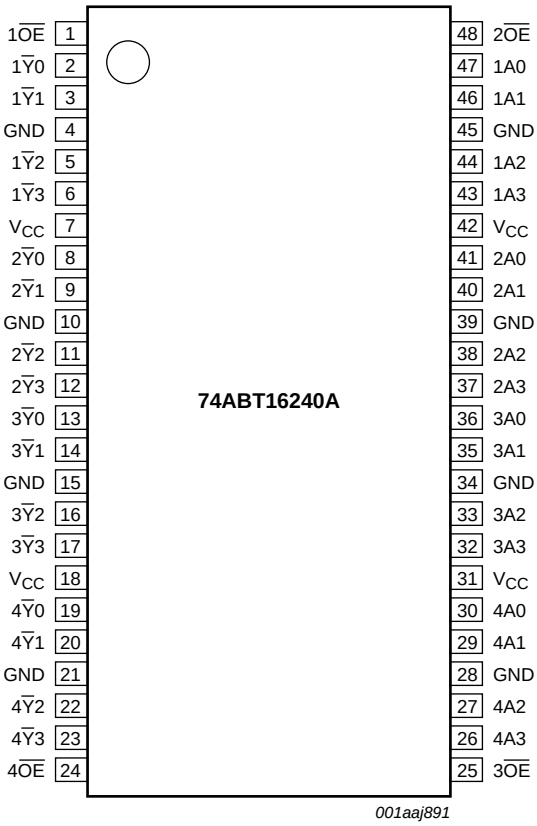



**Fig 3. Pin configuration**

## 5.2 Pin description

**Table 2. Pin description**

| Symbol | Pin | Description |
|---|---|---|
| $1\overline{OE}$, $2\overline{OE}$, $3\overline{OE}$, $4\overline{OE}$ | 1, 48, 25, 24 | output enable (LOW active) |
| $1\overline{Y}0$, $1\overline{Y}1$, $1\overline{Y}2$, $1\overline{Y}3$ | 2, 3, 5, 6 | 1 data output |
| GND | 4, 10, 15, 21, 28, 34, 39, 45 | ground (0 V) |
| $V_{CC}$ | 7, 18, 31, 42 | supply voltage |
| $2\overline{Y}0$, $2\overline{Y}1$, $2\overline{Y}2$, $2\overline{Y}3$ | 8, 9, 11, 12 | 2 data output |
| $3\overline{Y}0$, $3\overline{Y}1$, $3\overline{Y}2$, $3\overline{Y}3$ | 13, 14, 16, 17 | 3 data output |
| $4\overline{Y}0$, $4\overline{Y}1$, $4\overline{Y}2$, $4\overline{Y}3$ | 19, 20, 22, 23 | 4 data output |
| 4A0, 4A1, 4A2, 4A3 | 30, 29, 27, 26 | 4 data input |
| 3A0, 3A1, 3A2, 3A3 | 36, 35, 33, 32 | 3 data input |
| 2A0, 2A1, 2A2, 2A3 | 41, 40, 38, 37 | 2 data input |
| 1A0, 1A1, 1A2, 1A3 | 47, 46, 44, 43 | 1 data input |

## 6. Functional description

**Table 3. Function table[1]**

| Control | Input | Output |
|---|---|---|
| $\overline{nOE}$ | nAn | n$\overline{Y}$n |
| L | L | H |
| L | H | L |
| H | X | Z |

[1] H = HIGH voltage level; L = LOW voltage level; X = don't care; Z = high-impedance OFF-state.

## 7. Limiting values

**Table 4. Limiting values**

*In accordance with the Absolute Maximum Rating System (IEC 60134).*

| Symbol | Parameter | Conditions | | Min | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{CC}$ | supply voltage | | | –0.5 | +7.0 | V |
| $V_I$ | input voltage | | [1] | –1.2 | +7.0 | V |
| $V_O$ | output voltage | output in OFF-state or HIGH-state | [1] | –0.5 | +5.5 | V |
| $I_{IK}$ | input clamping current | $V_I < 0$ V | | –18 | - | mA |
| $I_{OK}$ | output clamping current | $V_O < 0$ V | | –50 | - | mA |
| $I_O$ | output current | output in LOW-state | | - | 128 | mA |
| | | output in HIGH-state | | - | –64 | mA |
| $T_j$ | junction temperature | | [2] | - | 150 | °C |
| $T_{stg}$ | storage temperature | | | –65 | +150 | °C |

[1] The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

[2] The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability.

## 8. Recommended operating conditions

**Table 5. Operating conditions**

*Voltages are referenced to GND (ground = 0 V).*

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{CC}$ | supply voltage | | 4.5 | - | 5.5 | V |
| $V_I$ | input voltage | | 0 | - | $V_{CC}$ | V |
| $V_{IH}$ | HIGH-level input voltage | | 2.0 | - | - | V |
| $V_{IL}$ | LOW-level Input voltage | | - | - | 0.8 | V |
| $I_{OH}$ | HIGH-level output current | | –32 | - | - | mA |
| $I_{OL}$ | LOW-level output current | | - | - | 32 | mA |
| | | duty cycle ≤ 50 %; $f_i \geq 1$ kHz | - | - | 64 | mA |
| $\Delta t/\Delta V$ | input transition rise and fall rate | | - | - | 10 | ns/V |
| $T_{amb}$ | ambient temperature | in free air | –40 | - | +85 | °C |

## 9. Static characteristics

**Table 6. Static characteristics**

| Symbol | Parameter | Conditions | | 25 °C | | | –40 °C to +85 °C | | Unit |
|---|---|---|---|---|---|---|---|---|---|
| | | | | Min | Typ | Max | Min | Max | |
| $V_{IK}$ | input clamping voltage | $V_{CC}$ = 4.5 V; $I_{IK}$ = –18 mA | | –1.2 | –0.9 | - | –1.2 | - | V |
| $V_{OH}$ | HIGH-level output voltage | $V_I$ = $V_{IL}$ or $V_{IH}$ | | | | | | | |
| | | $V_{CC}$ = 4.5 V; $I_{OH}$ = –3 mA | | 2.5 | 2.9 | - | 2.5 | - | V |
| | | $V_{CC}$ = 5.0 V; $I_{OH}$ = –3 mA | | 3.0 | 3.4 | - | 3.0 | - | V |
| | | $V_{CC}$ = 4.5 V; $I_{OH}$ = –32 mA | | 2.0 | 2.4 | - | 2.0 | - | V |
| $V_{OL}$ | LOW-level output voltage | $V_{CC}$ = 4.5 V; $I_{OL}$ = 64 mA; $V_I$ = $V_{IL}$ or $V_{IH}$ | | - | 0.42 | 0.55 | - | 0.55 | V |
| $I_I$ | input leakage current | $V_{CC}$ = 5.5 V; $V_I$ = $V_{CC}$ or GND | | - | ±0.01 | ±1.0 | - | ±1.0 | µA |
| $I_{OFF}$ | power-off leakage current | $V_{CC}$ = 0 V; $V_I$ or $V_O$ ≤ 4.5 V | | - | ±5.0 | ±100 | - | ±100 | µA |
| $I_{O(pu/pd)}$ | power-up/power-down output current | $V_{CC}$ = 2.0 V; $V_O$ = 0.5 V; $V_I$ = GND or $V_{CC}$; $n\overline{OE}$ = HIGH | [1] | - | ±5.0 | ±50 | - | ±50 | µA |
| $I_{OZ}$ | OFF-state output current | $V_{CC}$ = 5.5 V; $V_I$ = $V_{IL}$ or $V_{IH}$ | | | | | | | |
| | | output HIGH-state at $V_O$ = 5.5 V | | - | 1.0 | 10 | - | 10 | µA |
| | | output LOW-state at $V_O$ = 0.5 V | | - | –1.0 | –10 | - | –10 | µA |
| $I_{LO}$ | output leakage current | HIGH-state; $V_O$ = 5.5 V; $V_{CC}$ = 5.5 V; $V_I$ = GND or $V_{CC}$ | | - | 1.0 | 50 | - | 50 | µA |
| $I_O$ | output current | $V_{CC}$ = 5.5 V; $V_O$ = 2.5 V | [2] | –180 | –70 | –50 | –180 | –50 | mA |
| $I_{CC}$ | supply current | $V_{CC}$ = 5.5 V; $V_I$ = GND or $V_{CC}$ | | | | | | | |
| | | outputs HIGH-state | | - | 0.5 | 1.0 | - | 1.0 | mA |
| | | outputs LOW-state | | - | 8 | 19 | - | 19 | mA |
| | | outputs 3-state | | - | 0.5 | 1.0 | - | 1.0 | mA |
| $\Delta I_{CC}$ | additional supply current | per input pin; $V_{CC}$ = 5.5 V; one input at 3.4 V and other inputs at $V_{CC}$ or GND | [3][4] | - | 10 | 200 | - | 200 | µA |
| $C_I$ | input capacitance | $V_I$ = 0 V or $V_{CC}$ | | - | 4 | - | - | - | pF |
| $C_{I/O}$ | input/output capacitance | outputs disabled; $V_O$ = 0 V or $V_{CC}$ | | - | 6 | - | - | - | pF |

[1] This parameter is valid for any $V_{CC}$ between 0 V and 2.1 V, with a transition time of up to 10 ms. From $V_{CC}$ = 2.1 V to $V_{CC}$ = 5 V ± 10 %, a transition time of up to 100 µs is permitted.

[2] Not more than one output should be tested at a time, and the duration of the test should not exceed one second.

[3] This is the increase in supply current for each input at 3.4 V.

[4] This data sheet limit may vary among suppliers.

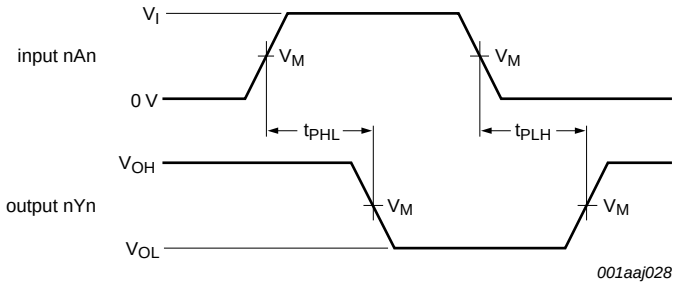
## 10. Dynamic characteristics

**Table 7. Dynamic characteristics**

*GND = 0 V. For test circuit, see Figure 6.*

| Symbol | Parameter | Conditions | 25 °C; $V_{CC}$ = 5.0 V | | | –40 °C to +85 °C; $V_{CC}$ = 5.0 V ± 0.5 V | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | Min | Max | |
| $t_{PLH}$ | LOW to HIGH propagation delay | nAn to n$\overline{Y}$n, see Figure 4 | 1.0 | 2.0 | 3.0 | 1.0 | 3.7 | ns |
| $t_{PHL}$ | HIGH to LOW propagation delay | nAn to n$\overline{Y}$n, see Figure 4 | 1.0 | 1.5 | 3.0 | 1.0 | 3.5 | ns |
| $t_{PZH}$ | OFF-state to HIGH propagation delay | n$\overline{OE}$ to n$\overline{Y}$n; see Figure 5 | 1.2 | 2.4 | 3.3 | 1.2 | 4.2 | ns |
| $t_{PZL}$ | OFF-state to LOW propagation delay | n$\overline{OE}$ to n$\overline{Y}$n; see Figure 5 | 1.2 | 2.3 | 3.2 | 1.0 | 4.2 | ns |
| $t_{PHZ}$ | HIGH to OFF-state propagation delay | n$\overline{OE}$ to n$\overline{Y}$n; see Figure 5 | 1.3 | 2.7 | 4.1 | 1.6 | 4.7 | ns |
| $t_{PLZ}$ | LOW to OFF-state propagation delay | n$\overline{OE}$ to n$\overline{Y}$n; see Figure 5 | 1.3 | 2.5 | 3.6 | 1.4 | 4.1 | ns |

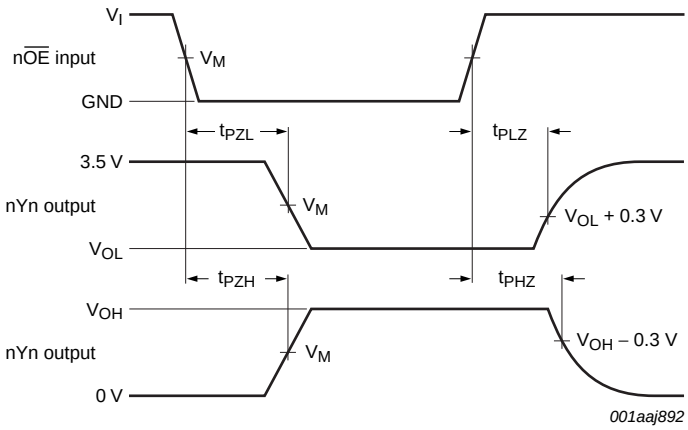
## 11. Waveforms




$V_M$ = 1.5 V

$V_{OL}$ and $V_{OH}$ are typical voltage output levels that occur with the output load.

**Fig 4. Input (nAn) to output (nYn) propagation delay**

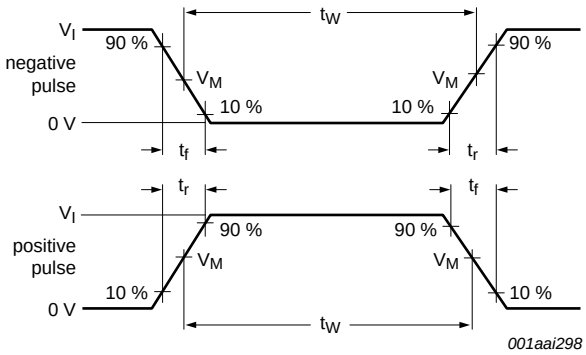



$V_M$ = 1.5 V

$V_{OL}$ and $V_{OH}$ are typical voltage output levels that occur with the output load.

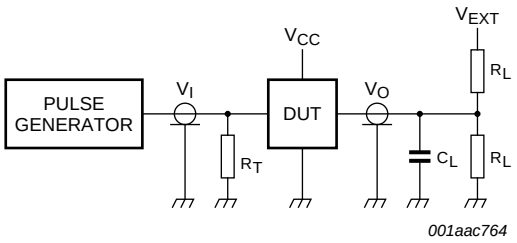
**Fig 5. 3-state output enable and disable times**

## 12. Test information




$V_M$ = 1.5 V

a. Input pulse definition




Test data is given in Table 8.

Definitions test circuit:

$R_L$ = Load resistance.

$C_L$ = Load capacitance including jig and probe capacitance.

$R_T$ = Termination resistance should be equal to output impedance $Z_o$ of the pulse generator.

b. Test circuit for 3-state outputs

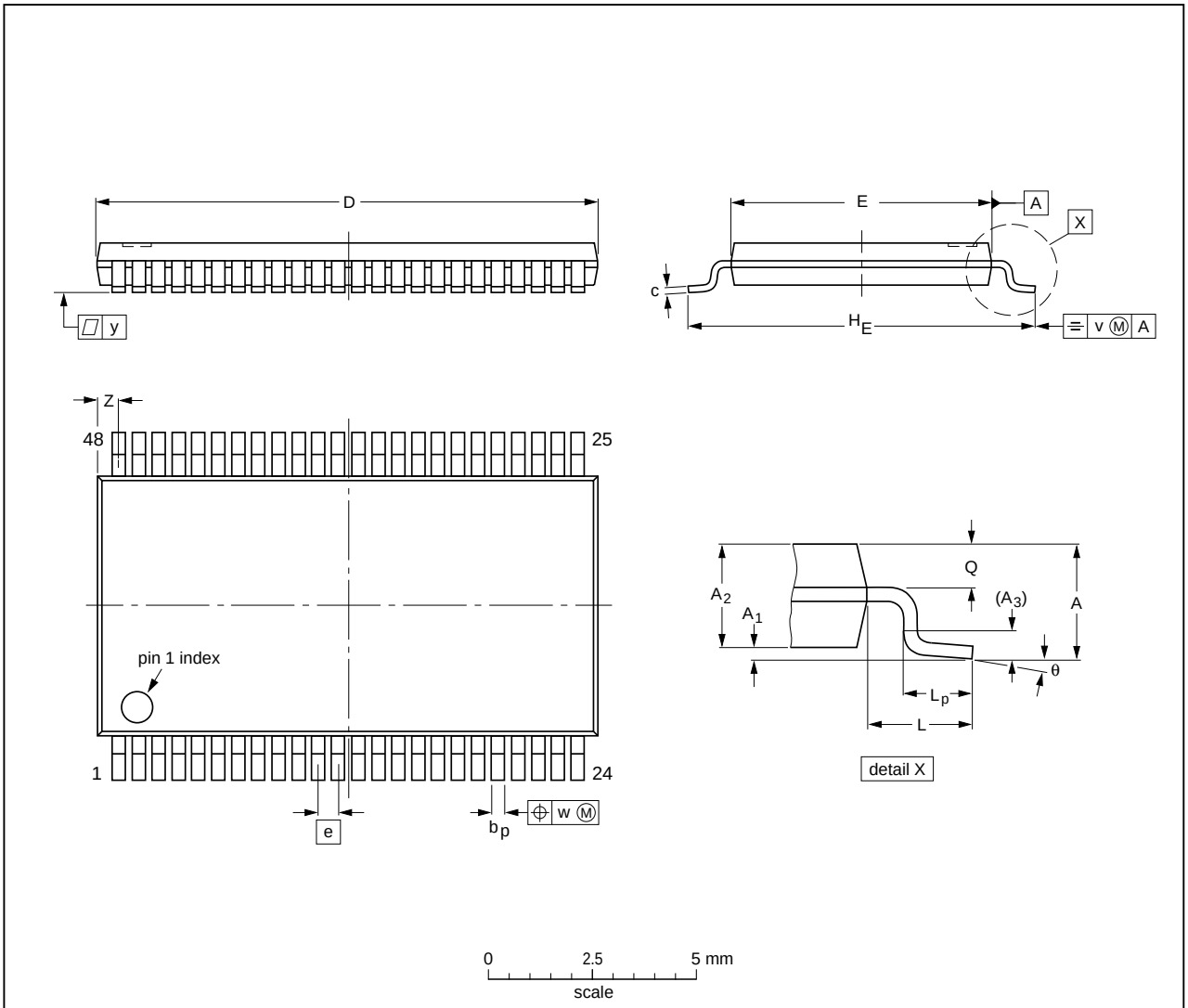
**Fig 6. Load circuitry for switching times**

**Table 8. Test data**

| Input | | | | Load | | $V_{EXT}$ | | |
|---|---|---|---|---|---|---|---|---|
| $V_I$ | $f_i$ | $t_W$ | $t_r$, $t_f$ | $C_L$ | $R_L$ | $t_{PHZ}$, $t_{PZH}$ | $t_{PLZ}$, $t_{PZL}$ | $t_{PLH}$, $t_{PHL}$ |
| 3.0 V | 1 MHz | 500 ns | 2.5 ns | 50 pF | 500 Ω | open | 7.0 V | open |

## 13. Package outline

**TSSOP48: plastic thin shrink small outline package; 48 leads; body width 6.1 mm** **SOT362-1**




**DIMENSIONS (mm are the original dimensions).**

| UNIT | A max. | $A_1$ | $A_2$ | $A_3$ | $b_p$ | c | $D^{(1)}$ | $E^{(2)}$ | e | $H_E$ | L | $L_p$ | Q | v | w | y | Z | θ |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| mm | 1.2 | 0.15<br>0.05 | 1.05<br>0.85 | 0.25 | 0.28<br>0.17 | 0.2<br>0.1 | 12.6<br>12.4 | 6.2<br>6.0 | 0.5 | 8.3<br>7.9 | 1 | 0.8<br>0.4 | 0.50<br>0.35 | 0.25 | 0.08 | 0.1 | 0.8<br>0.4 | $8^o$<br>$0^o$ |

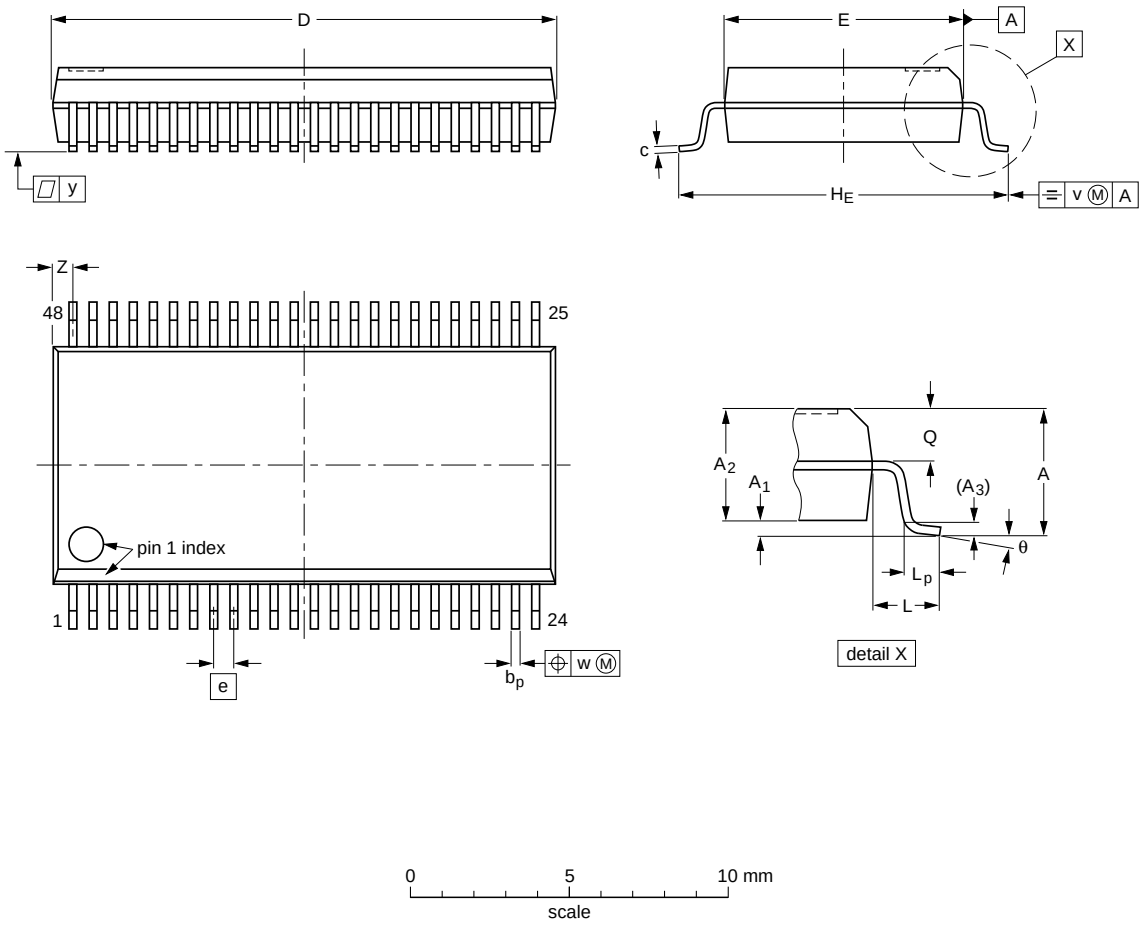
**Notes**

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

| OUTLINE VERSION | REFERENCES | | | | EUROPEAN PROJECTION | ISSUE DATE |
|---|---|---|---|---|---|---|
| | IEC | JEDEC | JEITA | | | |
| SOT362-1 | | MO-153 | | | | ~~99-12-27~~<br>03-02-19 |

**Fig 7. Package outline SOT362-1 (TSSOP48)**

**SSOP48: plastic shrink small outline package; 48 leads; body width 7.5 mm** **SOT370-1**







**DIMENSIONS (mm are the original dimensions)**

| UNIT | A max. | $A_1$ | $A_2$ | $A_3$ | $b_p$ | c | D (1) | E (1) | e | $H_E$ | L | $L_p$ | Q | v | w | y | Z (1) | θ |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| mm | 2.8 | 0.4<br>0.2 | 2.35<br>2.20 | 0.25 | 0.3<br>0.2 | 0.22<br>0.13 | 16.00<br>15.75 | 7.6<br>7.4 | 0.635 | 10.4<br>10.1 | 1.4 | 1.0<br>0.6 | 1.2<br>1.0 | 0.25 | 0.18 | 0.1 | 0.85<br>0.40 | $8^o$<br>$0^o$ |

**Note**

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

| OUTLINE VERSION | REFERENCES | | | | EUROPEAN PROJECTION | ISSUE DATE |
|---|---|---|---|---|---|---|
| | IEC | JEDEC | JEITA | | | |
| SOT370-1 | | MO-118 | | | | ~~99-12-27~~<br>03-02-19 |

**Fig 8. Package outline SOT370-1 (SSOP48)**

## 14. Abbreviations

**Table 9. Abbreviations**

| Acronym | Description |
|---|---|
| BiCMOS | Bipolar CMOS |
| DUT | Device Under Test |
| ESD | ElectroStatic Discharge |
| HBM | Human Body Model |
| CDM | Charged Device Model |
| TTL | Transistor-Transistor Logic |

## 15. Revision history

**Table 10. Revision history**

| Document ID | Release date | Data sheet status | Change notice | Supersedes |
|---|---|---|---|---|
| 74ABT16240A v.6 | 20111103 | Product data sheet | - | 74ABT16240A v.5 |
| Modifications: | • Legal pages updated | | | |
| 74ABT16240A v.5 | 20100525 | Product data sheet | - | 74ABT16240A v.4 |
| 74ABT16240A v.4 | 20090325 | Product data sheet | - | 74ABT16240A v.3 |
| 74ABT16240A v.3 | 20040212 | Product specification | 01-A15420 | 74ABT_H16240A v.2 |
| 74ABT_H16240A v.2 | 19980225 | Product specification | 853-1880 19019 | 74ABT_H16240A |
| 74ABT_H16240A | 19961001 | Product specification | - | - |

# 16. Legal information

## 16.1 Data sheet status

| Document status[1][2] | Product status[3] | Definition |
|---|---|---|
| Objective [short] data sheet | Development | This document contains data from the objective specification for product development. |
| Preliminary [short] data sheet | Qualification | This document contains data from the preliminary specification. |
| Product [short] data sheet | Production | This document contains the product specification. |

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

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