MWCT101XSF

MWCT101XS Data Sheet

Key Features

- Operating characteristics
  - Voltage range: 2.7 V to 5.5 V
  - Ambient temperature range: -40 °C to 105 °C for HSRUN, -40 °C to 125 °C for RUN
- Arm™ Cortex-M4F core, 32-bit CPU
  - Supports up to 112 MHz frequency (HSRUN) with 1.25 Dhrystone MIPS per MHz
  - Arm Core based on the Armv7 Architecture and Thumb®-2 ISA
  - Integrated Digital Signal Processor (DSP)
  - Configurable Nested Vectored Interrupt Controller (NVIC)
  - Single Precision Floating Point Unit (FPU)
- Clock interfaces
  - 4 - 40 MHz fast external oscillator (SOSC)
  - 48 MHz Fast Internal RC oscillator (FIRC)
  - 8 MHz Slow Internal RC oscillator (SIRC)
  - 128 kHz Low Power Oscillator (LPO)
  - Up to 112 MHz (HSRUN) System Phased Lock Loop (SPLL)
  - Up to 50 MHz DC external square wave input clock
  - Real Time Counter (RTC)
- Power management
  - Low-power Arm Cortex-M4F core with excellent energy efficiency
  - Power Management Controller (PMC) with multiple power modes: HSRUN, Run, Stop, VLPR, and VLPS
  - Supports peripheral specific clock gating. Only specific peripherals remain working in low power modes.
- Memory and memory interfaces
  - Up to 2 MB program flash memory with ECC
  - 64 KB FlexNVM for data flash memory with ECC and EEPROM emulation
  - Up to 256 KB SRAM with ECC
  - Up to 4 KB of FlexRAM for use as SRAM or EEPROM emulation
  - Up to 4 KB Code cache to minimize performance impact of memory access latencies
  - QuadSPI with HyperBus™ support
- Mixed-signal analog
  - Up to two 12-bit Analog-to-Digital Converter (ADC) with up to 32 channel analog inputs per module
  - One Analog Comparator (CMP) with internal 8-bit Digital to Analog Converter (DAC)
- Debug functionality
  - Serial Wire JTAG Debug Port (SWJ-DP) combines
  - Debug Watchpoint and Trace (DWT)
  - Instrumentation Trace Macrocell (ITM)
  - Test Port Interface Unit (TPIU)
  - Flash Patch and Breakpoint (FPB) Unit
- Human-machine interface (HMI)
  - Up to 156 GPIO pins with interrupt functionality
  - Non-Maskable Interrupt (NMI)
- Communications interfaces
  - Up to three Low Power Universal Asynchronous Receiver/Transmitter (LPUART) modules with DMA support and low power availability
  - Up to three Low Power Serial Peripheral Interface (LPSPI) modules with DMA support and low power availability
  - Up to two Low Power Inter-Integrated Circuit (LPI2C) modules with DMA support and low power availability
  - Up to three FlexCAN modules (with optional CAN-FD support)
  - FlexIO module for flexible and high performance serial interfaces
- Reliability, safety and security
  - HW Security Engine (CSEc)
  - Internal watchdog (WDOG)
  - External Watchdog monitor (EWM) module
  - Error-Correcting Code (ECC) on flash and SRAM memories
  - Cyclic Redundancy Check (CRC) module
  - 128-bit Unique Identification (ID) number
  - System Memory Protection Unit (System MPU)

- Timing and control
  - Up eight independent 16-bit FlexTimers (FTM) module, offering up to 64 standard channels (IC/OC/PWM)
  - One 16-bit Low Power Timer (LPTMR) with flexible wake up control
  - Two Programmable Delay Blocks (PDB) with flexible trigger system
  - One 32-bit Low Power Interrupt Timer (LPIT) with 4 channels
  - 32-bit Real Time Counter (RTC)
- I/O and package
  - 64-pin LQFP, 100-pin LQFP, 144-pin LQFP package options
- 16 channel DMA with up to 63 request sources using DMAMUX

Table of Contents

1 Block diagram

The figure below shows a superset high level architecture block diagram of the device. Other devices within the family have a subset of the features. See Feature comparison for chip specific values.

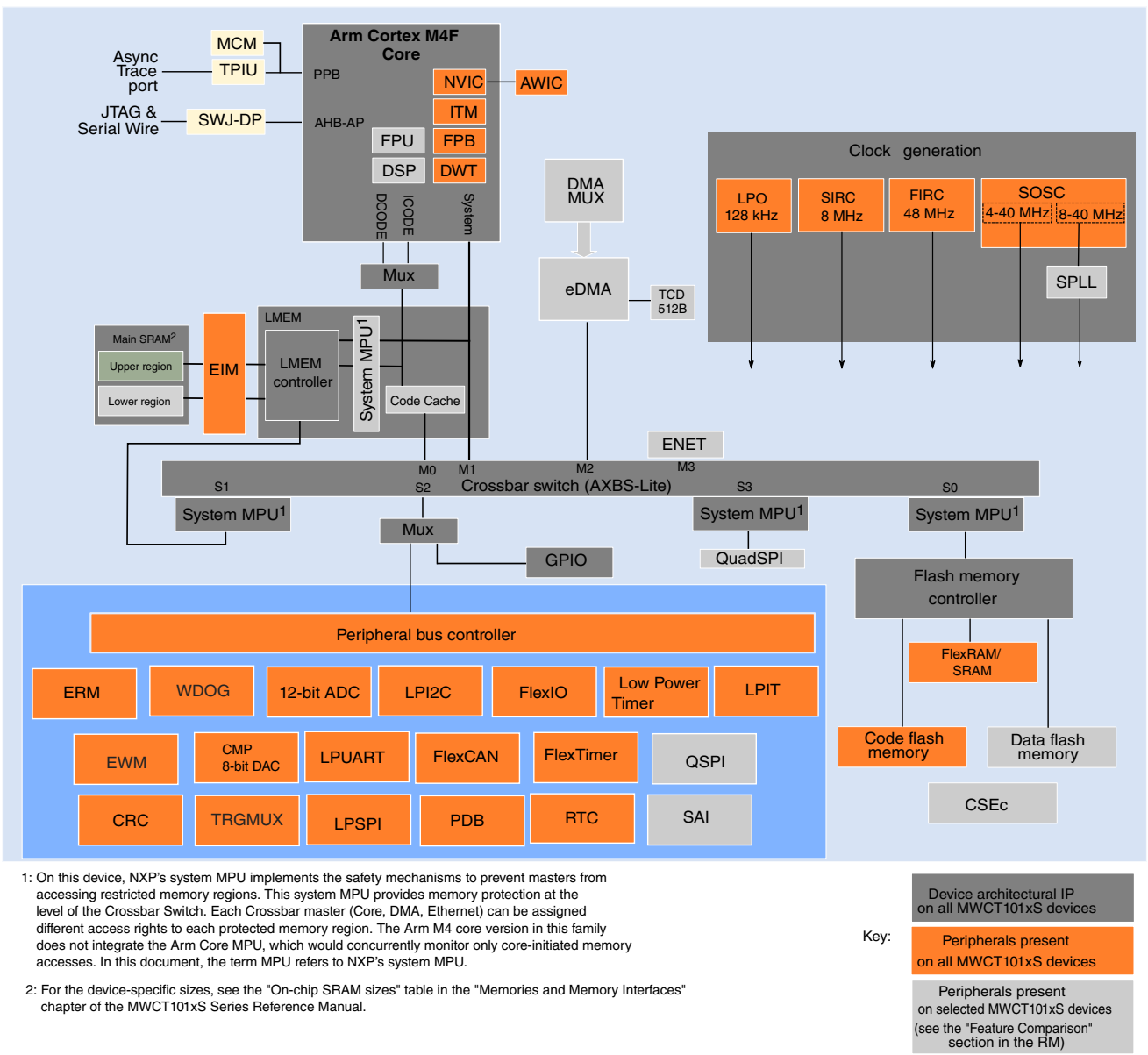


Figure 1. High-level architecture diagram for the MWCT101xS family

2 Feature comparison

The following figure summarizes the memory and package options for the MWCT101xS series and demonstrates where this device fits within the overall series. All devices which share a common package are pin-to-pin compatible.

Feature comparison

	Parameter	MWCT101xS		
		MWCT1014S	MWCT1015S	MWCT1016S
	Core	Arm® Cortex™-M4F		
	Frequency	up to 112 MHz (HSRUN)		
System	IEEE-754 FPU	●		
System	HW security module (CSEc)[1]	●		
System	CRC module	1x		
System	ISO 26262	capable up to ASIL-B		
System	Peripheral speed	up to 112 MHz (HSRUN)		
System	Crossbar	●		
System	DMA	●		
System	EWM	●		
System	Memory protection unit	●		
System	FIRC CMU	○		
System	Watchdog	1x		
System	Low power modes	●		
System	HSRUN mode	●		
System	Number of I/Os	up to 89	up to 128	up to 156
System	Single supply voltage	2.7 - 5.5 V		
System	Operating temperature (T_a) Temperature ambient	-40 to +105°C		
Memory	Flash	512 KB	1 MB	2 MB[2]
Memory	Error correction code (ECC)	●		
Memory	System RAM (including FlexRAM)	64 KB	128 KB	256 KB
Memory	FlexRAM (also available as system RAM)	4 KB		
Memory	Cache	4 KB		
Memory	EEPROM emulated by FlexRAM	4 KB (up to 64 KB D-Flash)		See footnote 3
Memory	External memory interface	○		QuadSPI incl. HyperBus™
Timer	Low power interrupt timer	1x		
Timer	FlexTimer (16-bit counter) 8 channels	4x (32)	6x (48)	8x (64)
Timer	Low power timer (LPTMR)	1x		
Timer	Real time counter (RTC)	1x		
Timer	Programmable delay block (PDB)	2x		
Analog	Trigger mux (TRGMUX)	1x (64)	1x (73)	1x (81)
Analog	12-bit SAR ADC (1 MSPS each)	2x (16)	2x (24)	2x (32)
Analog	Comparator with 8-bit DAC	1x		
Communication	100 Mbit IEEE-1588 ethernet MAC	○		1x
Communication	Serial audio interface (AC97, TDM, I2S)	○		2x
Communication	Low power UART/LIN (Supports LIN protocol versions 1.3, 2.0, 2.1, 2.2A and SAE J2602)	3x		
Communication	Low power SPI	3x		
Communication	Low power I2C	1x		2x
Communication	FlexCAN (CAN-FD ISO/CD 11898-1)	3x (1x with FD)	3x (2x with FD)	3x (3x with FD)
Communication	FlexIO (8 pins configurable as UART, SPI, I2C, I2S)	1x		
IDEs	Debug & trace	SWD, JTAG (ITM, SWV, SWO)		SWD, JTAG (ITM, SWV, SWO), ETM
IDEs	Ecosystem (IDE, compiler, debugger)	NXP S32 Design Studio (GCC) + SDK, IAR, GHS, COSMIC, Lauterbach, iSystems		
Other	Packages	LQFP-64 LQFP-100	LQFP-100	LQFP-144

LEGEND:
- ○ Not implemented
- ● Available on the device

1 No FTFC commands, including CSE commands (CSEc parts) are available when chip is in VLPR or HSRUN mode.
2 Available when EEEPROM, CSEc and Data Flash are not used. Else only up to 1,984 KB is available for Program Flash.
3 4 KB (up to 512 KB D-Flash as a part of 2M Flash). Up to 64 KB of flash is used as EEPROM backup and the remaining 448 KB of the last 512 KB block can be used as Data flash or Program flash. See chapter FTFC for details.

Figure 2. MWCT101xS product series comparison

3 Ordering parts

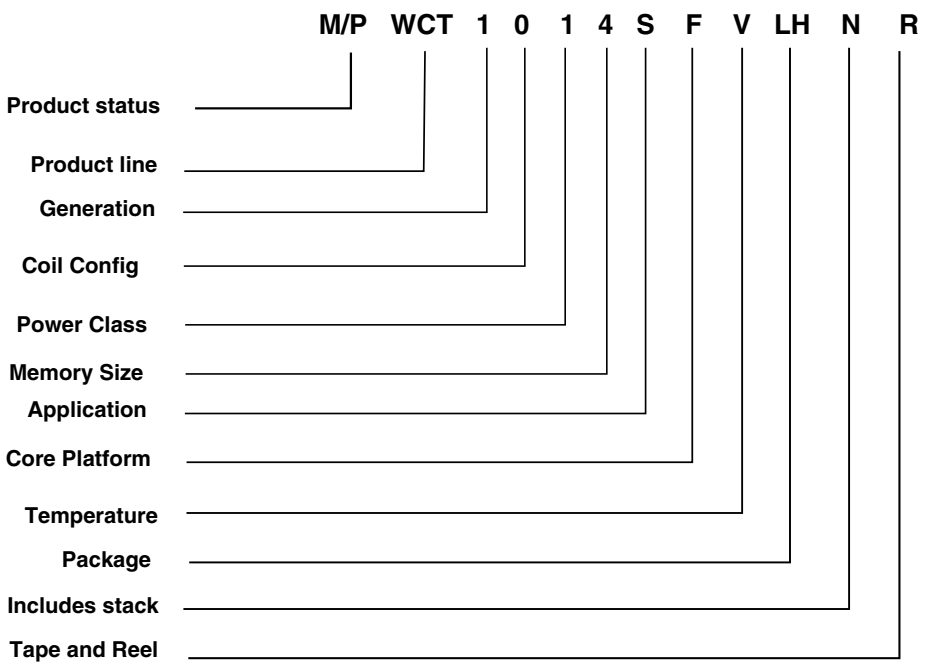
3.1 Determining valid orderable parts

To determine the orderable part numbers for this device, go to www.nxp.com and perform a part number search.

NOTE

Not all part number combinations exist

3.2 Ordering information



Product status
P: Pre Qualification
M: Fully Qualified

Product line
WCT: Wireless Charging Technology

Generation
1: 1st product Gen
2: 2nd product Gen

Coil config
0 = Standard
1 = Premium

Power Class
0 = 5 W
1 = 15 W
2 = 60 W
3 =200 W

Memory size (Flash)

	4	5	6
M0+		128 K	256 K
M4F	512 K	1 M	2 M

Application
Blank =Customer
A = Auto/Industr
S = A + AUTOSAR

Core platform
Z: Arm Cortex M0+
F: Arm Cortex M4F

Temperature
C: -40C to 85C
V: -40C to 105C
M: -40C to 125C

Package

Pins	LQFP	LQFP -EP	QFN	BGA
32	LC	-	FM	-
48	LF	KF	FT	-
64	LH	KH	-	-
100	LL	-	-	MH
144	LQ	-	-	-
176	LU	-	-	-

Includes stack
Blank = No stack
N = NFC

Tape and Reel
T: Trays and Tubes
R: Tape and Reel

Figure 3. Ordering information

4 General

4.1 Absolute maximum ratings

NOTE

Functional operating conditions appear in the DC electrical characteristics. Absolute maximum ratings are stress ratings only, and functional operation at the maximum values is not guaranteed. See footnotes in the following table for specific conditions.

Stress beyond the listed maximum values may affect device reliability or cause permanent damage to the device.

All the limits defined in the datasheet specification must be honored together and any violation to any one or more will not gaurantee desired operation.

Table 1. Absolute maximum ratings

Symbol	Parameter	Conditions[1]	Min	Max	Unit
V_{DD}[2]	2.7 V - 5. 5V input supply voltage	—	-0.3	5.8 [3]	V
V_{REFH}	3.3 V / 5.0 V ADC high reference voltage	—	-0.3	5.8 [3]	V
$I_{INJPAD\_DC\_ABS}$[4]	Continuous DC input current (positive / negative) that can be injected into an I/O pin	—	-3	+3	mA
V_{IN_DC}	Continuous DC Voltage on any I/O pin with respect to V_{SS}	—	-0.8	5.8[5]	V
$I_{INJSUM\_DC\_ABS}$	Sum of absolute value of injected currents on all the pins (Continuous DC limit)	—	—	30	mA
T_{ramp}[6]	Supply ramp rate	—	0.5 V/min	500 V/ms	—
T_A[7]	Ambient temperature	—	-40	125	°C
T_{STG}	Storage temperature	—	-55	165	°C
$V_{IN\_TRANSIENT}$	Transient overshoot voltage allowed on I/O pin beyond $V_{IN\_DC\ limit}$	—	—	6.8 [8]	V

1. All voltages are referred to V_{SS} unless otherwise specified.
2. As V_{DD} varies between the minimum value and the absolute maximum value the analog characteristics of the I/O and the ADC will both change. See section I/O parameters and ADC electrical specifications respectively for details.
3. 60 s lifetime – No restrictions i.e. The part can switch.

   10 hours lifetime – Device in reset i.e. The part cannot switch.
4. When input pad voltage levels are close to V_{DD} or V_{SS}, practically no current injection is possible.
5. While respecting the maximum current injection limit
6. Limit applies to both maximum absolute maximum ramp rate and typical operating conditions.
7. T_J (Junction temperature)=135 °C. Assumes T_A=125 °C for RUN mode

T_J (Junction temperature)=125 °C. Assumes TA=105 °C for HSRUN mode

- Assumes maximum θJA for 2s2p board. See Thermal characteristics

8. 60 seconds lifetime; device in reset (no outputs enabled/toggling)

4.2 Voltage and current operating requirements

NOTE

Full functionality/specifications cannot be guaranteed when voltage drops below 2.7 V.

Table 2. Voltage and current operating requirements [1]

Symbol	Description	Min.	Max.	Unit	Notes
V_{DD}[2]	Supply voltage	2.7[3]	5.5	V	4
V_{DD_OFF}	Voltage allowed to be developed on V_{DD} pin when it is not powered from any external power supply source.	0	0.1	V	
V_{DDA}	Analog supply voltage	2.7	5.5	V	4
$V_{DD} – V_{DDA}$	V_{DD}-to-V_{DDA} differential voltage	– 0.1	0.1	V	
V_{REFH}	ADC reference voltage high	2.7	V_{DDA} + 0.1	V	5
V_{REFL}	ADC reference voltage low	-0.1	0.1	V	
V_{ODPU}	Open drain pullup voltage level	V_{DD}	V_{DD}	V	6
$I_{INJPAD\_DC\_OP}$[7]	Continuous DC input current (positive / negative) that can be injected into an I/O pin	-3	+3	mA	
$I_{INJSUM\_DC\_OP}$	Continuous total DC input current that can be injected across all I/O pins such that there's no degradation in accuracy of analog modules: ADC and ACMP (See section Analog Modules)	—	30	mA	

1. Typical conditions assumes V_{DD} = V_{DDA} = V_{REFH} = 5 V, temperature = 25 °C and typical silicon process unless otherwise stated.
2. As V_{DD} varies between the minimum value and the absolute maximum value the analog characteristics of the I/O and the ADC will both change. See section I/O parameters and ADC electrical specifications respectively for details.
3. MWCT1016S will operate from 2.7 V when executing from internal FIRC. When the PLL is engaged MWCT1016S is guaranteed to operate from 2.97 V. All other MWCT101xS family devices operate from 2.7 V in all modes.
4. V_{DD} and V_{DDA} must be shorted to a common source on PCB. Appropriate decap to be used to filter noise on V_{DDA}. See application note AN5032 for reference supply design for SAR ADC.
5. V_{REFH} should always be equal to or less than V_{DDA} + 0.1 V and V_{DD} + 0.1 V
6. Open drain outputs must be pulled to V_{DD}.
7. When input pad voltage levels are close to V_{DD} or V_{SS}, practically no current injection is possible.

4.3 Thermal operating characteristics

Table 3. Thermal operating characteristics for 64 LQFP and 100 LQFP packages.

Symbol	Parameter	Value			Unit
		Min.	Typ.	Max.	
$T_{A\ C\text{-}Grade\ Part}$	Ambient temperature under bias	–40	—	85[1]	°C
$T_{J\ C\text{-}Grade\ Part}$	Junction temperature under bias	–40	—	105[1]	°C
$T_{A\ V\text{-}Grade\ Part}$	Ambient temperature under bias	–40	—	105[1]	°C
$T_{J\ V\text{-}Grade\ Part}$	Junction temperature under bias	–40	—	125[1]	°C
$T_{A\ M\text{-}Grade\ Part}$	Ambient temperature under bias	–40	—	125[2]	°C
$T_{J\ M\text{-}Grade\ Part}$	Junction temperature under bias	–40	—	135[2]	°C

1. Values mentioned are measured at ≤ 112 MHz in HSRUN mode.
2. Values mentioned are measured at ≤ 80 MHz in RUN mode.

4.4 Power and ground pins

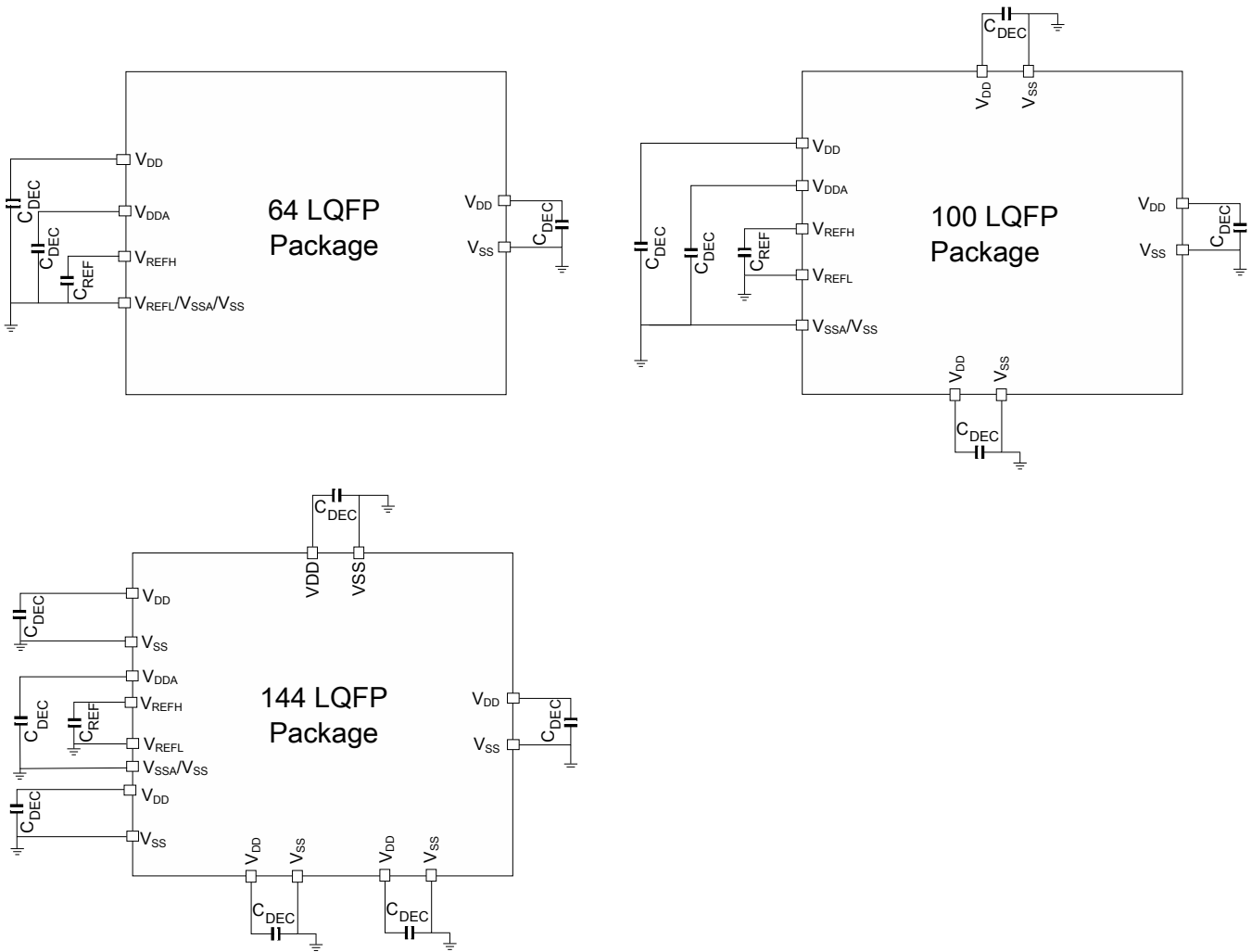


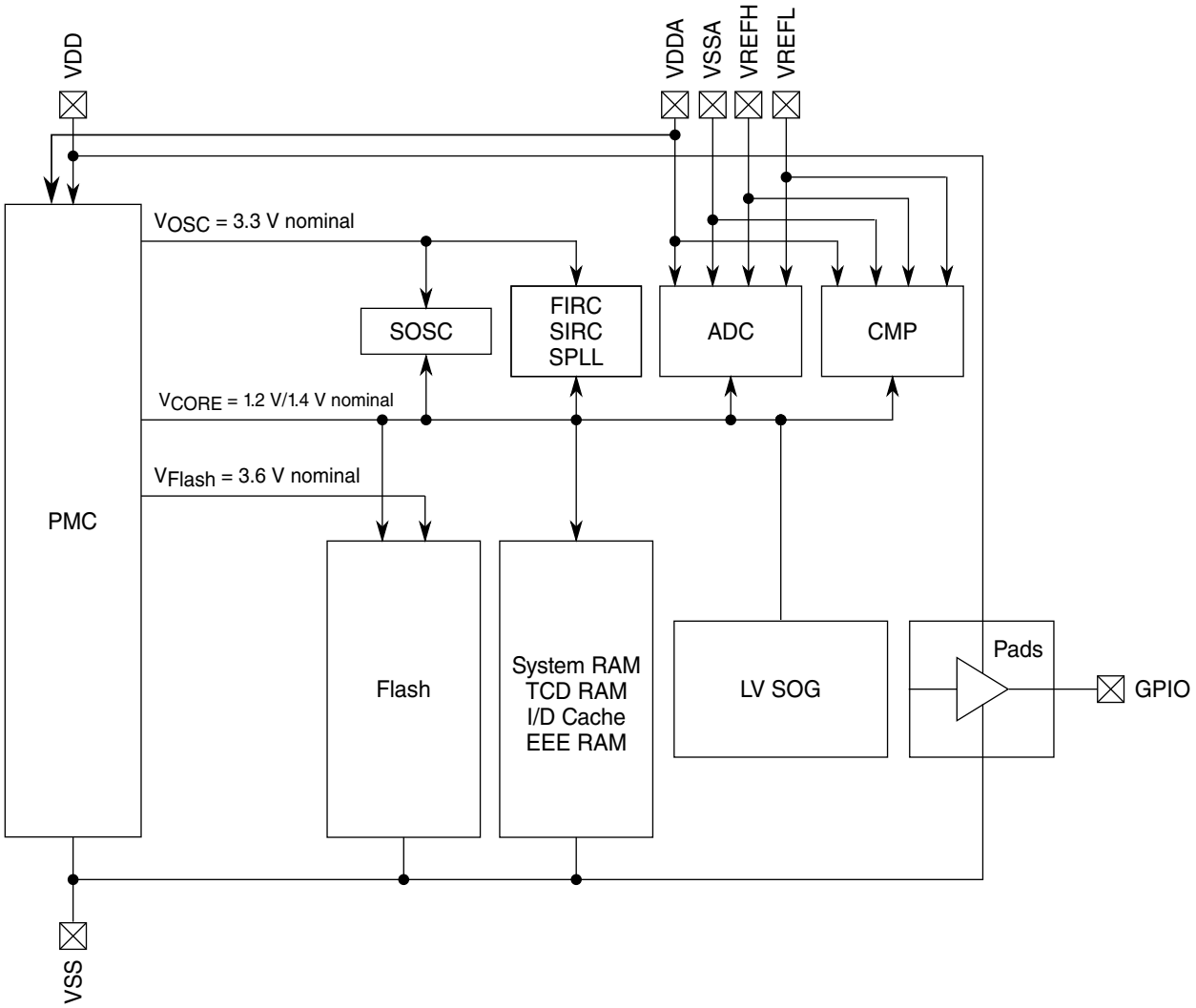
Figure 4. Pinout decoupling

Table 4. Supplies decoupling capacitors 1, 2

Symbol	Description	Min. [3]	Typ.	Max.	Unit
C_{REF} [4, 5]	ADC reference high decoupling capacitance	70	100	—	nF
C_{DEC} [5, 6, 7]	Recommended decoupling capacitance	70	100	—	nF

1. V_{DD} and V_{DDA} must be shorted to a common source on PCB. Appropriate decoupling capacitors to be used to filter noise on the supplies. See application note AN5032 for reference supply design for SAR ADC. All V_{SS} pins should be connected to common ground at the PCB level.
2. All decoupling capacitors must be low ESR ceramic capacitors (for example X7R type).
3. Minimum recommendation is after considering component aging and tolerance.
4. For improved performance, it is recommended to use 10 µF, 0.1 µF and 1 nF capacitors in parallel.
5. All decoupling capacitors should be placed as close as possible to the corresponding supply and ground pins.
6. Contact your local Field Applications Engineer for details on best analog routing practices.
7. The filtering used for decoupling the device supplies must comply with the following best practices rules:
   - The protection/decoupling capacitors must be on the path of the trace connected to that component.

- No trace exceeding 1 mm from the protection to the trace or to the ground.
- The protection/decoupling capacitors must be as close as possible to the input pin of the device (maximum 2 mm).
- The ground of the protection is connected as short as possible to the ground plane under the integrated circuit.



*Note: VSSA and VSS are shorted at package level

Figure 5. Power diagram

4.5 LVR, LVD and POR operating requirements

Table 5. V_{DD} supply LVR, LVD and POR operating requirements

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
V_{POR}	Rising and falling V_{DD} POR detect voltage	1.1	1.6	2.0	V	
V_{LVR}	LVR falling threshold (RUN, HSRUN, and STOP modes)	2.50	2.58	2.7	V	
V_{LVR_HYST}	LVR hysteresis	—	45	—	mV	1
V_{LVR_LP}	LVR falling threshold (VLPS/VLPR modes)	1.97	2.22	2.44	V	

Table continues on the next page...

Table 5. V_{DD} supply LVR, LVD and POR operating requirements (continued)

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
V_{LVD}	Falling low-voltage detect threshold	2.8	2.875	3	V	
V_{LVD_HYST}	LVD hysteresis	—	50	—	mV	1
V_{LVW}	Falling low-voltage warning threshold	4.19	4.305	4.5	V	
V_{LVW_HYST}	LVW hysteresis	—	75	—	mV	1
V_{BG}	Bandgap voltage reference	0.97	1.00	1.03	V	

1. Rising threshold is the sum of falling threshold and hysteresis voltage.

4.6 Power mode transition operating behaviors

All specifications in the following table assume this clock configuration:

- RUN Mode:
  - Clock source: FIRC
  - SYS_CLK/CORE_CLK = 48 MHz
  - BUS_CLK = 48 MHz
  - FLASH_CLK = 24 MHz
- HSRUN Mode:
  - Clock source: SPLL
  - SYS_CLK/CORE_CLK = 112 MHz
  - BUS_CLK = 56 MHz
  - FLASH_CLK = 28 MHz
- VLPR Mode:
  - Clock source: SIRC
  - SYS_CLK/CORE_CLK = 4 MHz
  - BUS_CLK = 4 MHz
  - FLASH_CLK = 1 MHz
- STOP1/STOP2 Mode:
  - Clock source: FIRC
  - SYS_CLK/CORE_CLK = 48 MHz
  - BUS_CLK = 48 MHz
  - FLASH_CLK = 24 MHz
- VLPS Mode: All clock sources disabled.

Table 6. Power mode transition operating behaviors

Symbol	Description	Min.	Typ.	Max.	Unit
t_{POR}	After a POR event, amount of time from the point V_{DD} reaches 2.7 V to execution of the first instruction across the operating temperature range of the chip.	—	325	—	µs

Table continues on the next page...

Table 6. Power mode transition operating behaviors (continued)

Symbol	Description	Min.	Typ.	Max.	Unit
	VLPS → RUN	8	—	17	µs
	STOP1 → RUN	0.07	0.075	0.08	µs
	STOP2 → RUN	0.07	0.075	0.08	µs
	VLPR → RUN	19	—	26	µs
	VLPR → VLPS	5.75	6.25	6.5	µs
	VLPS → VLPR	26.5	27.25	27.75	µs
	RUN → Compute operation	0.72	0.75	0.77	µs
	HSRUN → Compute operation	0.3	0.31	0.35	µs
	RUN → STOP1	0.35	0.38	0.4	µs
	RUN → STOP2	0.2	0.23	0.25	µs
	RUN → VLPS	0.35	0.38	0.4	µs
	RUN → VLPR	4.4	4.7	5	µs
	VLPS → Asynchronous DMA Wakeup	105	110	125	µs
	STOP1 → Asynchronous DMA Wakeup	1	1.1	1.3	µs
	STOP2 → Asynchronous DMA Wakeup	1	1.1	1.3	µs
	Pin reset → Code execution	—	214	—	µs

NOTE

HSRUN should only be used when frequencies in excess of 80 MHz are required. When using 80 MHz and below, RUN mode is the recommended operating mode.

4.7 Power consumption

The following table shows the power consumption targets for the device in various mode of operations.

Table 7. Power consumption (Typicals unless stated otherwise) 1

	Ambient Temperature (°C)		VLPS (µA)[2, 3]		VLPR (mA)		STOP1 (mA)	STOP2 (mA)	RUN@48 MHz (mA)		RUN@64 MHz (mA)		RUN@80 MHz (mA)		HSRUN@112 MHz (mA) [4]		Idd/MHz (µA/MHz)[5]
			Peripherals disabled [6]	Peripherals enabled	Peripherals disabled	Peripherals enabled			Peripherals disabled	Peripherals enabled	Peripherals disabled	Peripherals enabled	Peripherals disabled	Peripherals enabled	Peripherals disabled	Peripherals enabled	
MWCT1014S	25	Typ	29.8	39.1	1.48	1.50	7	7.7	19.7	26.9	25.1	33.3	30.2	39.6	43.3	55.6	378
	85	Typ	150	159	1.72	1.85	7.2	8.1	20.4	27.1	26.1	33.5	30.5	40	43.9	56.1	381
		Max	359	384	2.60	2.65	8.3	9.2	21.9	28.5	27.8	34.4	32.9	41.5	45.5	57.5	411
	105	Typ	256	273	1.80	2.10	7.8	8.5	20.6	27.4	26.6	33.8	31.2	40.5	44.8	57.1	390
		Max	850	900	2.65	2.70	10.3	10.6	22.7	30	28.3	36.5	33.4	43.3	47.9	61.3	418
	125	Max	1960	1998	3.18	3.25	12.2	13	25.3	32.7	35	39.8	37.1	46.5	NA	NA	464
MWCT1015S	25	Typ	40	55	5	6	15	20	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD
	105	Typ	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD
		Max	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	95	110	TBD
	125	Max	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	70	80	NA	NA	TBD
MWCT1016S[7, 8]	25	Typ	40	60	5	6	15	20	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD
	105	Typ	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD
		Max	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	120	125	TBD
	125	Max	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	100	110	NA	NA	TBD

1. Typical current numbers are indicative for typical silicon process and may vary based on the silicon distribution and user configuration.
2. This is an average based on the use case described in the Comparator section, whereby the analog sampling is taking place periodically, with a mechanism to only enable the DAC as required. The numbers quoted assumes that only a single ANLCMP is active and the others are disabled
3. Current numbers are for reduced configuration and may vary based on user configuration and silicon process variation.
4. HSRUN mode must not be used at 125°C. Max ambient temperature for HSRUN mode is 105°C.
5. Values mentioned are measured at 25 °C at RUN@80 MHz with peripherals disabled.
6. With PMC_REGSC[CLKBIASDIS] set to 1. See Reference Manual for details.
7. Above MWCT1016S data is preliminary targets only
8. The MWCT1016S data points assume that ENET/QuadSPI/SAI etc. are active. If the same configuration is selected as per the MWCT1014S, then the two devices will have very similar IDD.

4.7.1 Modes configuration

Attached *MWCT101xS_Power_Modes _Configuration.xlsx* details the modes used in gathering the power consumption data stated in the above table Table 7. For full functionality refer to table: Module operation in available low power modes of the *Reference Manual*.

4.8 ESD handling ratings

Symbol	Description	Min.	Max.	Unit	Notes
V_{HBM}	Electrostatic discharge voltage, human body model	– 4000	4000	V	1
V_{CDM}	Electrostatic discharge voltage, charged-device model				2
	All pins except the corner pins	– 500	500	V	
	Corner pins only	– 750	750	V	
I_{LAT}	Latch-up current at ambient temperature of 125 °C	– 100	100	mA	3

1. Determined according to JEDEC Standard JESD22-A114, *Electrostatic Discharge (ESD) Sensitivity Testing Human Body Model (HBM)*.
2. Determined according to JEDEC Standard JESD22-C101, *Field-Induced Charged-Device Model Test Method for Electrostatic-Discharge-Withstand Thresholds of Microelectronic Components*.
3. Determined according to JEDEC Standard JESD78, *IC Latch-Up Test*.

4.9 EMC radiated emissions operating behaviors

EMC measurements to IC-level IEC standards are available from NXP on request.

5 I/O parameters

5.1 AC electrical characteristics

Unless otherwise specified, propagation delays are measured from the 50% to the 50% point, and rise and fall times are measured at the 20% and 80% points, as shown in the following figure.

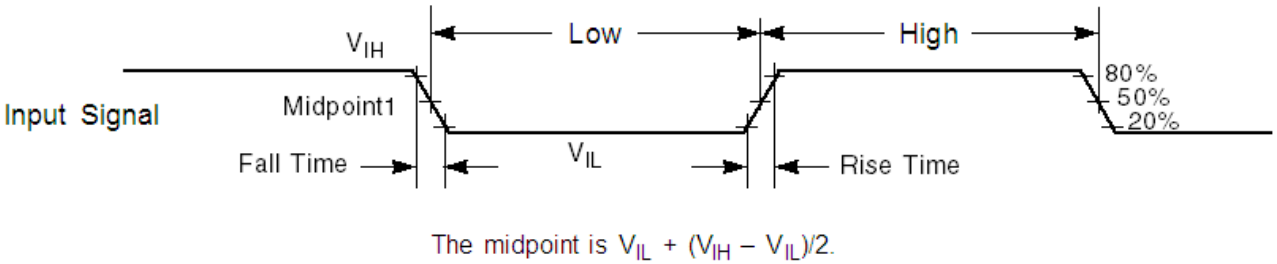


Figure 6. Input signal measurement reference

5.2 General AC specifications

These general purpose specifications apply to all signals configured for GPIO, UART, and timers.

Table 8. General switching specifications

Symbol	Description	Min.	Max.	Unit	Notes
	GPIO pin interrupt pulse width (digital glitch filter disabled) — Synchronous path	1.5	—	Bus clock cycles	1, 2
	GPIO pin interrupt pulse width (digital glitch filter disabled, passive filter disabled) — Asynchronous path	50	—	ns	3
WFRST	$\overline{\text{RESET}}$ input filtered pulse	—	100	ns	4
WFRST	$\overline{\text{RESET}}$ input not filtered pulse	100	—	ns	

1. This is the minimum pulse width that is guaranteed to pass through the pin synchronization circuitry. Shorter pulses may or may not be recognized. In Stop and VLPS modes, the synchronizer is bypassed so shorter pulses can be recognized in that case.
2. The greater of synchronous and asynchronous timing must be met.
3. These pins do not have a passive filter on the inputs. This is the shortest pulse width that is guaranteed to be recognized.
4. Minimum length of $\overline{\text{RESET}}$ pulse, guaranteed not to be filtered by the internal filter.

5.3 DC electrical specifications at 3.3 V Range

Table 9. DC electrical specifications at 3.3 V Range

Symbol	Parameter	Value			Unit	Notes
		Min.	Typ.	Max.		
V_{DD}	I/O Supply Voltage	2.7	3.3	4	V	1
V_{ih}	Input Buffer High Voltage	0.7 × V_{DD}	—	V_{DD} + 0.3	V	2
V_{il}	Input Buffer Low Voltage	V_{SS} – 0.3	—	0.3 × V_{DD}	V	3
V_{hys}	Input Buffer Hysteresis	0.06 × V_{DD}	—	—	V	
Ioh_Standard	I/O current source capability measured when pad = (V_{DDE} – 0.8 V)	3.5	—	—	mA	

Table continues on the next page...

Table 9. DC electrical specifications at 3.3 V Range (continued)

Symbol	Parameter	Value			Unit	Notes
		Min.	Typ.	Max.		
Iol_Standard	I/O current sink capability measured when pad = 0.8 V	3	—	—	mA	
Ioh_Strong	I/O current source capability measured when pad = (V_{DDE} – 0.8 V)	14	—	—	mA	4
Iol_Strong	I/O current sink capability measured when pad = 0.8 V	12	—	—	mA	5
IOHT	Output high current total for all ports	—	—	100	mA	
IIN	Input leakage current (per pin) for full temperature range at V_{DD} = 3.3 V					6
	All pins other than high drive port pins		0.005	0.5	µA	
	High drive port pins [7]		0.010	0.5	µA	
R_{PU}	Internal pullup resistors	20		60	kΩ	8
R_{PD}	Internal pulldown resistors	20		60	kΩ	9

1. MWCT1016S will operate from 2.7 V when executing from internal FIRC. When the PLL is engaged MWCT1016S is guaranteed to operate from 2.97 V. All other MWCT101xS family devices operate from 2.7 V in all modes.
2. For reset pads, same V_{ih} levels are applicable
3. For reset pads, same V_{il} levels are applicable
4. The value given is measured at high drive strength mode. For value at low drive strength mode see the Ioh_Standard value given above.
5. The value given is measured at high drive strength mode. For value at low drive strength mode see the Iol_Standard value given above.
6. Several I/O have both high drive and normal drive capability selected by the associated Portx_PCRn[DSE] control bit. All other GPIOs are normal drive only. For details refer to *MWCT101xS_IO_Signal_Description_Input_Multiplexing.xlsx* attached with the *Reference Manual*.
7. When using ENET and SAI on MWCT1016S, the overall device limits associated with high drive pin configurations must be respected i.e. On 144-pin LQFP the general purpose pins: PTA10, PTD0, and PTE4 must be set to low drive.
8. Measured at input V = V_{SS}
9. Measured at input V = V_{DD}

5.4 DC electrical specifications at 5.0 V Range

Table 10. DC electrical specifications at 5.0 V Range

Symbol	Parameter	Value			Unit	Notes
		Min.	Typ.	Max.		
V_{DD}	I/O Supply Voltage	4	—	5.5	V	
V_{ih}	Input Buffer High Voltage	0.65 x V_{DD}	—	V_{DD} + 0.3	V	1
V_{il}	Input Buffer Low Voltage	V_{SS} – 0.3	—	0.35 x V_{DD}	V	2
V_{hys}	Input Buffer Hysteresis	0.06 x V_{DD}	—	—	V	
Ioh_Standard	I/O current source capability measured when pad = (V_{DDE} - 0.8 V)	5	—	—	mA	
Iol_Standard	I/O current sink capability measured when pad = 0.8 V	5	—	—	mA	

Table continues on the next page...

Table 10. DC electrical specifications at 5.0 V Range (continued)

Symbol	Parameter	Value			Unit	Notes
		Min.	Typ.	Max.		
Ioh_Strong	I/O current source capability measured when pad = V_{DDE} - 0.8 V	20	—	—	mA	3, 4
Iol_Strong	I/O current sink capability measured when pad = 0.8 V	20	—	—	mA	4, 5
IOHT	Output high current total for all ports	—	—	100	mA	
IIN	Input leakage current (per pin) for full temperature range at V_{DD} = 5.5 V					6
	All pins other than high drive port pins		0.005	0.5	µA	
	High drive port pins		0.010	0.5	µA	
R_{PU}	Internal pullup resistors	20		50	kΩ	7
R_{PD}	Internal pulldown resistors	20		50	kΩ	8

1. For reset pads, same V_{ih} levels are applicable
2. For reset pads, same V_{il} levels are applicable
3. The value given is measured at high drive strength mode. For value at low drive strength mode see the Ioh_Standard value given above.
4. The strong pad I/O pin is capable of switching a 50 pF load at up to 40 MHz.
5. The value given is measured at high drive strength mode. For value at low drive strength mode see the Iol_Standard value given above.
6. Several I/O have both high drive and normal drive capability selected by the associated Portx_PCRn[DSE] control bit. All other GPIOs are normal drive only. For details refer to *MWCT101xS_IO_Signal_Description_Input_Multiplexing.xlsx* attached with the *Reference Manual*.
7. Measured at input V = V_{SS}
8. Measured at input V = V_{DD}

5.5 AC electrical specifications at 3.3 V range

Table 11. AC electrical specifications at 3.3 V Range

Symbol	DSE	Rise time (nS) [1]		Fall time (nS) [1]		Capacitance (pF) [2]
		Min.	Max.	Min.	Max.	
Standard	NA	4.6	14.5	3.9	15.7	25
		7.2	23.7	6.2	26.2	50
		24.0	75.4	20.8	88.4	200
Strong	0	4.6	14.5	3.9	15.7	25
		7.2	23.7	6.2	26.2	50
		24.0	75.4	20.8	88.4	200
	1	2.0	5.8	1.8	6.1	25
		2.8	8.0	2.6	8.3	50
		7.0	20.7	6.0	22.4	200

1. For reference only. Run simulations with the IBIS model and your custom board for accurate results.
2. Maximum capacitances supported on Standard IOs. However interface or protocol specific specifications might be different, for example for ENET, QSPI etc. . For protocol specific AC specifications, see respective sections.

5.6 AC electrical specifications at 5 V range

Table 12. AC electrical specifications at 5 V Range

Symbol	DSE	Rise time (nS)[1]		Fall time (nS) [1]		Capacitance (pF) [2]
		Min.	Max .	Min.	Max.	
Standard	NA	3.2	9.4	3.6	10.7	25
		5.4	15.7	5.1	17.4	50
		18.5	52.6	17.6	59.7	200
Strong	0	4.0	9.4	3.6	10.7	25
		5.8	15.7	5.1	17.4	50
		18.1	52.6	17.6	59.7	200
	1	1.6	4.6	1.5	5.0	25
		2.2	5.7	2.2	5.8	50
		5.6	14.6	5.0	15.4	200

1. For reference only. Run simulations with the IBIS model and your custom board for accurate results.
2. Maximum capacitances supported on Standard IOs. However interface or protocol specific specifications might be different, for example for ENET, QSPI etc. . For protocol specific AC specifications, see respective sections.

5.7 Standard input pin capacitance

Table 13. Standard input pin capacitance

Symbol	Description	Min.	Max.	Unit
C_{IN_D}	Input capacitance: digital pins	—	7	pF

NOTE

Please refer to External System Oscillator electrical specifications for EXTAL/XTAL pins.

5.8 Device clock specifications

Table 14. Device clock specifications [1]

Symbol	Description	Min.	Max.	Unit
High Speed run mode[2]				
f_{SYS}	System and core clock	—	112	MHz
f_{BUS}	Bus clock	—	56	MHz
f_{FLASH}	Flash clock	—	28	MHz
Normal run mode (MWCT101xS series) [3]				

Table continues on the next page...

Table 14. Device clock specifications 1 (continued)

Symbol	Description	Min.	Max.	Unit
f_{SYS}	System and core clock	—	80	MHz
f_{BUS}	Bus clock	—	40	MHz
f_{FLASH}	Flash clock	—	26.67	MHz
VLPR mode[4]				
f_{SYS}	System and core clock	—	4	MHz
f_{BUS}	Bus clock	—	4	MHz
f_{FLASH}	Flash clock	—	1	MHz
f_{ERCLK}	External reference clock	—	16	MHz

1. Refer to the section Feature comparison for the availability of modes and other specifications.
2. Only available on some devices. See section Feature comparison.
3. With SPLL as system clock source.
4. The frequency limitations in VLPR mode here override any frequency specification listed in the timing specification for any other module.

6 Peripheral operating requirements and behaviors

6.1 System modules

There are no electrical specifications necessary for the device's system modules.

6.2 Clock interface modules

6.2.1 External System Oscillator electrical specifications

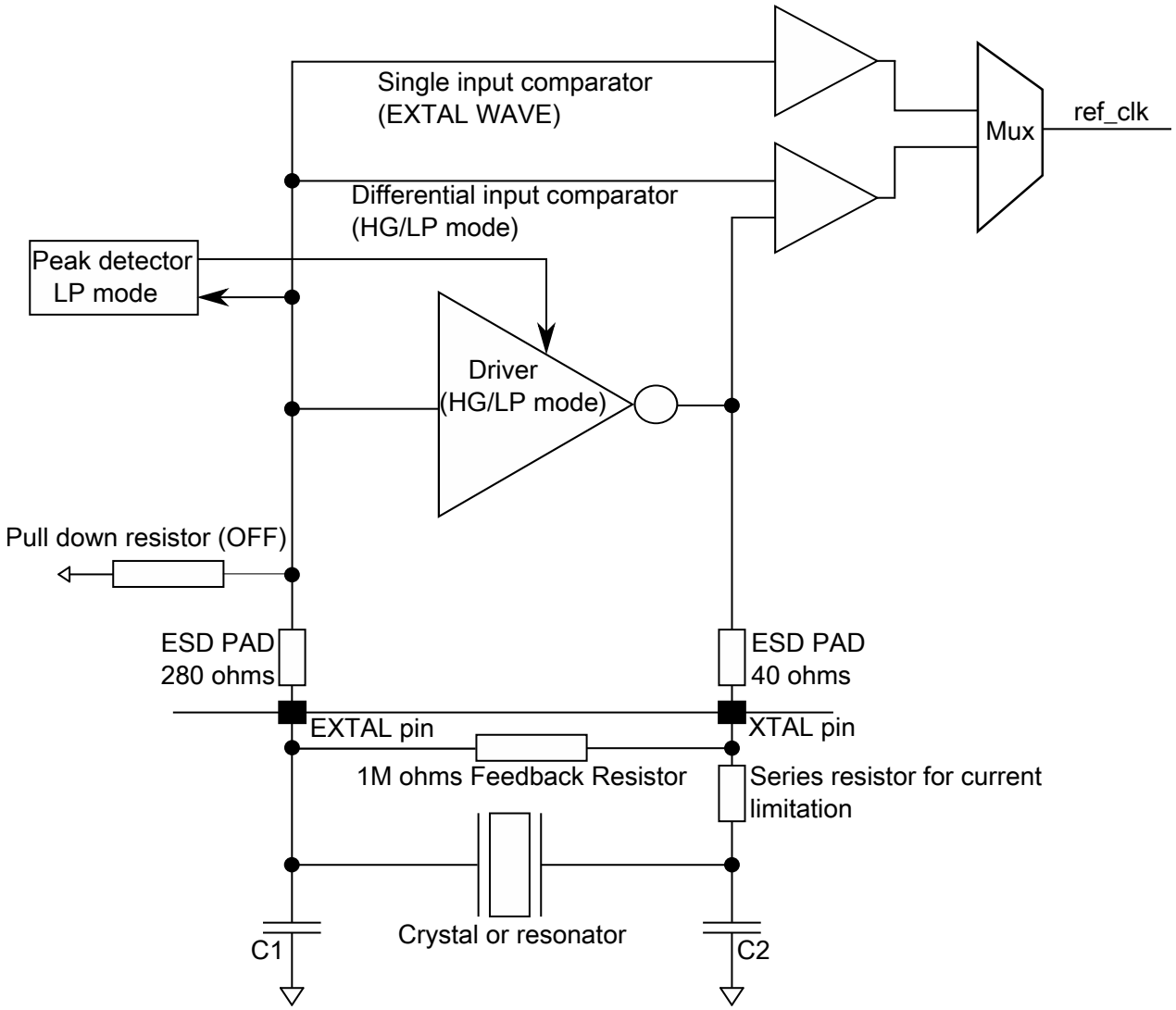


Figure 7. Oscillator connections scheme

Table 15. External System Oscillator electrical specifications

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
g_{mXOSC}	Crystal oscillator transconductance					
	4-8 MHz	2.2	—	13.7	mA/V	
	8-40 MHz	16	—	47	mA/V	
V_{IL}	Input low voltage — EXTAL pin in external clock mode	V_{SS}	—	0.35 * V_{DD}	V	
V_{IH}	Input high voltage — EXTAL pin in external clock mode	0.7 * V_{DD}	—	V_{DD}	V	
C_1	EXTAL load capacitance	—	—	—		1
C_2	XTAL load capacitance	—	—	—		1
R_F	Feedback resistor					2
	Low-gain mode (HGO=0)	—	—	—	MΩ	

Table continues on the next page...

Table 15. External System Oscillator electrical specifications (continued)

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
	High-gain mode (HGO=1)	—	1	—	MΩ	
R_S	Series resistor					
	Low-gain mode (HGO=0)	—	0	—	kΩ	
	High-gain mode (HGO=1)	—	0	—	kΩ	
V_{pp}	Peak-to-peak amplitude of oscillation (oscillator mode)					3
	Low-gain mode (HGO=0)	—	1.0	—	V	
	High-gain mode (HGO=1)	—	3.3	—	V	

1. Crystal oscillator circuit provides stable oscillations when g_{mXOSC} > 5 * gm_crit. The gm_crit is defined as:

   gm_crit = 4 * ESR * $(2\pi F)^2$ * $(C_0 + C_L)^2$

   where:

   - g_{mXOSC} is the transconductance of the internal oscillator circuit
   - ESR is the equivalent series resistance of the external crystal
   - F is the external crystal oscillation frequency
   - C_0 is the shunt capacitance of the external crystal
   - C_L is the external crystal total load capacitance. $C_L = C_s + [C_1 * C_2/(C_1+C_2)]$
   - C_s is stray or parasitic capacitance on the pin due to any PCB traces
   - C_1, C_2 external load capacitances on EXTAL and XTAL pins

   See manufacture datasheet for external crystal component values
2. - When low-gain is selected, internal R_F will be selected and external R_F should not be attached.
   - When high-gain is selected, external R_F (1 M Ohm) needs to be connected for proper operation of the crystal. For external resistor, up to 5% tolerance is allowed.
3. The EXTAL and XTAL pins should only be connected to required oscillator components and must not be connected to any other devices.

6.2.2 External System Oscillator frequency specifications

Table 16. External System Oscillator frequency specifications

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
f_{osc_hi}	Oscillator crystal or resonator frequency	4	—	40	MHz	
f_{ec_extal}	Input clock frequency (external clock mode)	—	—	50	MHz	
t_{dc_extal}	Input clock duty cycle (external clock mode)	40	50	60	%	
t_{cst}	Crystal Start-up Time					
	8 MHz low-gain mode (HGO=0)	—	1.5	—	ms	1
	8 MHz high-gain mode (HGO=1)	—	2.5	—		
	40 MHz low-gain mode (HGO=0)	—	2	—		
	40 MHz high-gain mode (HGO=1)	—	2	—		

1. Proper PC board layout procedures must be followed to achieve specifications.

6.2.3 System Clock Generation (SCG) specifications

6.2.3.1 Fast internal RC Oscillator (FIRC) electrical specifications

Table 17. Fast internal RC Oscillator electrical specifications

Symbol	Parameter[1]	Value			Unit
		Min.	Typ.	Max.	
F_{FIRC}	FIRC target frequency	—	48	—	MHz
ΔF	Frequency deviation across process, voltage, and temperature < 105°C	—	±0.5	±1	$\%F_{FIRC}$
ΔF125	Frequency deviation across process, voltage, and temperature < 125°C	—	±0.5	±1.1	$\%F_{FIRC}$
$T_{Startup}$	Startup time		3.4	5	µs[2]
T_{JIT}, [3]	Cycle-to-Cycle jitter	—	250	500	ps
T_{JIT}[3]	Long term jitter over 1000 cycles	—	0.04	0.1	$\%F_{FIRC}$

1. With FIRC regulator enable
2. Startup time is defined as the time between clock enablement and clock availability for system use.
3. FIRC as system clock

NOTE

Fast internal RC Oscillator is compliant with CAN and LIN standards.

6.2.3.2 Slow internal RC oscillator (SIRC) electrical specifications

Table 18. Slow internal RC oscillator (SIRC) electrical specifications

Symbol	Parameter	Value			Unit
		Min.	Typ.	Max.	
F_{SIRC}	SIRC target frequency	—	8	—	MHz
ΔF	Frequency deviation across process, voltage, and temperature < 105°C	—	—	±3	$\%F_{SIRC}$
ΔF125	Frequency deviation across process, voltage, and temperature < 125°C	—	—	±3.3	$\%F_{SIRC}$
$T_{Startup}$	Startup time	—	9	12.5	µs[1]

1. Startup time is defined as the time between clock enablement and clock availability for system use.

6.2.4 Low Power Oscillator (LPO) electrical specifications

Table 19. Low Power Oscillator (LPO) electrical specifications

Symbol	Parameter	Min.	Typ.	Max.	Unit
F_{LPO}	Internal low power oscillator frequency	113	128	139	kHz
$T_{startup}$	Startup Time	—	—	20	µs

6.2.5 SPLL electrical specifications

Table 20. SPLL electrical specifications

Symbol	Parameter	Min.	Typ.	Max.	Unit
F_{SPLL_REF}[1]	PLL Reference Frequency Range	8	—	16	MHz
F_{SPLL_Input}[2]	PLL Input Frequency	8	—	40	MHz
F_{VCO_CLK}	VCO output frequency	180	—	320	MHz
F_{SPLL_CLK}	PLL output frequency	90	—	160	MHz
J_{CYC_SPLL}	PLL Period Jitter (RMS)[3]				
	at F_{VCO_CLK} 180 MHz	—	120	—	ps
	at F_{VCO_CLK} 320 MHz	—	75	—	ps
J_{ACC_SPLL}	PLL accumulated jitter over 1µs (RMS)[3]				
	at F_{VCO_CLK} 180 MHz	—	1350	—	ps
	at F_{VCO_CLK} 320 MHz	—	600	—	ps
D_{UNL}	Lock exit frequency tolerance	± 4.47	—	± 5.97	%
T_{SPLL_LOCK}	Lock detector detection time[4]	—	—	$150 \times 10^{-6} + 1075(1/F_{SPLL\_REF})$	s

1. F_{SPLL_REF} is PLL reference frequency range after the PREDIV. For PREDIV and MULT settings refer SCG_SPLLCFG register of Reference Manual.
2. F_{SPLL_Input} is PLL input frequency range before the PREDIV must be limited to the range 8 MHz to 40 MHz. This input source could be derived from a crystal oscillator or some other external square wave clock source using OSC bypass mode. For external clock source settings refer SCG_SOSCCFG register of Reference Manual.
3. This specification was obtained using a NXP developed PCB. PLL jitter is dependent on the noise characteristics of each PCB and results will vary
4. Lock detector detection time is defined as the time between PLL enablement and clock availability for system use.

6.3 Memory and memory interfaces

6.3.1 Flash memory module (FTFC) electrical specifications

This section describes the electrical characteristics of the flash memory module.

6.3.1.1 Flash timing specifications — commands

Table 21. Flash command timing specifications

Symbol	Description[1]	Min.	Typ.	Max.	Unit	Notes
$t_{rd1blk64k}$ $t_{rd1blk512k}$	Read 1s Block execution time • 64 KB data flash • 512 KB program flash	— —	— —	0.5 1.8	ms ms	
$t_{rd1sec2k}$	Read 1s Section execution time (2 KB flash)	—	—	75	µs	
$t_{rd1sec4k}$	Read 1s Section execution time (4 KB flash)	—	—	100	µs	
t_{pgmchk}	Program Check execution time	—	—	95	µs	
t_{pgm8}	Program Phrase execution time	—	90	150	µs	
$t_{ersblk64k}$ $t_{ersblk512k}$	Erase Flash Block execution time • 64 KB data flash • 512 KB program flash	— —	55 435	475 3700	ms ms	2
t_{ersscr}	Erase Flash Sector execution time	—	15	115	ms	2
$t_{pgmsec1k}$	Program Section execution time (1KB flash)	—	5	—	ms	
$t_{rd1allx}$	Read 1s All Blocks execution time	— — —	— — —	2.2 4.4 6.6	ms ms ms	
t_{rdonce}	Read Once execution time	—	—	30	µs	
$t_{pgmonce}$	Program Once execution time	—	90	—	µs	
t_{ersall}	Erase All Blocks execution time	—	500	4200	ms	2
t_{vfykey}	Verify Backdoor Access Key execution time	—	—	35	µs	
$t_{ersallu}$	Erase All Blocks Unsecure execution time	—	500	4200	ms	2
$t_{pgmpart32k}$ $t_{pgmpart64k}$	Program Partition for EEPROM execution time • 32 KB EEPROM backup • 64 KB EEPROM backup (Non-Interleaved DFlash) • 64 KB EEPROM backup (Interleaved DFlash)	— —	70 71 250	— —	ms ms ms	3, 4
$t_{setramff}$ $t_{setram32k}$ $t_{setram48k}$ $t_{setram64k}$	Set FlexRAM Function execution time: • Control Code 0xFF • 32 KB EEPROM backup • 48 KB EEPROM backup • 64 KB EEPROM backup	— — — —	70 0.8 1.0 1.3	— 1.2 1.5 1.9	µs ms ms ms	3, 4
$t_{eewr8b32k}$ $t_{eewr8b48k}$ $t_{eewr8b64k}$	Byte-write to FlexRAM execution time: • 32 KB EEPROM backup • 48 KB EEPROM backup • 64 KB EEPROM backup	— — —	385 430 475	1700 1850 2000	µs µs µs	3, 4
$t_{eewr16b32k}$ $t_{eewr16b48k}$	16-bit write to FlexRAM execution time: • 32 KB EEPROM backup	— —	385 430	1700 1850	µs µs	3, 4

Table continues on the next page...

Table 21. Flash command timing specifications (continued)

Symbol	Description[1]	Min.	Typ.	Max.	Unit	Notes
$t_{eewr16b64k}$	• 48 KB EEPROM backup • 64 KB EEPROM backup	—	475	2000	µs	
$t_{eewr32bers}$	32-bit write to erased FlexRAM location execution time	—	360	2000	µs	
$t_{eewr32b32k}$ $t_{eewr32b48k}$ $t_{eewr32b64k}$	32-bit write to FlexRAM execution time: • 32 KB EEPROM backup • 48 KB EEPROM backup • 64 KB EEPROM backup	— — —	630 720 810	2000 2125 2250	µs µs µs	3, 4
$t_{quickwr}$	32-bit Quick Write execution time : Time from CCIF clearing (start the write) until CCIF setting (32-bit write complete, ready for next 32-bit write)					
	• 1st 32-bit write • 2nd through Next to Last (Nth-1) 32-bit write • Last (Nth) 32-bit write (time for write only, not cleanup)	— — —	200 150 200	550 550 550	µs µs µs	5, 6
$t_{quickwrClnup}$	Quick Write Cleanup execution time	—	—	(Number of Quick Writes) * 2.0	ms	7

1. All command times assumes 25 MHz or greater flash clock frequency (for synchronization time between internal/external clocks).
2. Maximum times for erase parameters based on expectations at cycling end-of-life.
3. For all EEPROM Emulation terms, the specified timing shown assumes previous record clean up has occurred. This may be verified by executing FCCOB Command 0x77, and checking FCCOB number 5 contents show 0x00 - No EEPROM issues detected.
4. 'First time' EERAM writes after a Reset or SETRAM may incur additional overhead for EEE cleanup, resulting in up to 2x the times shown.
5. For 'Typ.', only after the Nth write completes will any data will be valid. Emulated EEPROM record scheme cleanup overhead may occur after this point even after a brownout or reset. If power or reset occurs before the Nth write completes, the last valid record set will still be valid and the new records will be discarded.
6. Quick Write may take up to 550 µs as additional cleanup may occur when crossing sector boundaries.
7. Time for emulated EEPROM record scheme overhead cleanup. Automatically done after last (Nth) write completes, assuming still powered. Or via SETRAM cleanup execution command is requested at a later point.

NOTE

Under certain circumstances FlexMEM maximum times may be exceeded. In this case the user or application may wait, or assert reset to the FTFC macro to stop the operation.

6.3.1.2 Reliability specifications

Table 22. NVM reliability specifications

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
When using as Program and Data Flash						

Table continues on the next page...

Table 22. NVM reliability specifications (continued)

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
$t_{nvmretp1k}$	Data retention after up to 1 K cycles	20	—	—	years	
$n_{nvmcycp}$	Cycling endurance	1 K	—	—	cycles	2, 1
When using FlexMemory feature: FlexRAM as Emulated EEPROM						
$t_{nvmretee}$	Data retention	5	—	—	years	
$n_{nvmwree16}$ $n_{nvmwree256}$	Write endurance • EEPROM backup to FlexRAM ratio = 16 • EEPROM backup to FlexRAM ratio = 256	100 K 1.6 M	— —	— —	writes writes	3, 4, 5

1. Program and Erase for PFlash and DFlash are supported across product temperature specification in Normal Mode (not supported in HSRUN mode).
2. Cycling endurance is per DFlash or PFlash Sector.
3. FlexMemory write endurance specified for 16-bit and/or 32-bit writes to FlexRAM and is supported across standard temperature specification in Normal Mode (not supported in HSRUN mode). Greater write endurance may be achieved with larger ratios of EEPROM backup to FlexRAM.
4. For usage of any other EEE driver other than the FlexMemory feature, the endurance specification will fall back to the specified endurance value of the D-Flash specification (1 K).
5. EEE calculator tool is available at NXP web site to help estimate the maximum write endurance achievable at specific EEPROM/FlexRAM ratio. The “In Spec” portions of the online calculator refer to the NVM reliability specifications section of data sheet. This calculator is only applies to the FlexMemory feature.

6.3.2 QuadSPI AC specifications

The following table describes the QuadSPI electrical characteristics.

- Measurements are with maximum output load of 25 pF, input transition of 1 ns and pad configured with fastest slew settings (DSE = 1'b1).
- I/O operating voltage ranges from 2.97 V to 3.6 V
- While doing the mode transition (RUN -> HSRUN or HSRUN -> RUN), the interface should be OFF.
- Add 50 ohm series termination on board in QuadSPI SCK for Flash A to avoid loop back reflection when using in Internal DQS (PAD Loopback) mode.
- For non-Quad mode of operation if external device doesn’t have pull-up feature, external pull-up needs to be added at board level for non-used pads.
- With external pull-up, performance of the interface may degrade based on load associated with external pull-up.

Table 23. QuadSPI electrical specifications

FLASH PORT	Sym	Unit	FLASH A												FLASH B			
			RUN[1]						HSRUN[1]						RUN/HSRUN[2]			
QuadSPI Mode			SDR						SDR						SDR		DDR[3]	
			Internal Sampling		Internal DQS				Internal Sampling		Internal DQS				Internal Sampling		External DQS	
			N1		PAD Loopback		Internal Loopback		N1		PAD Loopback		Internal Loopback		N1		Extrenal DQS	
			Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max
Register Settings																		
MCR[DDR_EN]		-	0		0		0		0		0		0		0		1	
MCR[DQS_EN]		-	0		1		1		0		1		1		0		1	
MCR[SCLKCFG[0]]		-	-		1		0		-		1		0		-		-	
MCR[SCLKCFG[1]]		-	-		1		0		-		1		0		-		-	
MCR[SCLKCFG[2]]		-	-		-		-		-		-		-		-		0	
MCR[SCLKCFG[3]]		-	-		-		-		-		-		-		-		0	
MCR[SCLKCFG[5]]		-	-		-		-		-		-		-		-		1	
SMPR[FSPHS]		-	0		1		0		0		1		0		0		0	
SMPR[FSDLY]		-	0		0		0		0		0		0		0		0	
SOCCR [SOCCFG[7:0]]			-		0		23		-		0		30		-		-	
SOCCR[SOCCFG[15:8]]		-	-		-		-		-		-		-		-		30	
FLSHCR[TDH]		-	0x00		0x00		0x00		0x00		0x00		0x00		0x00		0x01	
Timing Parameters																		
SCK Clock Frequency	f_{SCK}	MHz	-	38	-	64	-	48	-	40	-	80	-	50	-	20	-	20[4]
SCK Clock Period	t_{SCK}	ns	1/fSCK	-	1/fSCK	-	1/fSCK	-	1/fSCK	-	1/fSCK	-	1/fSCK	-	50.0	-	50.0[4]	-

Table continues on the next page...

Table 23. QuadSPI electrical specifications (continued)

FLASH PORT	Sym	Unit	FLASH A												FLASH B			
			RUN[1]						HSRUN[1]						RUN/HSRUN[2]			
QuadSPI Mode			SDR						SDR						SDR		DDR[3]	
			Internal Sampling		Internal DQS				Internal Sampling		Internal DQS				Internal Sampling		External DQS	
			N1		PAD Loopback		Internal Loopback		N1		PAD Loopback		Internal Loopback		N1		Extrenal DQS	
			Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max
SCK Duty Cycle	t_{SDC}	ns	tSCK/2 - 1.5	tSCK/2 + 1.5	tSCK/2 - 1.5	tSCK/2 + 1.5	tSCK/2 - 1.5	tSCK/2 + 1.5	tSCK/2 - 1.5	tSCK/2 + 1.5	tSCK/2 - 0.750	tSCK/2 - 0.750	tSCK/2 - 1.5	tSCK/2 + 1.5	tSCK/2 - 2.5	tSCK/2 + 2.5	tSCK/2 - 2.5	tSCK/2 + 2.5
Data Input Setup Time	t_{IS}	ns	15	-	2.5	-	10	-	14	-	1.5	-	9	-	25	-	-2	-
Data Input Hold Time	t_{IH}	ns	0	-	1	-	1	-	0	-	1	-	1	-	0	-	0	-
Data Output Valid Time	t_{OV}	ns	-	4.5	-	4.5	-	4.5	-	4	-	4	-	4	-	10	-	10
Data Output In-Valid Time	t_{IV}	ns	5	-	5	-	5	-	5	-	3[5]	-	5	-	5	-	5	-
CS to SCK Time [6]	t_{CSSCK}	ns	5	-	5	-	5	-	5	-	5	-	5	-	10	-	10	-
SCK to CS Time [7]	t_{SCKCS}	ns	5	-	5	-	5	-	5	-	5	-	5	-	5	-	5	-
Output Load		pf	25		25		25		25		25		25		25		25	

1. See Reference Manual for details on mode settings
2. See Reference Manual for details on mode settings
3. Valid for HyperRAM only
4. RWDS(External DQS CLK) frequency
5. For operating frequency ≤ 64 Mhz,Output invalid time is 5 ns.
6. Program register value QuadSPI_FLSHCR[TCSS] = 4`h2
7. Program register value QuadSPI_FLSHCR[TCSH] = 4`h1

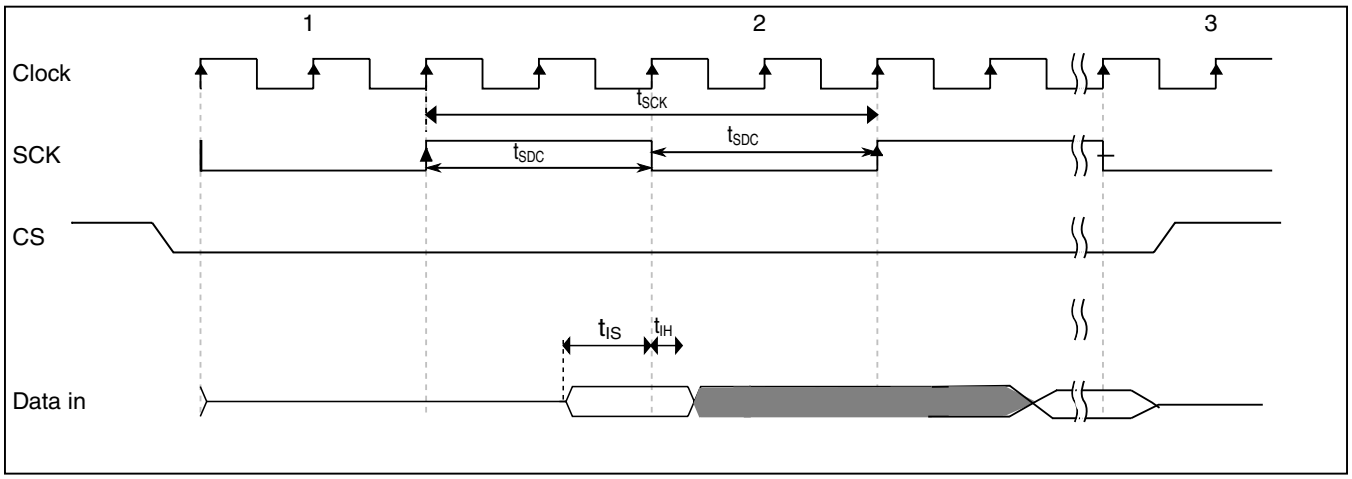


Figure 8. QuadSPI input timing (SDR mode) diagram

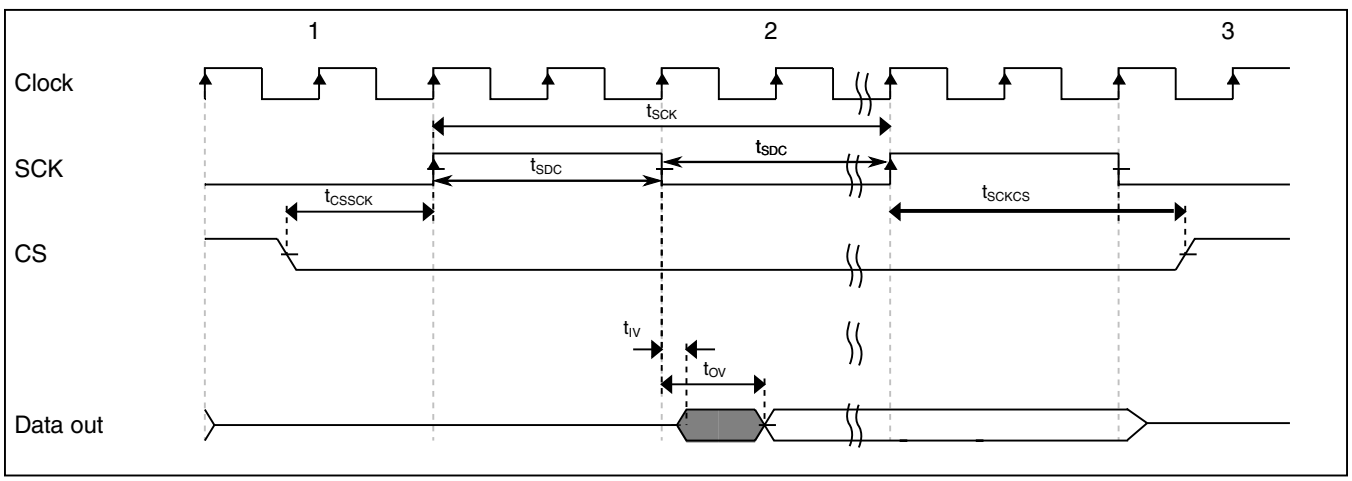


Figure 9. QuadSPI output timing (SDR mode) diagram

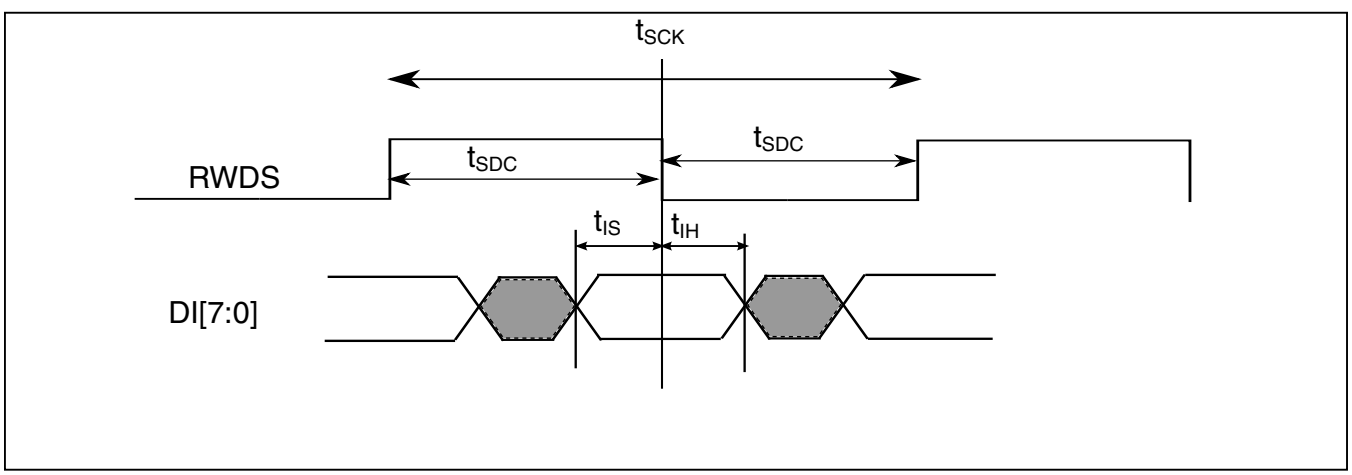


Figure 10. QuadSPI input timing (HyperRAM mode) diagram

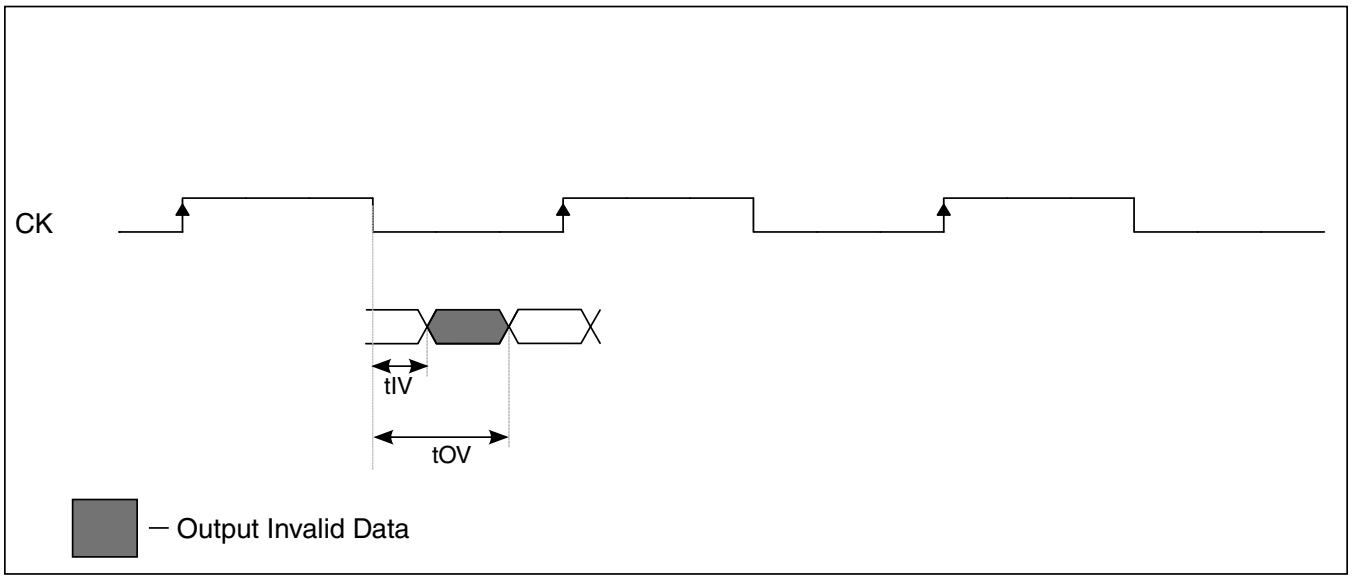


Figure 11. QuadSPI output timing (HyperRAM mode) diagram

6.4 Analog modules

6.4.1 ADC electrical specifications

6.4.1.1 12-bit ADC operating conditions

Table 24. 12-bit ADC operating conditions

Symbol	Description	Conditions	Min.	Typ.[1]	Max.	Unit	Notes
ΔV_{DDA}	Supply voltage	Delta to V_{DD} (V_{DD} – V_{DDA})	-0.1	0	+0.1	V	2
V_{REFH}	ADC reference voltage high		See Voltage and current operating requirements for values	V_{DDA}	See Voltage and current operating requirements for values	V	3
V_{REFL}	ADC reference voltage low		See Voltage and current operating requirements for values	0	See Voltage and current operating requirements for values	mV	3
V_{ADIN}	Input voltage		V_{REFL}	—	V_{REFH}	V	
R_S	Source impedendance	f_{ADCK} < 4 MHz	—	—	5	kΩ	
R_{SW1}	Channel Selection Switch Impedance		—	-0.75	1.2	kΩ	
R_{AD}	Sampling Switch Impedance		—	2	5	kΩ	
C_{P1}	Pin Capacitance		—	10	—	pF	

Table continues on the next page...

Table 24. 12-bit ADC operating conditions (continued)

Symbol	Description	Conditions	Min.	Typ.[1]	Max.	Unit	Notes
C_{P2}	Analog Bus Capacitance		—	—	4	pF	
C_S	Sampling capacitance		—	4	5	pF	
f_{ADCK}	ADC conversion clock frequency	Normal usage	2	40	50	MHz	4, 5
f_{CONV}	ADC conversion frequency	No ADC hardware averaging.[6] Continuous conversions enabled, subsequent conversion time	46.4	928	1160	Ksps	7, 8
		ADC hardware averaging set to 32. [6] Continuous conversions enabled, subsequent conversion time	1.45	29	36.25	Ksps	7, 8

1. Typical values assume V_{DDA} = 5 V, Temp = 25 °C, f_{ADCK} = 40 MHz, R_{AS}=20 Ω, and C_{AS}=10 nF unless otherwise stated. Typical values are for reference only, and are not tested in production.
2. DC potential difference.
3. For packages without dedicated V_{REFH} and V_{REFL} pins, V_{REFH} is internally tied to V_{DDA}, and V_{REFL} is internally tied to V_{SS}. To get maximum performance, reference supply quality should be better than SAR ADC. See application note AN5032 for details.
4. Clock and compare cycle need to be set according to the guidelines mentioned in the *Reference Manual* .
5. ADC conversion will become less reliable above maximum frequency.
6. When using ADC hardware averaging, see the *Reference Manual* to determine the most appropriate setting for AVGS.
7. Numbers based on the minimum sampling time of 275 ns.
8. For guidelines and examples of conversion rate calculation, see the *Reference Manual* or download the ADC calculator tool.

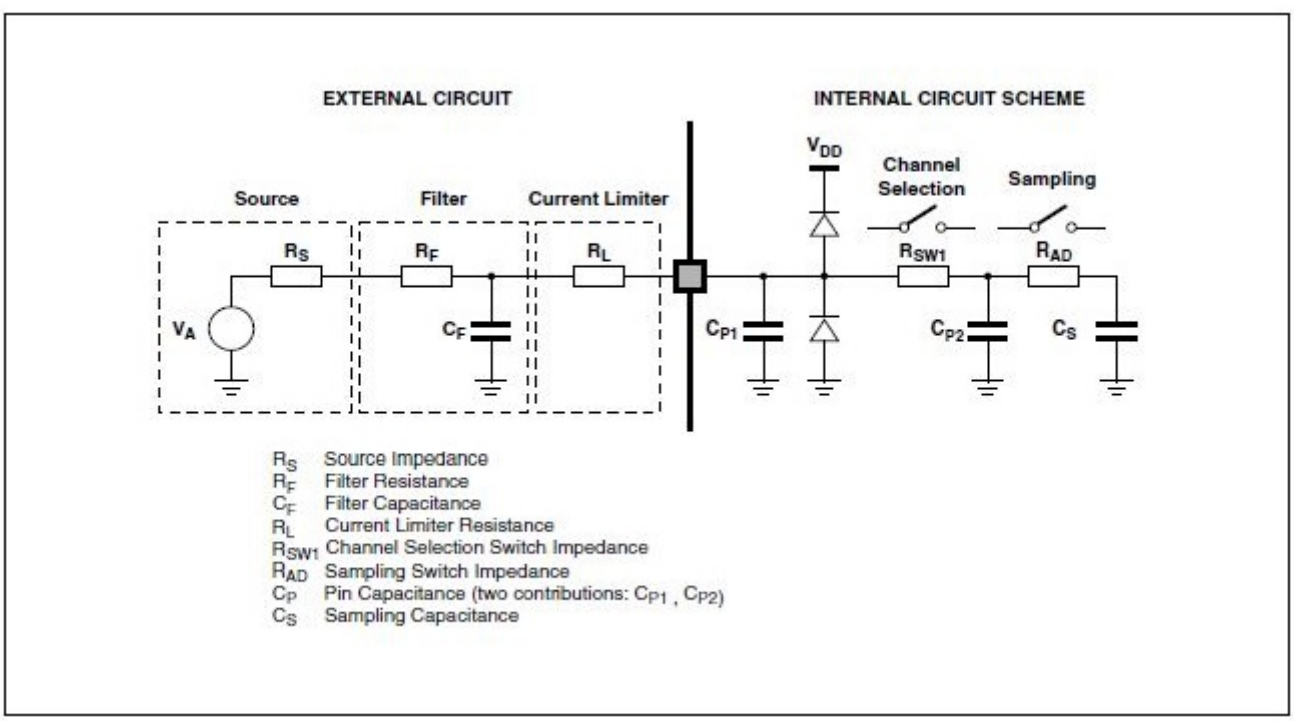


Figure 12. ADC input impedance equivalency diagram

6.4.1.2 12-bit ADC electrical characteristics

NOTE

ADC performance specifications are documented using a single ADC. For parallel/simultaneous operation of both ADCs, either for sampling the same channel by both ADCs or for sampling different channels by each ADC, some amount of decrease in performance can be expected. Care must be taken to stagger the two ADC conversions, in particular the sample phase, to minimize the impact of simultaneous conversions.

Table 25. 12-bit ADC characteristics (2.7 V to 3 V) ($V_{REFH} = V_{DDA}$, $V_{REFL} = V_{SS}$)

Symbol	Description	Conditions [1]	Min.	Typ.[2]	Max.	Unit	Notes
V_{DDA}	Supply voltage		2.7	—	3	V	
I_{DDA_ADC}	Supply current per ADC		—	0.6	1.5	mA	3
SMPLTS	Sample Time		275	—	Refer to the *Reference Manual*	ns	
TUE[4]	Total unadjusted error		—	±4	±8	LSB[5]	6, 7, 8, 9
DNL	Differential non-linearity		—	±1.0	—	LSB[5]	6, 7, 8, 9
INL	Integral non-linearity		—	±2.0	—	LSB[5]	6, 7, 8, 9

1. All accuracy numbers assume the ADC is calibrated with V_{REFH}=V_{DDA}=V_{DD}, with the calibration frequency set to half the ADC clock frequency.
2. Typical values assume V_{DDA} = 3 V, Temp = 25 °C, f_{ADCK} = 40 MHz, R_{AS}=20 Ω, and C_{AS}=10 nF, 100 LQFP package unless otherwise stated.
3. The ADC supply current depends on the ADC conversion rate.
4. Represents total static error, which includes offset and full scale error.
5. 1 LSB = $(V_{REFH} - V_{REFL})/2^N$
6. The specifications are with averaging and in standalone mode only. Performance may degrade depending upon device use case scenario. When using ADC averaging, refer to the *Reference Manual* to determine the most appropriate settings for AVGS.
7. For ADC signals adjacent to V_{DD}/V_{SS} or XTAL/EXTAL or high frequency switching pins, some degradation in the ADC performance may be observed.
8. All values guarantee the performance of the ADC for multiple ADC input channel pins. When using ADC to monitor the internal analog parameters, assume minor degradation.
9. All the parameters in the table are given assuming system clock as the clocking source for ADC.

Table 26. 12-bit ADC characteristics (3 V to 5.5 V)($V_{REFH} = V_{DDA}$, $V_{REFL} = V_{SS}$)

Symbol	Description	Conditions [1]	Min.	Typ.[2]	Max.	Unit	Notes
V_{DDA}	Supply voltage		3	—	5.5	V	
I_{DDA_ADC}	Supply current per ADC		—	1	2.1	mA	3
SMPLTS	Sample Time		275	—	Refer to the *Reference Manual*	ns	

Table continues on the next page...

Table 26. 12-bit ADC characteristics (3 V to 5.5 V)(V_{REFH} = V_{DDA}, V_{REFL} = V_{SS}) (continued)

Symbol	Description	Conditions [1]	Min.	Typ.[2]	Max.	Unit	Notes
TUE[4]	Total unadjusted error		—	±4	±8	LSB[5]	6, 7, 8, 9
DNL	Differential non-linearity		—	±0.7	—	LSB[5]	6, 7, 8, 9
INL	Integral non-linearity		—	±1.0	—	LSB[5]	6, 7, 8, 9

1. All accuracy numbers assume the ADC is calibrated with V_{REFH}=V_{DDA}=V_{DD}, with the calibration frequency set to half the ADC clock frequency.
2. Typical values assume V_{DDA} = 5.0 V, Temp = 25 °C, f_{ADCK} = 40 MHz, R_{AS}=20 Ω, and C_{AS}=10 nF unless otherwise stated.
3. The ADC supply current depends on the ADC conversion rate.
4. Represents total static error, which includes offset and full scale error.
5. 1 LSB = (V_{REFH} - V_{REFL})/2^N
6. The specifications are with averaging and in standalone mode only. Performance may degrade depending upon device use case scenario. When using ADC averaging, refer to the *Reference Manual* to determine the most appropriate settings for AVGS.
7. For ADC signals adjacent to V_{DD}/V_{SS} or XTAL/EXTAL or high frequency switching pins, some degradation in the ADC performance may be observed.
8. All values guarantee the performance of the ADC for multiple ADC input channel pins. When using ADC to monitor the internal analog parameters, assume minor degradation.
9. All the parameters in the table are given assuming system clock as the clocking source for ADC.

NOTE

When using high speed interfaces such as the QuadSPI, SAI0, SAI1 or ENET there may be some ADC degradation on the adjacent analog input paths. See following table for details.

Pin name	TGATE purpose
PTE8	CMP0_IN3
PTC3	ADC0_SE11/CMP0_IN4
PTC2	ADC0_SE10/CMP0_IN5
PTD7	CMP0_IN6
PTD6	CMP0_IN7
PTD28	ADC1_SE22
PTD27	ADC1_SE21

6.4.2 CMP with 8-bit DAC electrical specifications

Table 28. Comparator with 8-bit DAC electrical specifications

Symbol	Description	Min.	Typ.	Max.	Unit
I_{DDHS}	Supply current, High-speed mode[1]				µA
	-40 - 125 °C	—	230	300	
I_{DDLS}	Supply current, Low-speed mode[1]				µA
	-40 - 105 °C	—	5	10	
	-40 - 125 °C		5	13	

Table continues on the next page...

Table 28. Comparator with 8-bit DAC electrical specifications (continued)

Symbol	Description	Min.	Typ.	Max.	Unit
V_{AIN}	Analog input voltage	0	0 - V_{DDA}	V_{DDA}	V
V_{AIO}	Analog input offset voltage, High-speed mode				mV
	-40 - 125 °C	-25	±1	25	
V_{AIO}	Analog input offset voltage, Low-speed mode				mV
	-40 - 125 °C	-40	±4	40	
t_{DHSB}	Propagation delay, High-speed mode[2]				ns
	-40 - 105 °C	—	30	200	
	-40 - 125 °C		30	300	
t_{DLSB}	Propagation delay, Low-speed mode[2]				µs
	-40 - 105 °C	—	0.5	2	
	-40 - 125 °C	—	0.5	3	
t_{DHSS}	Propagation delay, High-speed mode[3]				ns
	-40 - 105 °C	—	70	400	
	-40 - 125 °C	—	70	500	
t_{DLSS}	Propagation delay, Low-speed mode[3]				µs
	-40 - 105 °C	—	1	5	
	-40 - 125 °C	—	1	5	
t_{IDHS}	Initialization delay, High-speed mode[4]				µs
	-40 - 125 °C	—	1.5	3	
t_{IDLS}	Initialization delay, Low-speed mode[4]				µs
	-40 - 125 °C	—	10	30	
V_{HYST0}	Analog comparator hysteresis, Hyst0 (V_{AIO})				mV
	-40 - 125 °C	—	0	—	
V_{HYST1}	Analog comparator hysteresis, Hyst1, High-speed mode				mV
	-40 - 125 °C	—	16	66	
	Analog comparator hysteresis, Hyst1, Low-speed mode				
	-40 - 125 °C	—	11	40	
V_{HYST2}	Analog comparator hysteresis, Hyst2, High-speed mode				mV
	-40 - 125 °C	—	32	133	
	Analog comparator hysteresis, Hyst2, Low-speed mode				
	-40 - 125 °C	—	22	80	
V_{HYST3}	Analog comparator hysteresis, Hyst3, High-speed mode				mV
	-40 - 125 °C	—	48	200	
	Analog comparator hysteresis, Hyst3, Low-speed mode				
	-40 - 125 °C	—	33	120	

Table continues on the next page...

Table 28. Comparator with 8-bit DAC electrical specifications (continued)

Symbol	Description	Min.	Typ.	Max.	Unit
I_{DAC8b}	8-bit DAC current adder (enabled)				
	3.3V Reference Voltage	—	6	9	µA
	5V Reference Voltage	—	10	16	µA
INL[5]	8-bit DAC integral non-linearity	–0.75	—	0.75	LSB[6]
DNL	8-bit DAC differential non-linearity	–0.5	—	0.5	LSB[6]
t_{DDAC}	Initialization and switching settling time	—	—	30	µs

1. Difference at input > 200mV
2. Applied ± (100 mV + $V_{HYST0/1/2/3}$+ max. of V_{AIO}) around switch point.
3. Applied ± (30 mV + 2 × $V_{HYST0/1/2/3}$+ max. of V_{AIO}) around switch point.
4. Applied ± (100 mV + $V_{HYST0/1/2/3}$).
5. Calculation method used: Linear Regression Least Square Method
6. 1 LSB = $V_{reference}$/256

NOTE

For comparator IN signals adjacent to V_{DD}/V_{SS} or XTAL/EXTAL or switching pins cross coupling may happen and hence hysteresis settings can be used to obtain the desired comparator performance. Additionally, an external capacitor (1nF) should be used to filter noise on input signal. Also, source drive should not be weak (Signal with < 50 K pull up/down is recommended).

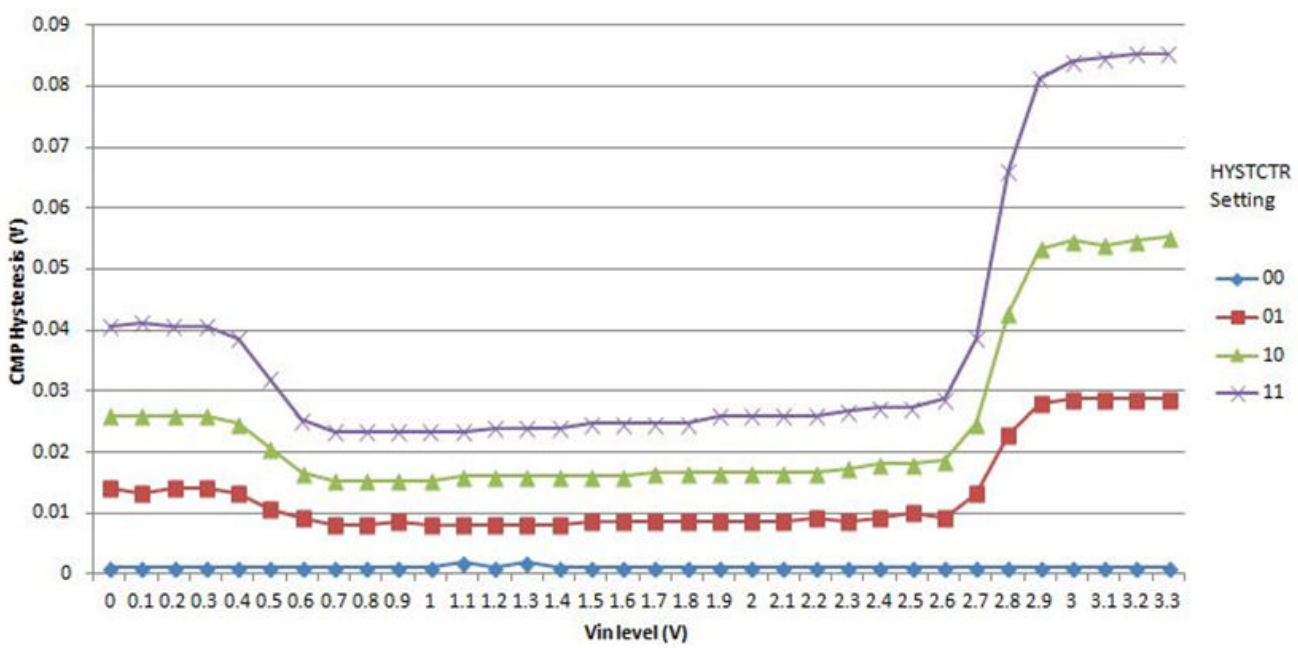


Figure 13. Typical hysteresis vs. Vin level (VDDA = 3.3 V, PMODE = 0)

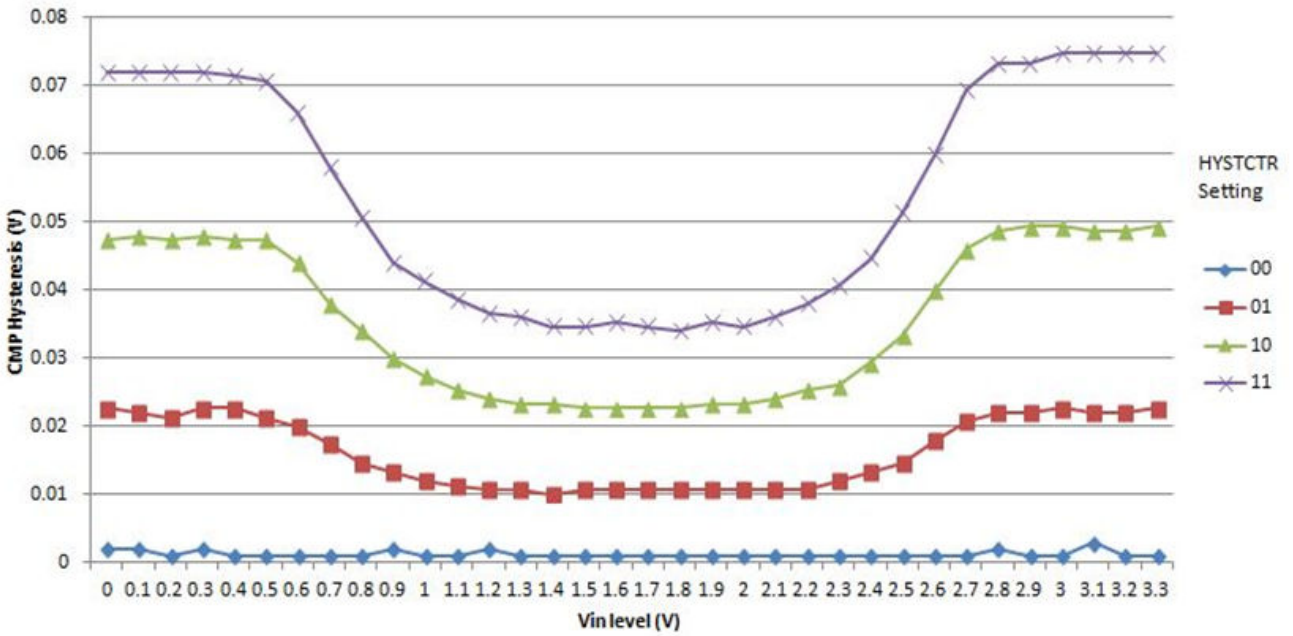


Figure 14. Typical hysteresis vs. Vin level (VDDA = 3.3 V, PMODE = 1)

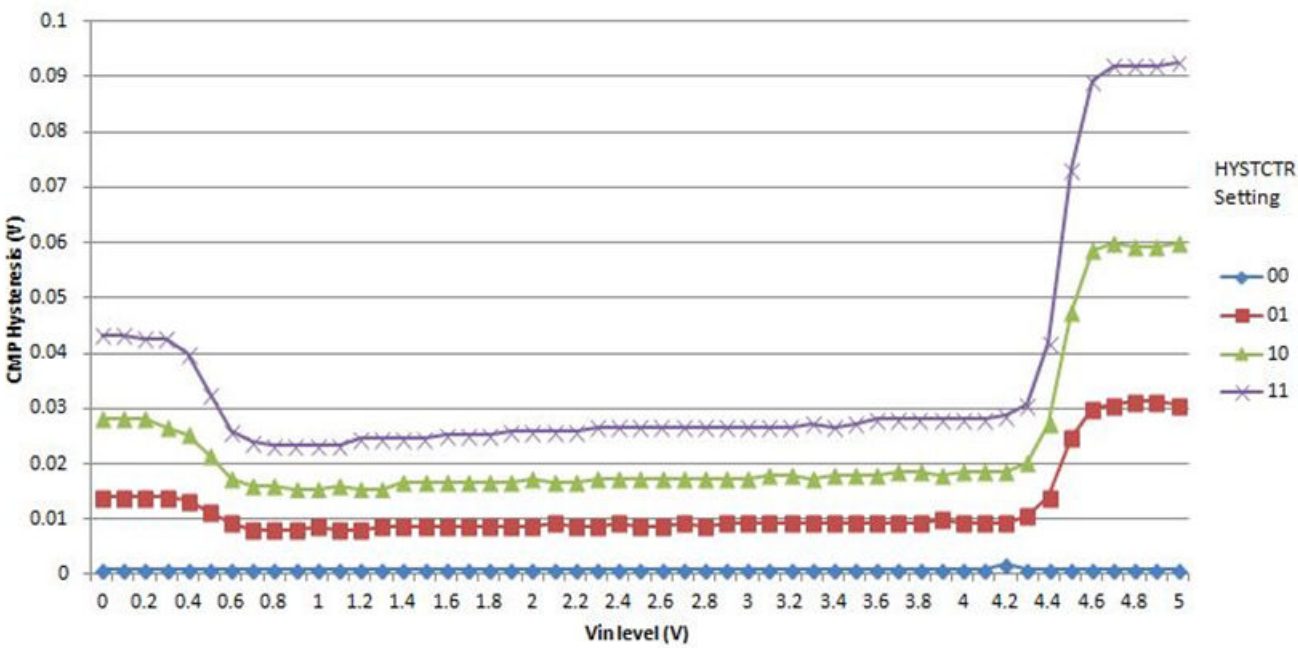


Figure 15. Typical hysteresis vs. Vin level (VDDA = 5 V, PMODE = 0)

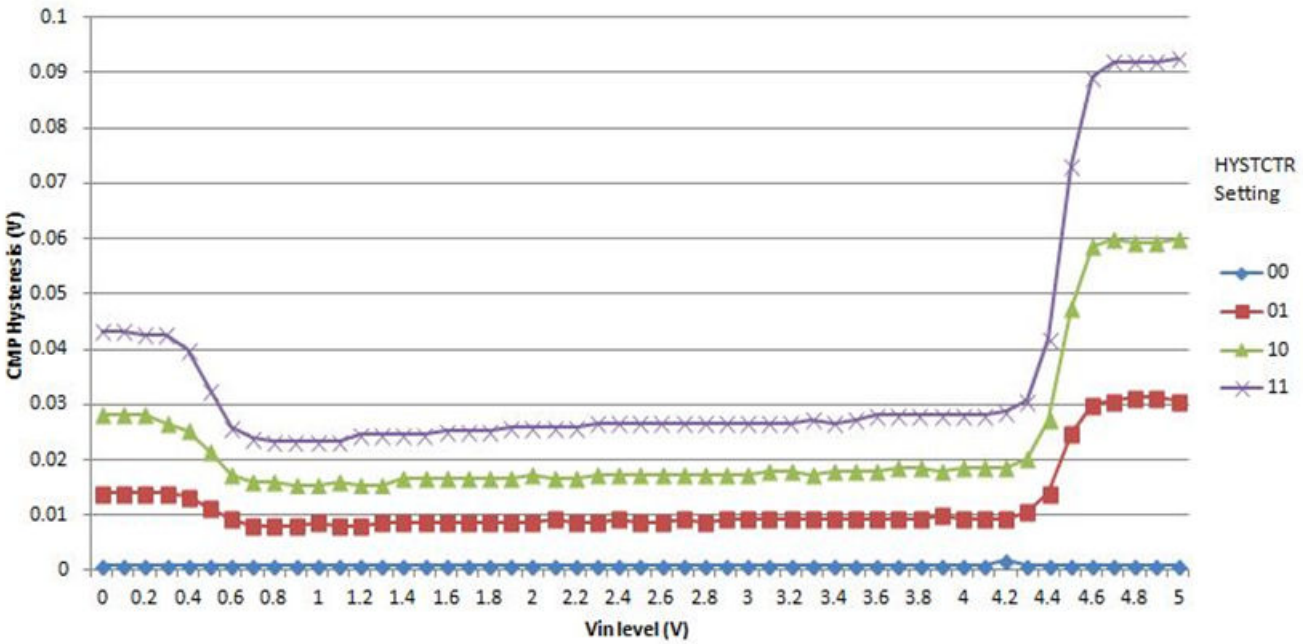


Figure 16. Typical hysteresis vs. Vin level (VDDA = 5 V, PMODE = 1)

6.5 Communication modules

6.5.1 LPUART electrical specifications

Refer to General AC specifications for LPUART specifications.

6.5.1.1 Supported baud rate

Baud rate = Baud clock / ((OSR+1) * SBR).

For details, see section: 'Baud rate generation' of the *Reference Manual*.

6.5.2 LPSPI electrical specifications

The Low Power Serial Peripheral Interface (LPSPI) provides a synchronous serial bus with master and slave operations. Many of the transfer attributes are programmable. The following tables provide timing characteristics for classic LPSPI timing modes.

- All timing is shown with respect to 20% V_{DD} and 80% V_{DD} thresholds.
- All measurements are with maximum output load of 50 pF, input transition of 1 ns and pad configured with fastest slew setting (DSE = 1).

Table 29. LPSPI electrical specifications[1]

Num	Symbol	Description	Conditions	Run Mode[2]				HSRUN Mode[2]				VLPR Mode				Unit
				5.0 V IO		3.3 V IO		5.0 V IO		3.3 V IO		5.0 V IO		3.3 V IO		
				Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
	f_{periph} [3, 4]	Peripheral Frequency	Slave	-	40	-	40	-	56	-	56	-	8	-	8	MHz
			Master	-	40	-	40	-	56	-	56	-	8	-	8	
			Master Loopback [5]	-	40	-	48	-	48	-	48	-	8	-	8	
			Master Loopback(Slow) [6]	-	48	-	48	-	48	-	48	-	8	-	8	
1	f_{op}	Frequency of operation	Slave	-	10	-	10	-	14	-	14	-	4	-	4	MHz
			Master	-	10	-	10	-	14	-	14	-	4	-	4	
			Master Loopback[5]	-	20	-	12	-	24	-	12	-	4	-	4	
			Master Loopback(slow) [6]	-	12	-	12	-	12	-	12	-	4	-	4	
2	t_{SPSCK}	SPSCK period	Slave	100	-	100	-	72	-	72	-	250	-	250	-	ns
			Master	100	-	100	-	72	-	72	-	250	-	250	-	
			Master Loopback[5]	50	-	83	-	42	-	83	-	250	-	250	-	
			Master Loopback(slow) [6]	83	-	83	-	83	-	83	-	250	-	250	-	
3	t_{Lead}[7]	Enable lead time (PCS to SPSCK delay)	Slave	-	-	-	-	-	-	-	-	-	-	-	-	ns

Table continues on the next page...

Table 29. LPSPI electrical specifications[1] (continued)

Num	Symbol	Description	Conditions	Run Mode[2]				HSRUN Mode[2]				VLPR Mode				Unit
				5.0 V IO		3.3 V IO		5.0 V IO		3.3 V IO		5.0 V IO		3.3 V IO		
				Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
			Master	(PCSSCK + 1)*t_{SPSCK} - 25	-	(PCSSCK + 1)*t_{SPSCK} - 25	-	(PCSSCK + 1)*t_{SPSCK} - 25	-	(PCSSCK + 1)*t_{SPSCK} - 25	-	(PCSSCK + 1)*t_{SPSCK} - 50	-	(PCSSCK + 1)*t_{SPSCK} - 50	-	ns
			Master Loopback[5]													
			Master Loopback(slow) [6]													
4	t_{Lag}[8]	Enable lag time (After SPSCK delay)	Slave	-	-	-	-	-	-	-	-	-	-	-	-	
			Master	(SCKPCS + 1)*t_{SPSCK} - 25	-	(SCKPCS + 1)*t_{SPSCK} - 25	-	(SCKPCS + 1)*t_{SPSCK} - 25	-	(SCKPCS + 1)*t_{SPSCK} - 25	-	(SCKPCS + 1)*t_{SPSCK} - 50	-	(SCKPCS + 1)*t_{SPSCK} - 50	-	
			Master Loopback[5]													
			Master Loopback(slow) [6]													

Table continues on the next page...

Table 29. LPSPI electrical specifications[1] (continued)

Num	Symbol	Description	Conditions	Run Mode[2]				HSRUN Mode[2]				VLPR Mode				Unit
				5.0 V IO		3.3 V IO		5.0 V IO		3.3 V IO		5.0 V IO		3.3 V IO		
				Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
5	t_{WSPSCK}	Clock(SPSCK) high or low time (SPSCK duty cycle)	Slave	$t_{SPSCK}/2 - 3$	$t_{SPSCK}/2 + 3$	$t_{SPSCK}/2 - 3$	$t_{SPSCK}/2 + 3$	$t_{SPSCK}/2 - 3$	$t_{SPSCK}/2 + 3$	$t_{SPSCK}/2 - 3$	$t_{SPSCK}/2 + 3$	$t_{SPSCK}/2 - 5$	$t_{SPSCK}/2 + 5$	$t_{SPSCK}/2 - 5$	$t_{SPSCK}/2 + 5$	ns
			Master													
			Master Loopback[5]													
			Master Loopback(slow)[6]													
6	t_{SU}	Data setup time(inputs)	Slave	3	-	5	-	3	-	5	-	18	-	18	-	ns
			Master	29	-	38	-	26	-	37	-	72	-	78	-	
			Master Loopback[5]	7	-	8	-	5	-	7	-	20	-	20	-	
			Master Loopback(slow)[6]	8	-	10	-	7	-	9	-	20	-	20	-	
7	t_{HI}	Data hold time(inputs)	Slave	3	-	3	-	3	-	3	-	14	-	14	-	ns
			Master	0	-	0	-	0	-	0	-	0	-	0	-	
			Master Loopback[5]	3	-	3	-	2	-	3	-	11	-	11	-	
			Master Loopback(slow)[6]	3	-	3	-	3	-	3	-	12	-	12	-	
8	t_a	Slave access time	Slave	-	50	-	50	-	50	-	50	-	100	-	100	ns
9	t_{dis}	Slave MISO (SOUT) disable time	Slave	-	50	-	50	-	50	-	50	-	100	-	100	ns

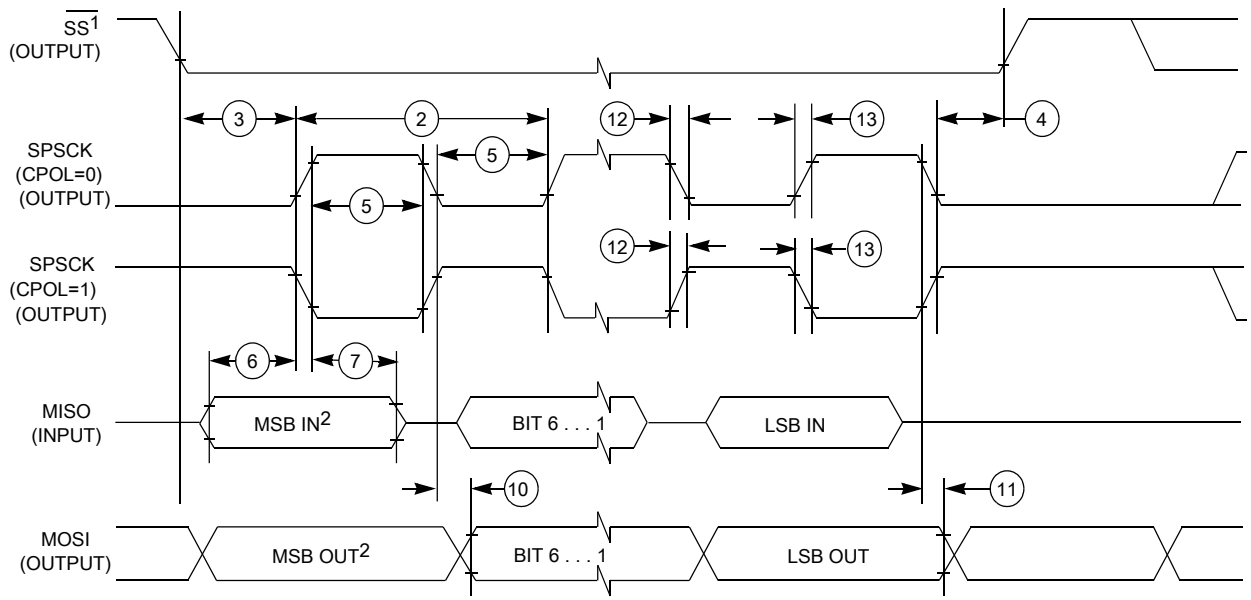
Table continues on the next page...

Table 29. LPSPI electrical specifications[1] (continued)

Num	Symbol	Description	Conditions	Run Mode[2]				HSRUN Mode[2]				VLPR Mode				Unit
				5.0 V IO		3.3 V IO		5.0 V IO		3.3 V IO		5.0 V IO		3.3 V IO		
				Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
10	t_V	Data valid (after SPSCK edge)	Slave	-	30	-	39	-	26	-	36	-	92	-	96	ns
			Master	-	12	-	16	-	11	-	15	-	47	-	48	
			Master Loopback[5]	-	12	-	16	-	11	-	15	-	47	-	48	
			Master Loopback(slow) [6]	-	8	-	10	-	7	-	9	-	44	-	44	
11	t_{HO}	Data hold time(outputs)	Slave	4	-	4	-	4	-	4	-	4	-	4	-	ns
			Master	-15	-	-22	-	-15	-	-23	-	-22	-	-29	-	
			Master Loopback[5]	-10	-	-14	-	-10	-	-14	-	-14	-	-19	-	
			Master Loopback(slow) [6]	-15	-	-22	-	-15	-	-22	-	-21	-	-27	-	
12	$t_{RI/FI}$	Rise/Fall time input	Slave	-	1	-	1	-	1	-	1	-	1	-	1	ns
			Master	-		-		-		-		-		-		
			Master Loopback[5]	-		-		-		-		-		-		
			Master Loopback(slow) [6]	-		-		-		-		-		-		
13	$t_{RO/FO}$	Rise/Fall time output	Slave	-	25	-	25	-	25	-	25	-	25	-	25	ns
			Master	-		-		-		-		-		-		
			Master Loopback [5]	-		-		-		-		-		-		
			Master Loopback(slow) [6]	-		-		-		-		-		-		

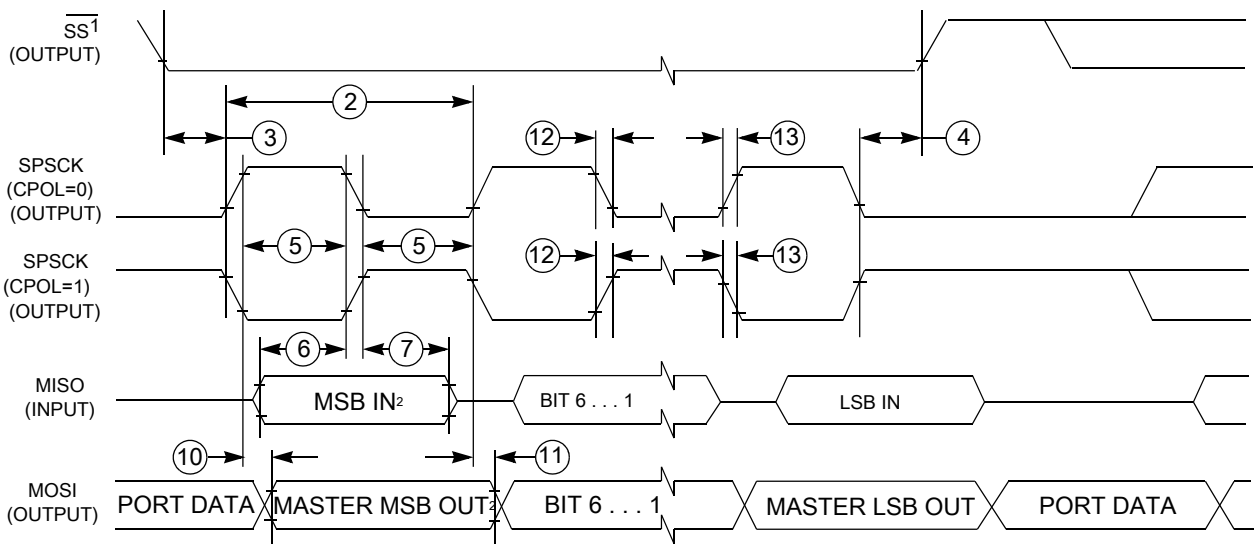
1. Trace length should not exceed 11 inches for SCK pad when used in Master loopback mode.
2. While transitioning from HSRUN mode to RUN mode, LPSPI output clock should not be more than 14 MHz.
3. f_{periph} = LPSPI peripheral clock

4. $t_{periph} = 1/f_{periph}$
5. Master Loopback mode - In this mode LPSPI_SCK clock is delayed for sampling the input data which is enabled by setting LPSPI_CFGR1[SAMPLE] bit as 1. Clock pads used are PTD15 and PTE0. Applicable only for LPSPI0.
6. Master Loopback (slow) - In this mode LPSPI_SCK clock is delayed for sampling the input data which is enabled by setting LPSPI_CFGR1[SAMPLE] bit as 1. Clock pad used is PTB2. Applicable only for LPSPI0.
7. Set the PCSSCK configuration bit as 0, for a minimum of 1 delay cycle of LPSPI baud rate clock, where PCSSCK ranges from 0 to 255.
8. Set the SCKPCS configuration bit as 0, for a minimum of 1 delay cycle of LPSPI baud rate clock, where SCKPCS ranges from 0 to 255.



1. If configured as an output.
2. LSBF = 0. For LSBF = 1, bit order is LSB, bit 1, ..., bit 6, MSB.

Figure 17. LPSPI master mode timing (CPHA = 0)



1.If configured as output
2. LSBF = 0. For LSBF = 1, bit order is LSB, bit 1, ..., bit 6, MSB.

Figure 18. LPSPI master mode timing (CPHA = 1)

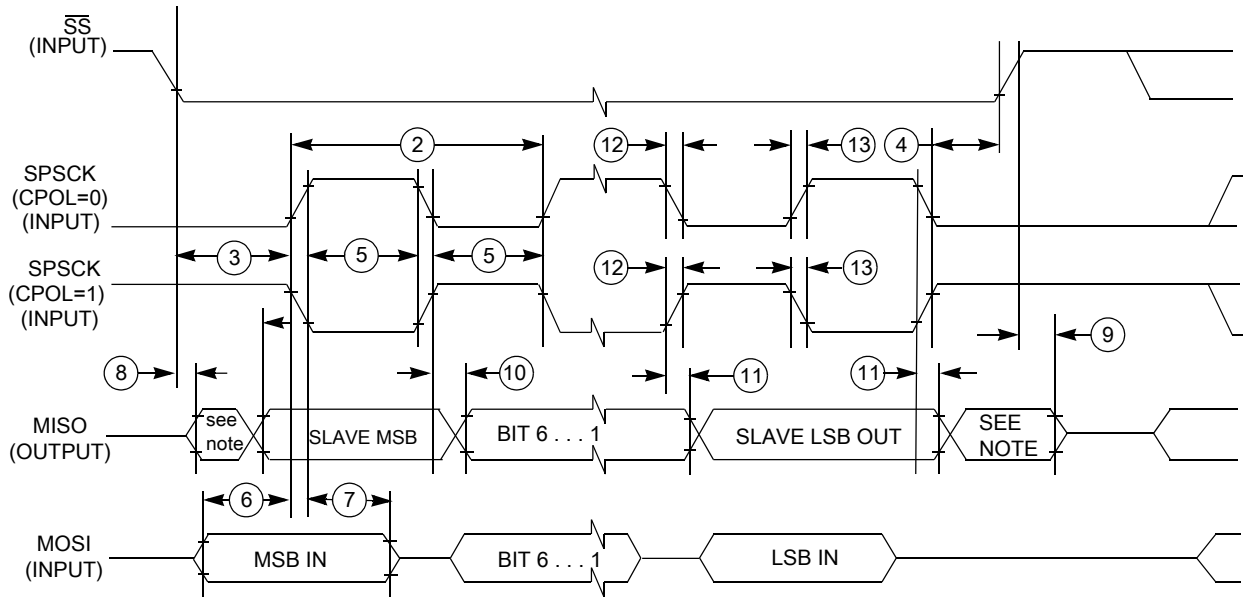


Figure 19. LPSPI slave mode timing (CPHA = 0)

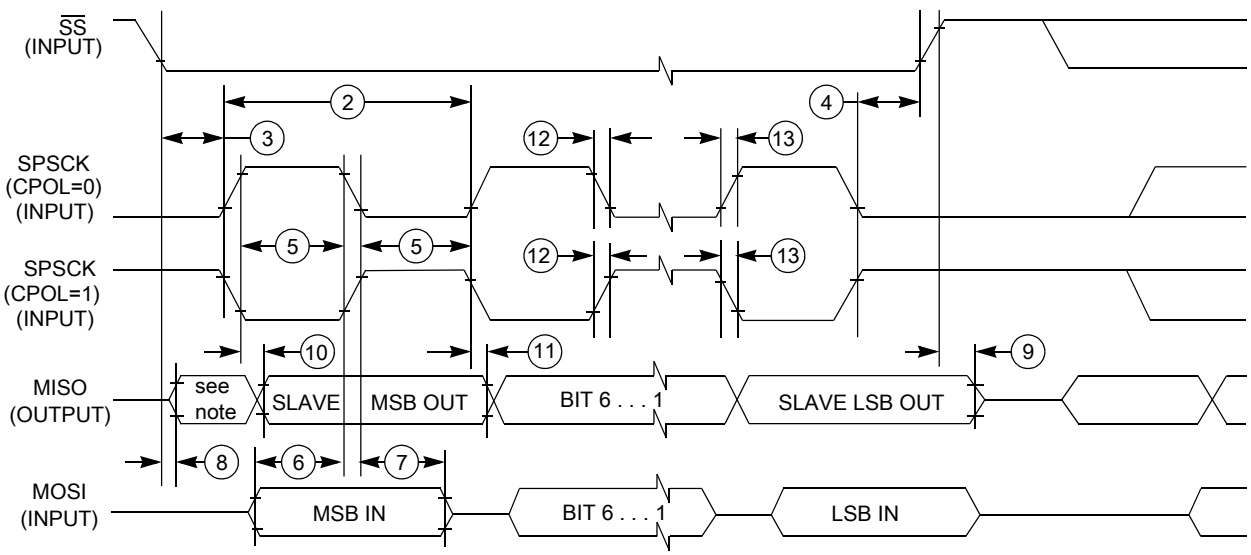


Figure 20. LPSPI slave mode timing (CPHA = 1)

6.5.3 LPI2C electrical specifications

See General AC specifications for LPI2C specifications.

For supported baud rate see section 'Chip-specific LPI2C information' of the *Reference Manual.*

6.5.4 FlexCAN electical specifications

For supported baud rate, see section 'Protocol timing' of the *Reference Manual*.

6.5.5 SAI electrical specifications

The following table describes the SAI electrical characteristics.

- Measurements are with maximum output load of 50 pF, input transition of 1 ns and pad configured with fastest slew settings (DSE = 1'b1).
- I/O operating voltage ranges from 2.97 V to 3.6 V
- While doing the mode transition (RUN -> HSRUN or HSRUN -> RUN), the interface should be OFF.

Table 30. Master mode timing specifications

Symbol	Description	Min.	Max.	Unit
—	Operating voltage	2.97	3.6	V
S1	SAI_MCLK cycle time	40	—	ns
S2	SAI_MCLK pulse width high/low	45%	55%	MCLK period
S3	SAI_BCLK cycle time	80	—	ns
S4	SAI_BCLK pulse width high/low	45%	55%	BCLK period
S5	SAI_RXD input setup before SAI_BCLK	28	—	ns
S6	SAI_RXD input hold after SAI_BCLK	0	—	ns
S7	SAI_BCLK to SAI_TXD output valid	—	8	ns
S8	SAI_BCLK to SAI_TXD output invalid	-2	—	ns
S9	SAI_FS input setup before SAI_BCLK	28	—	ns
S10	SAI_FS input hold after SAI_BCLK	0	—	ns
S11	SAI_BCLK to SAI_FS output valid	—	8	ns
S12	SAI_BCLK to SAI_FS output invalid	-2	—	ns

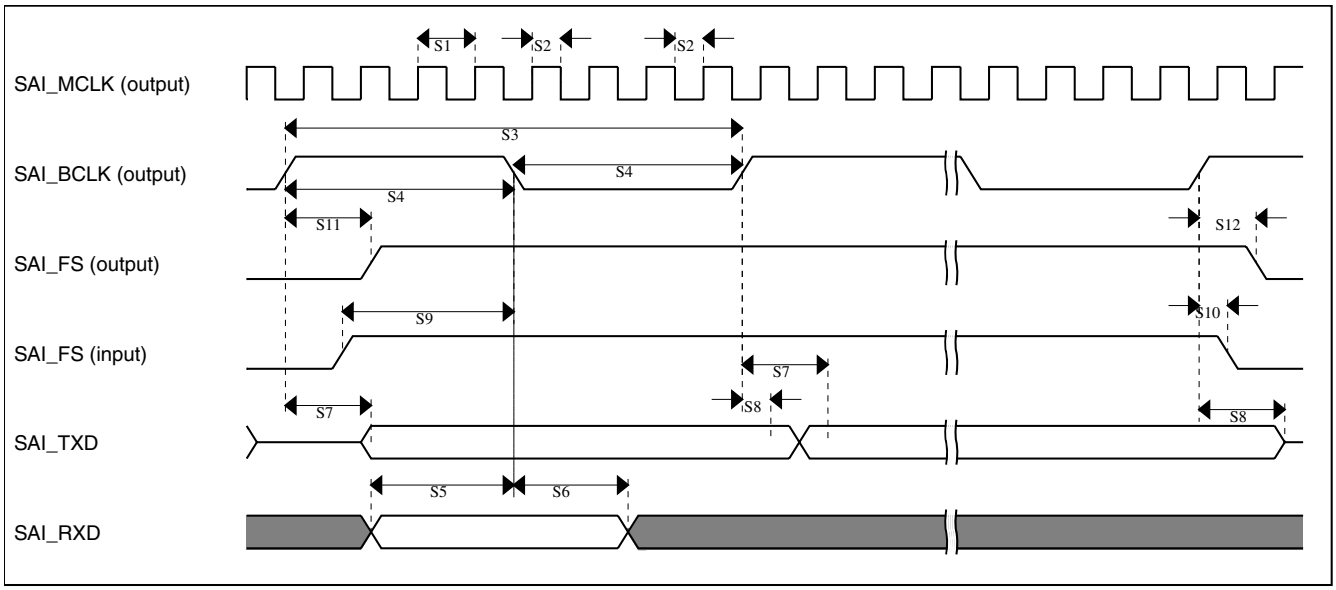


Figure 21. SAI Timing — Master modes

Table 31. Slave mode timing specifications

Symbol	Description	Min.	Max.	Unit
—	Operating voltage	2.97	3.6	V
S13	SAI_BCLK cycle time (input)	80	—	ns
S14[1]	SAI_BCLK pulse width high/low (input)	45%	55%	BCLK period
S15	SAI_RXD input setup before SAI_BCLK	8	—	ns
S16	SAI_RXD input hold after SAI_BCLK	2	—	ns
S17	SAI_BCLK to SAI_TXD output valid	—	28	ns
S18	SAI_BCLK to SAI_TXD output invalid	0	—	ns
S19	SAI_FS input setup before SAI_BCLK	8	—	ns
S20	SAI_FS input hold after SAI_BCLK	2	—	ns
S21	SAI_BCLK to SAI_FS output valid	—	28	ns
S22	SAI_BCLK to SAI_FS output invalid	0	—	ns

1. The slave mode parameters (S15 - S22) assume 50% duty cycle on SAI_BCLK input. Any change in SAI_BCLK duty cycle input must be taken care during the board design or by the master timing.

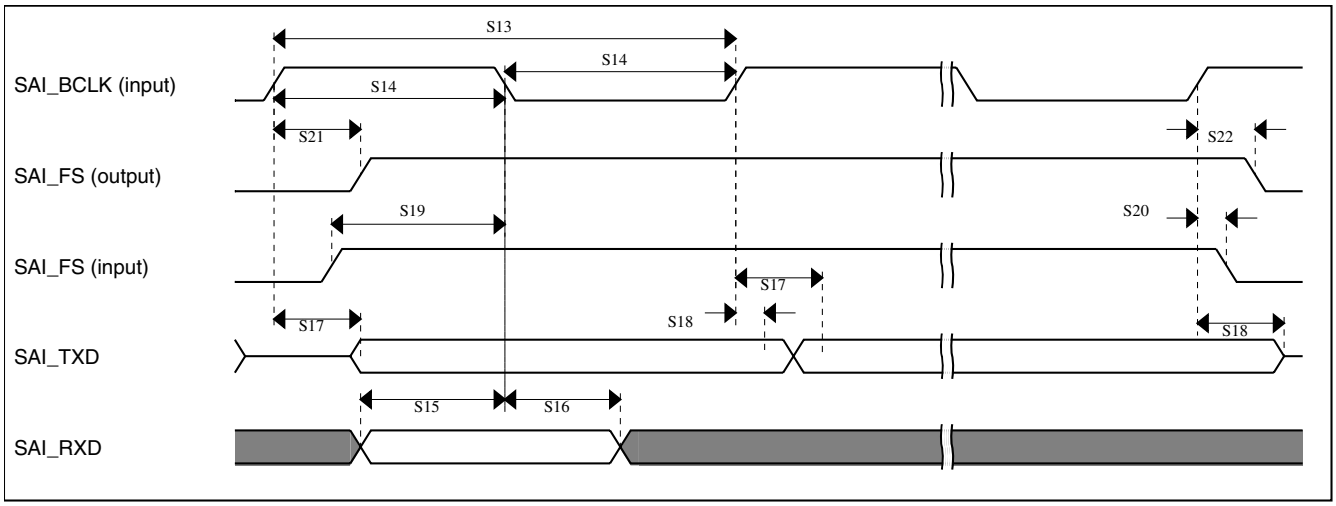


Figure 22. SAI Timing — Slave modes

6.5.6 Ethernet AC specifications

The following timing specs are defined at the chip I/O pin and must be translated appropriately to arrive at timing specs/constraints for the physical interface.

The following table describes the MII electrical characteristics.

- Measurements are with maximum output load of 25 pF, input transition of 1 ns and pad configured with fastest slew settings (DSE = 1'b1).
- I/O operating voltage ranges from 2.97 V to 3.6 V
- While doing the mode transition (RUN -> HSRUN or HSRUN -> RUN), the interface should be OFF.

Table 32. MII signal switching specifications

Symbol	Description	Min.	Max.	Unit
—	RXCLK frequency	—	25	MHz
MII1	RXCLK pulse width high	35%	65%	RXCLK period
MII2	RXCLK pulse width low	35%	65%	RXCLK period
MII3	RXD[3:0], RXDV, RXER to RXCLK setup	5	—	ns
MII4	RXCLK to RXD[3:0], RXDV, RXER hold	5	—	ns
—	TXCLK frequency	—	25	MHz
MII5	TXCLK pulse width high	35%	65%	TXCLK period
MII6	TXCLK pulse width low	35%	65%	TXCLK period
MII7	TXCLK to TXD[3:0], TXEN, TXER invalid	2	—	ns
MII8	TXCLK to TXD[3:0], TXEN, TXER valid	—	25	ns

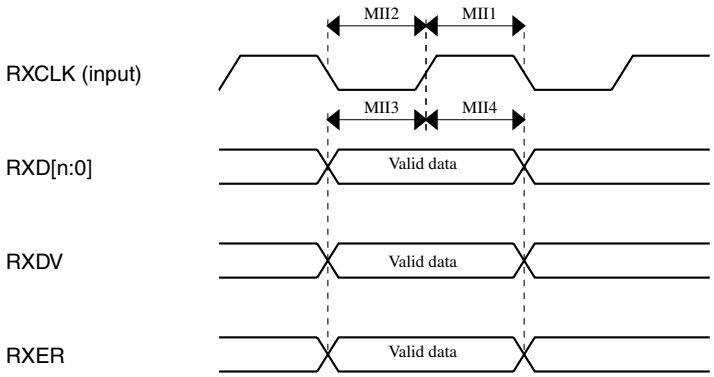


Figure 23. MII receive diagram

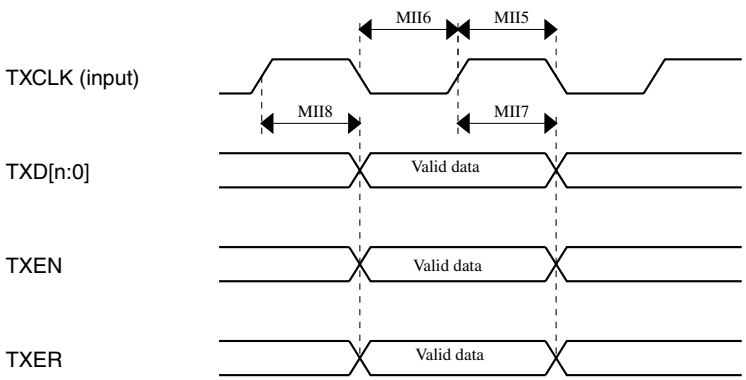


Figure 24. MII transmit signal diagram

The following table describes the RMII electrical characteristics.

- Measurements are with maximum output load of 25 pF, input transition of 1 ns and pad configured with fastest slew settings (DSE = 1'b1).
- I/O operating voltage ranges from 2.97 V to 3.6 V
- While doing the mode transition (RUN -> HSRUN or HSRUN -> RUN), the interface should be OFF.

Table 33. RMII signal switching specifications

Symbol	Description	Min.	Max.	Unit
—	RMII input clock RMII_CLK Frequency	—	50	MHz
RMII1, RMII5	RMII_CLK pulse width high	35%	65%	RMII_CLK period
RMII2, RMII6	RMII_CLK pulse width low	35%	65%	RMII_CLK period
RMII3	RXD[1:0], CRS_DV, RXER to RMII_CLK setup	4	—	ns
RMII4	RMII_CLK to RXD[1:0], CRS_DV, RXER hold	2	—	ns

Table continues on the next page...

Table 33. RMII signal switching specifications (continued)

Symbol	Description	Min.	Max.	Unit
RMII7	RMII_CLK to TXD[1:0], TXEN invalid	2	—	ns
RMII8	RMII_CLK to TXD[1:0], TXEN valid	—	15	ns

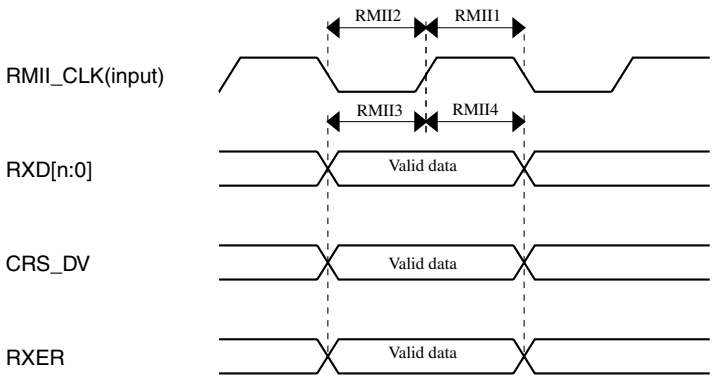


Figure 25. RMII receive diagram

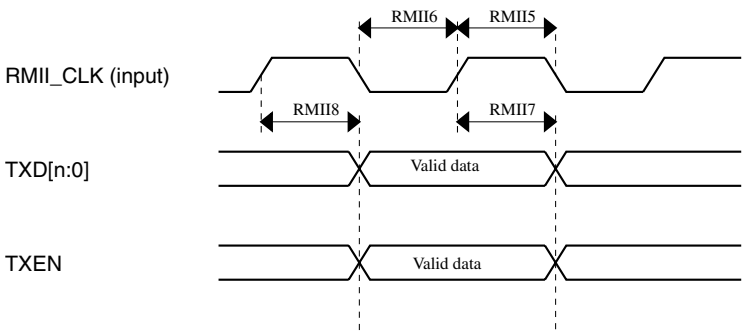


Figure 26. RMII transmit diagram

The following table describes the MDIO electrical characteristics.

- Measurements are with maximum output load of 25 pF, input transition of 1 ns and pad configured with fastest slew settings (DSE = 1'b1).
- I/O operating voltage ranges from 2.97 V to 3.6 V
- While doing the mode transition (RUN -> HSRUN or HSRUN -> RUN), the interface should be OFF.
- MDIO pin must have external Pull-up.

Table 34. MDIO timing specifications

Symbol	Description	Min.	Max.	Unit
—	MDC Clock Frequency	—	2.5	MHz

Table continues on the next page...

Table 34. MDIO timing specifications (continued)

Symbol	Description	Min.	Max.	Unit
MDC1	MDC pulse width high	40%	60%	MDC period
MDC2	MDC pulse width low	40%	60%	MDC period
MDC3	MDIO (input) to MDC rising edge setup	25	—	ns
MDC4	MDIO (input) to MDC rising edge hold	0	—	ns
MDC5	MDC falling edge to MDIO output valid (maximum propagation delay)	—	25	ns
MDC6	MDC falling edge to MDIO output invalid (minimum propagation delay)	-10	—	ns

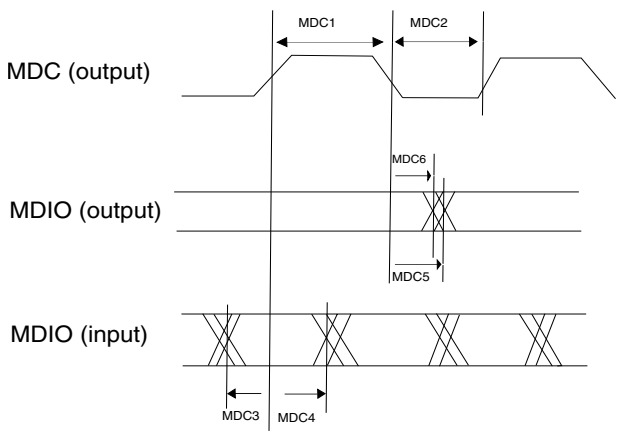


Figure 27. MII/RMII serial management channel timing diagram

6.5.7 Clockout frequency

Maximum supported clock out frequency for this device is 20 MHz

6.6 Debug modules

6.6.1 SWD electrical specofications

Table 35. SWD electrical specifications

Symbol	Description	Run Mode				HSRUN Mode				VLPR Mode				Unit
		5.0 V IO		3.3 V IO		5.0 V IO		3.3 V IO		5.0 V IO		3.3 V IO		
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
S1	SWD_CLK frequency of operation	-	25	-	25	-	25	-	25	-	10	-	10	MHz
S2	SWD_CLK cycle period	1/S1	-	1/S1	-	1/S1	-	1/S1	-	1/S1	-	1/S1	-	ns
S3	SWD_CLK clock pulse width	S2/2 - 5	S2/2 + 5	S2/2 - 5	S2/2 + 5	S2/2 - 5	S2/2 + 5	S2/2 - 5	S2/2 + 5	S2/2 - 5	S2/2 + 5	S2/2 - 5	S2/2 + 5	ns
S4	SWD_CLK rise and fall times	-	1	-	1	-	1	-	1	-	1	-	1	ns
S9	SWD_DIO input data setup time to SWD_CLK rise	4	-	4	-	4	-	4	-	16	-	16	-	ns
S10	SWD_DIO input data hold time after SWD_CLK rise	3	-	3	-	3	-	3	-	10	-	10	-	ns
S11	SWD_CLK high to SWD_DIO data valid	-	28	-	38	-	28	-	38	-	70	-	77	ns
S12	SWD_CLK high to SWD_DIO high-Z	-	28	-	38	-	28	-	38	-	70	-	77	ns
S13	SWD_CLK high to SWD_DIO data invalid	0	-	0	-	0	-	0	-	0	-	0	-	ns

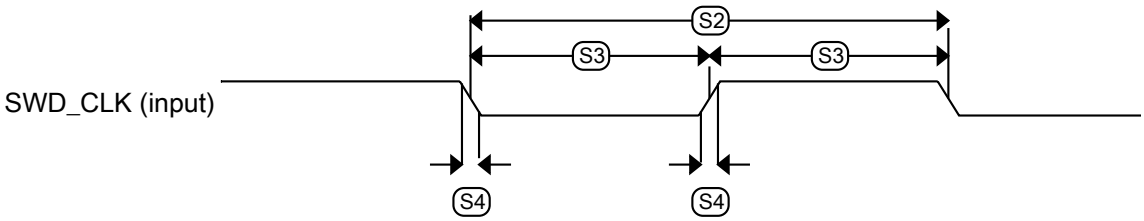


Figure 28. Serial wire clock input timing

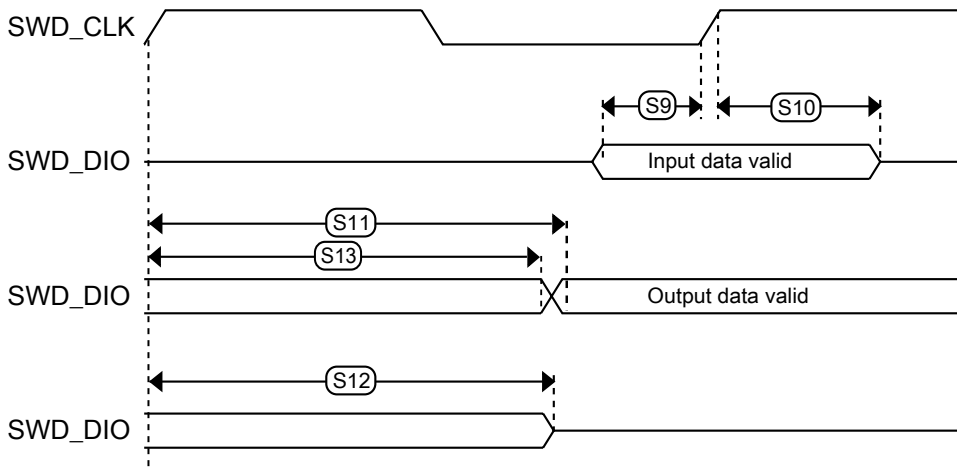


Figure 29. Serial wire data timing

6.6.2 Trace electrical specifications

The following table describes the Trace electrical characteristics.

- Measurements are with maximum output load of 50 pF, input transition of 1 ns and pad configured with fastest slew settings (DSE = 1'b1).
- While doing the mode transition (RUN -> HSRUN or HSRUN -> RUN), the interface should be OFF.

Table 36. Trace specifications

	Symbol	Description	RUN Mode			HSRUN Mode		VLPR Mode	Unit
—	Fsys	System frequency	80	48	40	112	80	4	MHz

Table continues on the next page...

Table 36. Trace specifications (continued)

	Symbol	Description	RUN Mode			HSRUN Mode		VLPR Mode	Unit
Trace on fast pads	f_{TRACE}	Max Trace frequency	80	48	40	74.667	80	4	MHz
	t_{DVO}	Data Output Valid	4	4	4	4	4	20	ns
	t_{DIV}	Data Output Invalid	-2	-2	-2	-2	-2	-10	ns
Trace on slow pads	f_{TRACE}	Max Trace frequency	22.86	24	20	22.4	22.86	4	MHz
	t_{DVO}	Data Output Valid	8	8	8	8	8	20	ns
	t_{DIV}	Data Output Invalid	-4	-4	-4	-4	-4	-10	ns

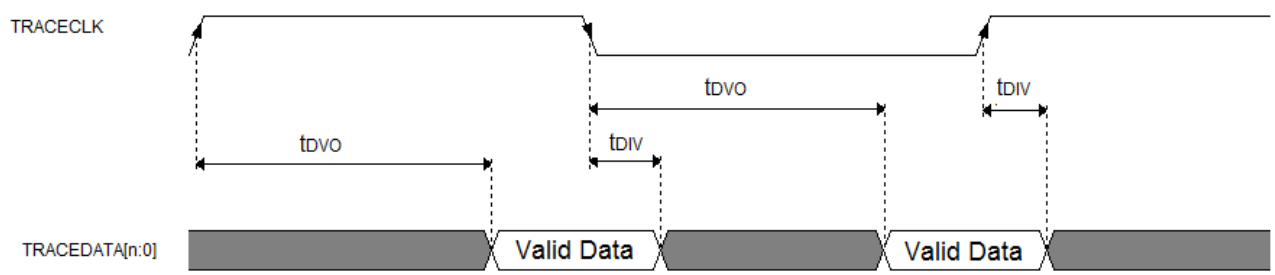


Figure 30. TRACE CLKOUT specifications

6.6.3 JTAG electrical specifications

Table 37. JTAG electrical specifications

Symbol	Description	Run Mode				HSRUN Mode				VLPR Mode				Unit
		5.0 V IO		3.3 V IO		5.0 V IO		3.3 V IO		5.0 V IO		3.3 V IO		
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
JI	TCLK frequency of operation													MHz
	Boundary Scan	-	20	-	20	-	20	-	20	-	10	-	10	
	JTAG	-	20	-	20	-	20	-	20	-	10	-	10	
J2	TCLK cycle period	1/JI	-	1/JI	-	1/JI	-	1/JI	-	1/JI	-	1/JI	-	ns
J3	TCLK clock pulse width													ns
	Boundary Scan	J2/2 - 5	J2/2 + 5	J2/2 - 5	J2/2 + 5	J2/2 - 5	J2/2 + 5	J2/2 - 5	J2/2 + 5	J2/2 - 5	J2/2 + 5	J2/2 - 5	J2/2 + 5	
	JTAG													
J4	TCLK rise and fall times	-	1	-	1	-	1	-	1	-	1	-	1	ns
J5	Boundary scan input data setup time to TCLK rise	5	-	5	-	5	-	5	-	15	-	15	-	ns
J6	Boundary scan input data hold time after TCLK rise	5	-	5	-	5	-	5	-	8	-	8	-	ns
J7	TCLK low to boundary scan output data valid	-	28	-	32	-	28	-	32	-	80	-	80	ns
J8	TCLK low to boundary scan output data invalid	0	-	0	-	0	-	0	-	0	-	0	-	
J9	TCLK low to boundary scan output high-Z	-	28	-	32	-	28	-	32	-	80	-	80	ns
J10	TMS, TDI input data setup time to TCLK rise	3	-	3	-	3	-	3	-	15	-	15	-	ns
J11	TMS, TDI input data hold time after TCLK rise	2	-	2	-	2	-	2	-	8	-	8	-	ns
J12	TCLK low to TDO data valid	-	28	-	32	-	28	-	32	-	80	-	80	ns
J13	TCLK low to TDO data invalid	0	-	0	-	0	-	0	-	0	-	0	-	ns
J14	TCLK low to TDO high-Z	-	28	-	32	-	28	-	32	-	80	-	80	ns

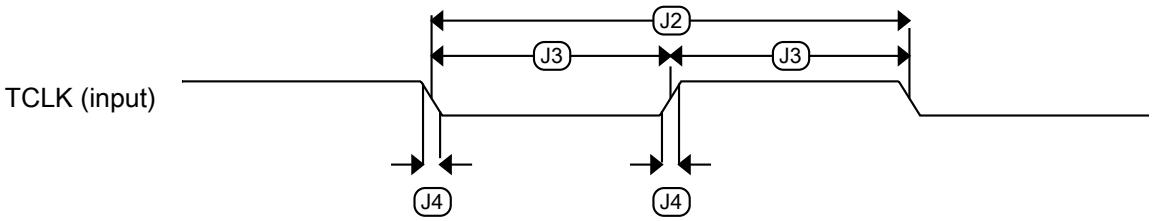


Figure 31. Test clock input timing

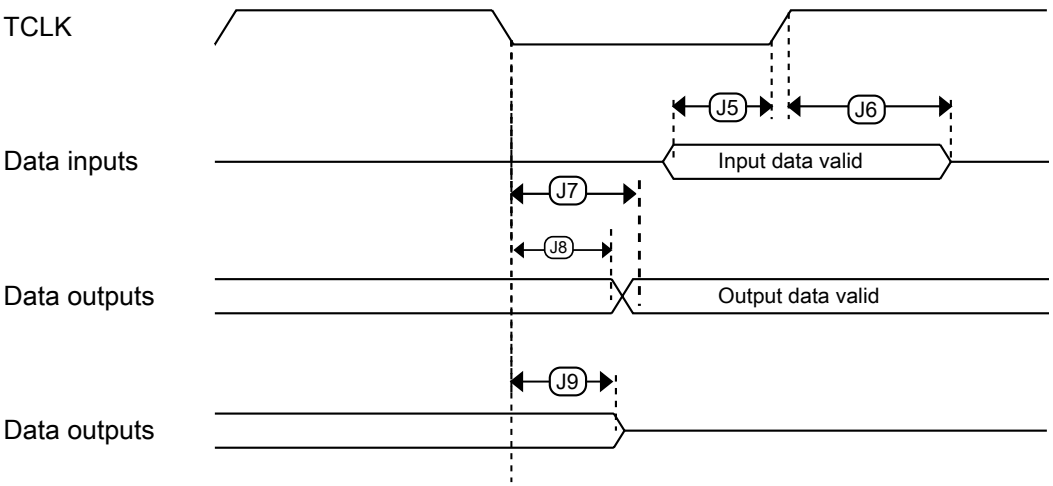


Figure 32. Boundary scan (JTAG) timing

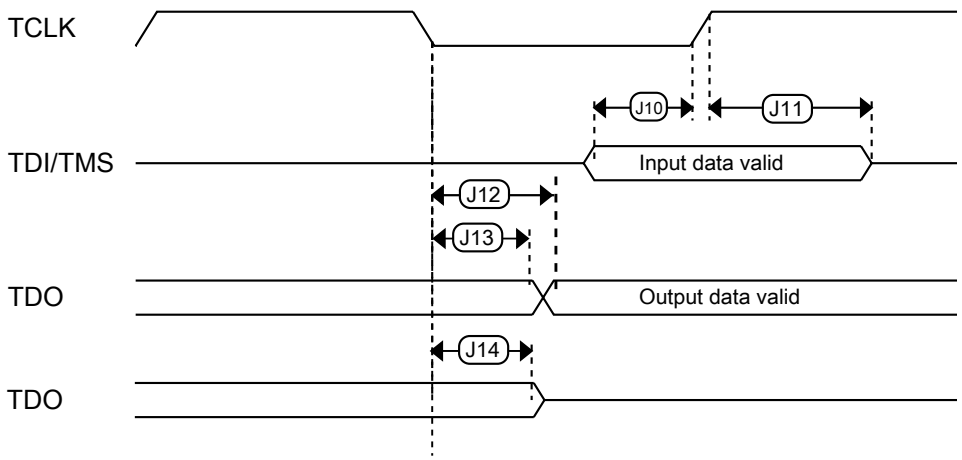


Figure 33. Test Access Port timing

7 Thermal attributes

7.1 Description

The tables in the following sections describe the thermal characteristics of the device.

NOTE

Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting side (board) temperature, ambient temperature, air flow, power dissipation or other components on the board, and board thermal resistance.

7.2 Thermal characteristics

Table 38. Thermal characteristics for the 64/100/144-pin LQFP package

Rating	Conditions	Symbol	Packages	Values			Unit
				MWCT1014S	MWCT1015S	MWCT1016S	
Thermal resistance, Junction to Ambient (Natural Convection)[1, 2]	Single layer board (1s)	$R_{\theta JA}$	64	61	59	NA	°C/W
			100	52	21	NA	°C/W
Thermal resistance, Junction to Ambient (Natural Convection)[1]	Two layer board (1s1p)	$R_{\theta JA}$	64	45	44	NA	°C/W
			100	42	40	NA	°C/W
Thermal resistance, Junction to Ambient (Natural Convection)[1, 2]	Four layer board (2s2p)	$R_{\theta JA}$	64	43	41	NA	°C/W
			100	40	39	NA	°C/W
Thermal resistance, Junction to Ambient (@200 ft/min)[1, 3]	Single layer board (1s)	$R_{\theta JMA}$	64	49	48	NA	°C/W
			100	42	41	NA	°C/W
Thermal resistance, Junction to Ambient (@200 ft/min)[1]	Two layer board (1s1p)	$R_{\theta JMA}$	64	38	37	NA	°C/W
			100	35	34	NA	°C/W
Thermal resistance, Junction to Ambient (@200 ft/min)[1, 3]	Four layer board (2s2p)	$R_{\theta JMA}$	64	36	35	NA	°C/W
			100	34	33	NA	°C/W
Thermal resistance, Junction to Board[4]	—	$R_{\theta JB}$	64	25	23	NA	°C/W
			100	25	24	NA	°C/W
Thermal resistance, Junction to Case [5]	—	$R_{\theta JC}$	64	12	11	NA	°C/W
			100	12	11	NA	°C/W
Thermal resistance, Junction to Package Top[6]	Natural Convection	Ψ_{JT}	64	2	2	NA	°C/W
			100	2	2	NA	°C/W

1. Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.
2. Per JEDEC JESD51-2 with natural convection for horizontally oriented board. Board meets JESD51-9 specification for 1s or 2s2p board, respectively.
3. Per JEDEC JESD51-6 with forced convection for horizontally oriented board. Board meets JESD51-9 specification for 1s or 2s2p board, respectively.
4. Thermal resistance between the die and the printed circuit board per JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.
5. Thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC-883 Method 1012.1).
6. Thermal characterization parameter indicating the temperature difference between package top and the junction temperature per JEDEC JESD51-2. When Greek letters are not available, the thermal characterization parameter is written as Psi-JT.

7.3 General notes for specifications at maximum junction temperature

An estimation of the chip junction temperature, T_J, can be obtained from this equation:

$$T_J = T_A + (R_{\theta JA} \times P_D)$$

where:

- T_A = ambient temperature for the package (°C)
- $R_{\theta JA}$ = junction to ambient thermal resistance (°C/W)
- P_D = power dissipation in the package (W)

The junction to ambient thermal resistance is an industry standard value that provides a quick and easy estimation of thermal performance. Unfortunately, there are two values in common usage: the value determined on a single layer board and the value obtained on a board with two planes. For packages such as the PBGA, these values can be different by a factor of two. Which value is closer to the application depends on the power dissipated by other components on the board. The value obtained on a single layer board is appropriate for the tightly packed printed circuit board. The value obtained on the board with the internal planes is usually appropriate if the board has low power dissipation and the components are well separated.

When a heat sink is used, the thermal resistance is expressed in the following equation as the sum of a junction-to-case thermal resistance and a case-to-ambient thermal resistance:

$$R_{\theta JA} = R_{\theta JC} + R_{\theta CA}$$

where:

- $R_{\theta JA}$ = junction to ambient thermal resistance (°C/W)
- $R_{\theta JC}$ = junction to case thermal resistance (°C/W)
- $R_{\theta CA}$ = case to ambient thermal resistance (°C/W)

$R_{\theta JC}$ is device related and cannot be influenced by the user. The user controls the thermal environment to change the case to ambient thermal resistance, $R_{\theta CA}$. For instance, the user can change the size of the heat sink, the air flow around the device, the interface material, the mounting arrangement on printed circuit board, or change the thermal dissipation on the printed circuit board surrounding the device.

To determine the junction temperature of the device in the application when heat sinks are not used, the Thermal Characterization Parameter (Ψ_{JT}) can be used to determine the junction temperature with a measurement of the temperature at the top center of the package case using this equation:

$$T_J = T_T + (\Psi_{JT} \times P_D)$$

where:

- T_T = thermocouple temperature on top of the package (°C)
- Ψ_{JT} = thermal characterization parameter (°C/W)
- P_D = power dissipation in the package (W)

The thermal characterization parameter is measured per JESD51-2 specification using a 40 gauge type T thermocouple epoxied to the top center of the package case. The thermocouple should be positioned so that the thermocouple junction rests on the package. A small amount of epoxy is placed over the thermocouple junction and over about 1 mm of wire extending from the junction. The thermocouple wire is placed flat against the package case to avoid measurement errors caused by cooling effects of the thermocouple wire.

8 Dimensions

8.1 Obtaining package dimensions

Package dimensions are provided in the package drawings.

To find a package drawing, go to http://www.nxp.com and perform a keyword search for the drawing's document number:

Package option	Document Number
64-pin LQFP	98ASS23234W
100-pin LQFP	98ASS23308W
144-pin LQFP	98ASS23177W

9 Pinouts

9.1 Package pinouts and signal descriptions

For package pinouts and signal descriptions, refer to the Reference Manual.

10 Revision History

The following table provides a revision history for this document.

Table 39. Revision History

Rev. No.	Date	Substantial Changes
Rev. 0	May 2017	• Initial release.

Rev. 1	Dec 2017	• In "Feature comparison" section, updated the "MWCT101xS product series comparison" figure.
		• In Table 1,
		  • Updated note 'All the limits defined ... '
		  • Updated parameter '$I_{INJPAD\_DC\_ABS}$', 'V_{IN_DC}', $I_{INJSUM\_DC\_ABS}$.
		• In Table 2,
		  • Updated min. value of V_{DD_OFF}
		  • Added parameter $I_{INJPAD\_DC\_OP}$ and $I_{INJSUM\_DC\_OP}$.
		• Updated footnote to T_{SPLL_LOCK} and removed I_{DDSPLL} in "SPLL electrical specifications" table.
		• In "12-bit ADC electrical characteristics" section,
		  • Updated table: 12-bit ADC characteristics (2.7 V to 3 V) (VREFH = VDDA, VREFL = VSS)
		  • Added typ. value to I_{DDA_ADC}, TUE, DNL, and INL
		  • Added min. value to SMPLTS
		  • Removed footnote 'All the parameters in this table ... '
		  • Updated table: 12-bit ADC characteristics (3 V to 5.5 V) (VREFH = VDDA, VREFL = VSS)
		  • Added typ. value to I_{DDA_ADC}
		  • Removed footnote 'All the parameters in this table ... '
		• In "Flash command timing specifications" table, updated Max. value of t_{vfykey} to 35 µs
		• Updated "MWCT101xS product series comparison" figure.
		• In Table 5, updated TBDs for V_{LVR_HYST}, V_{LVD_HYST}, and V_{LVW_HYST}
		• In Power mode transition operating behaviors,
		  • Added VLPR → VLPS
		  • Added VLPS → VLPR
		  • Updated TBDs for VLPS → Asynchronous DMA Wakeup, STOP1 → Asynchronous DMA Wakeup, and STOP2 → Asynchronous DMA Wakeup
		• In Table 7, updated the specifications for MWCT1014S.
		• Updated the attachment *MWCT101xS_Power_Modes _Configuration.xlsx*.
		• In "Standard input pin capacitance" table, removed C_{IN_A}.
		• In "External System Oscillator electrical specifications" table,

Table 39. Revision History

Rev. No.	Date	Substantial Changes
		• Updated specifications for g_{mXOSC}. • Removed I_{DDOSC} • In "Fast internal RC Oscillator (FIRC) electrical specifications" section, • Added parameter ΔF125. • Removed I_{DDFIRC} • In "Slow internal RC oscillator (SIRC) electrical specifications" section, • Added parameter ΔF125. • Removed I_{DDSIRC} • In "Low Power Oscillator (LPO) electrical specifications" section, removed I_{LPO} • Updated section: "Flash memory module (FTFC) electrical specifications" • In section: "12-bit ADC electrical characteristics", • Updated TBDs in Table 25. • Updated TBDs in Table 26. • In section: QuadSPI AC specifications, updated figure 'QuadSPI output timing (HyperRAM mode) diagram'. • In section: "ADC electrical specifications", updated 12-bit ADC operating conditions. • In section: "CMP with 8-bit DAC electrical specifications", added note 'For comparator IN signals adjacent ... ' • In table: LPSPI electrical specifications, minor update in footnote 6. • In table: Table 38, updated specifications for MWCT1015S.

How to Reach Us:

Home Page:
nxp.com

Web Support:
nxp.com/support

Document Number: MWCT101xSF
Rev. 1
02/2018