AN11007

Single stage 5-6 GHz WLAN LNA with BFU730F

Rev. 2 — 20 November 2012 | Application note

document information

Info	Content
Keywords	BFU730F, LNA, 802.11a & 802.11n MIMO WLAN
Abstract	The document provides circuit, layout, BOM and performance information on 5-6 GHz band LNA equipped with NXP's BFU730F wide band transistor. This Application note is related to evaluation board OM7691/BFU730F,598 12nC 934065628598

Revision history

Rev	Date	Description
1	20110104	Initial document.
2	20121120	Chapter added about switching time.

Contact information

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1. Introduction

The BFU730F is a discrete HBT that is produced using NXP Semiconductors' advanced 110 GHz f_T SiGe:C BiCmos process. SiGe:C is a normal silicon germanium process with the addition of Carbon in the base layer of the NPN transistor. The presence of carbon in the base layer suppresses the boron diffusion during wafer processing. This allows steeper and narrower SiGe HBT base and a heavier doped base. As a result, lower base resistance, lower noise and higher cut off frequency can be achieved.

The BFU730F is one of a series of transistors made in SiGe:C.

BFU710F; BFU760 and BFU790 are the other types, BFU710 is intended for ultra low current applications. The BFU760F and BFU790F are high current types and are intended for application where linearity is key.

The BFU7XXF are ideal in all kind of applications where cost matters. It also gives design flexibility.

2. Requirements and design of the 5-6 GHz WLAN LNA

The circuit shown in this application note is intended to demonstrate the performance of the BFU730 in a 5-6 GHz LNA for e.g. 802.11 & 802.11n "MIMO" WLAN applications. Key requirements for this application as are:

- NF
- Gain
- Turn on turn of time
- Linearity.

The target for this circuit is listed in table 1.

Table 1. Target spec.

Target specification of the 5-6GHz LNA.

Vcc	Icc	NF	Gain	IRL	ORL
3	10	<2	>15	>10	>10
V	mA	dB	dB	dB	dB

3. Design

The 5-6 GHz LNA consists of one stage BFU730F amplifier. For this amplifier 12 external components are used, for matching, biasing and decoupling.

The design has been conducted using Agilent's Advanced Design System (ADS). The 2D EM Momentum tool has been used to co simulate the PCB see Fig 1. Results are given in paragraph 4.5.

The LNA shows a Gain of 14 dB @5.5 GHz, NF of 1.3 dB, with only 10 mA it shows a high input P1 dB compression of –7.5 dBm, as well as a input IP3 of +10 dBm.

Finally the LNA is unconditional stable 10 MHz-20 GHz.

3.1 BFU730F 5-6 GHz-ADS Simulation circuit

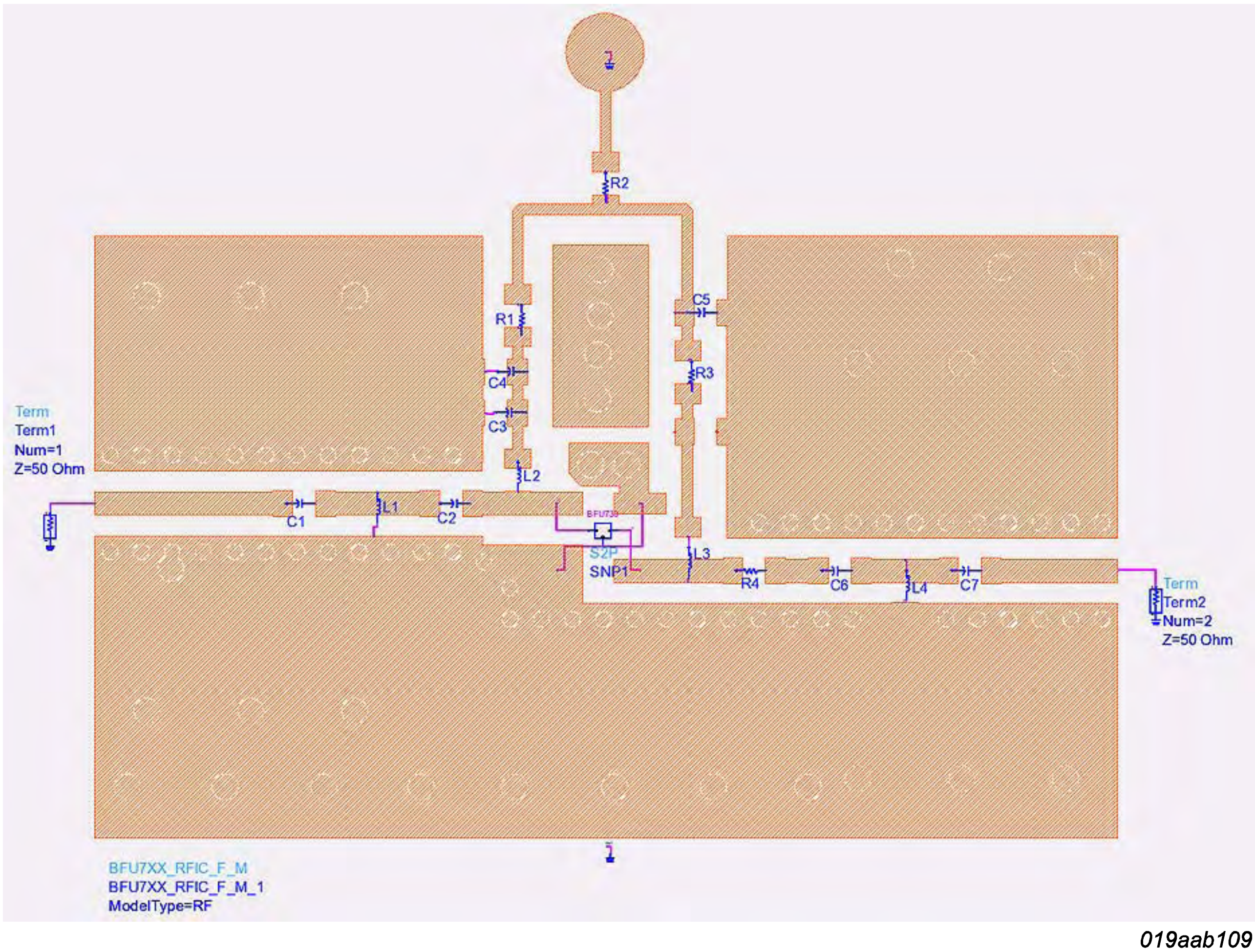


Fig 1. ADS simulation circuit for 5-6 GHz WLAN LNA

3.2 BFU730F 5-6 GHz - ADS Gain and match simulation results

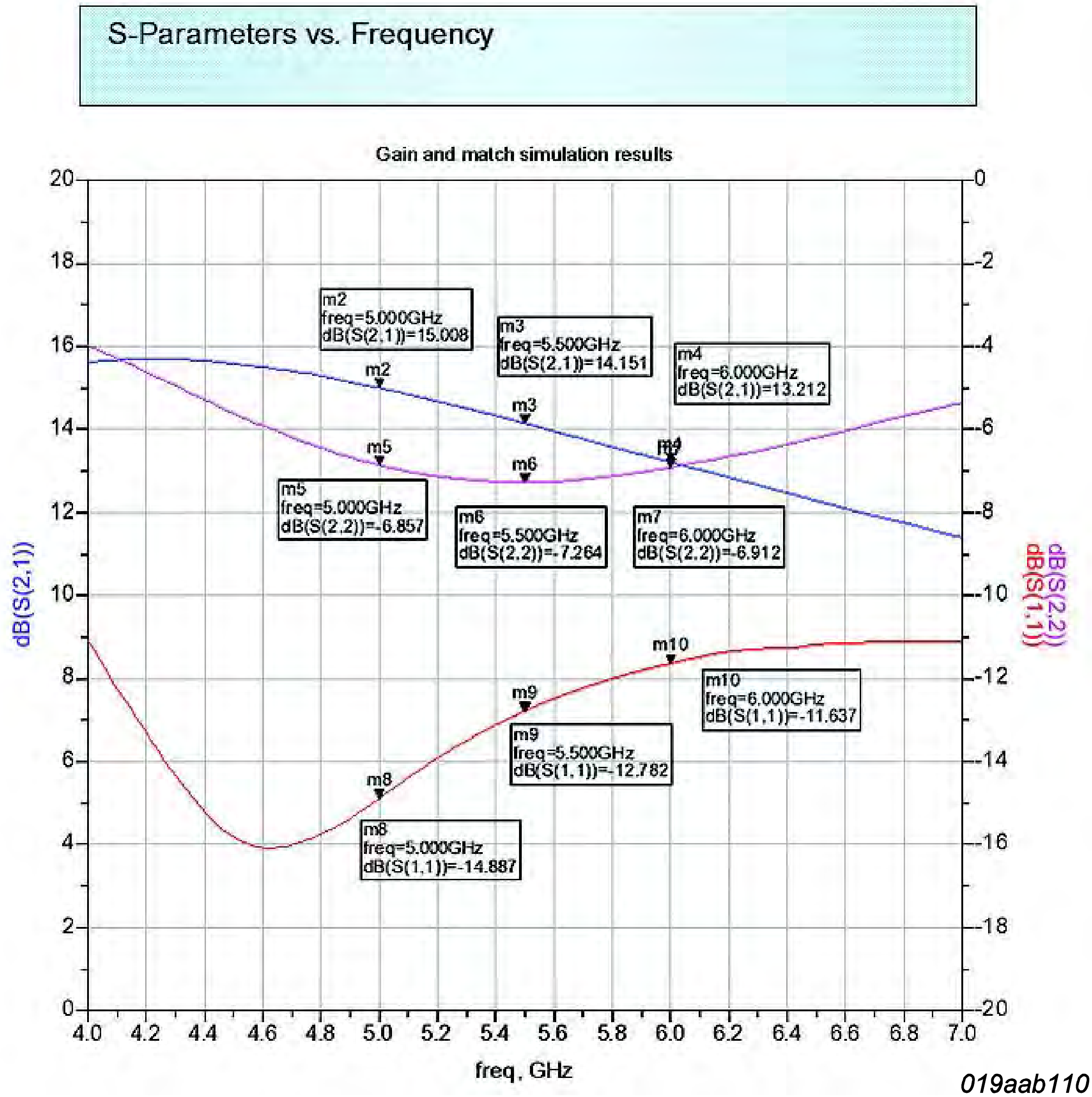


Fig 2. ADS Gain and match simulation results for 5-6 GHz WLAN LNA

3.3 BFU730F 5-6 GHz-ADS NF simulation

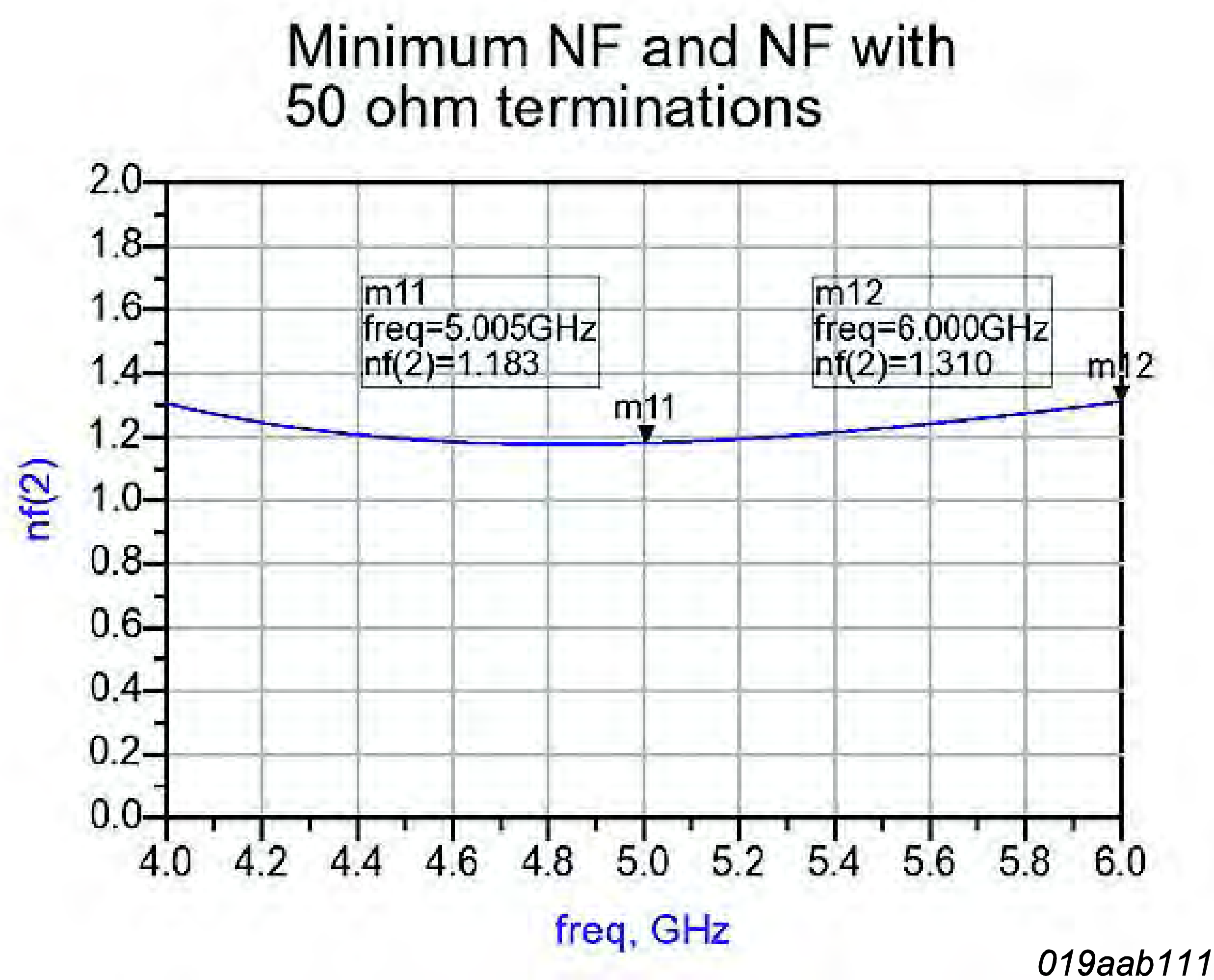
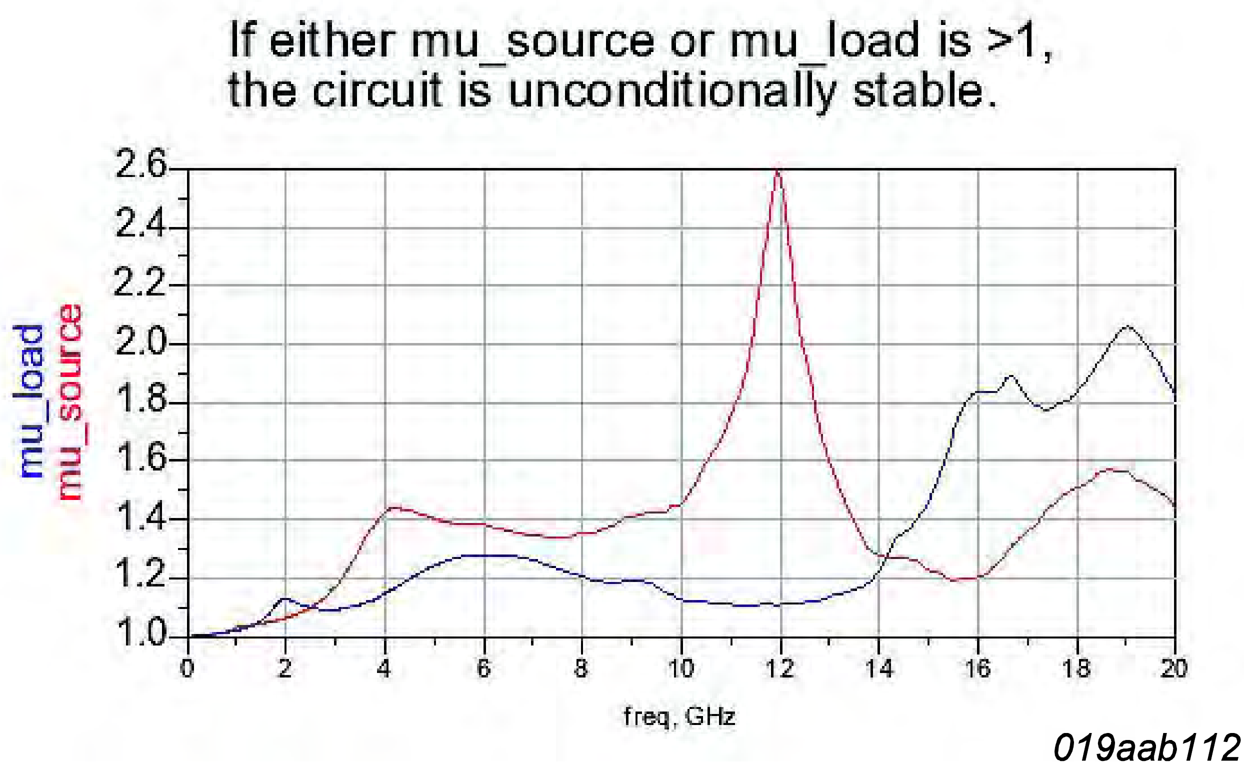


Fig 3. ADS Noise Figure simulation results of 5-6 GHz WLAN LNA

3.4 BFU730F 5-6 GHz-ADS Stability simulation



As K≥1 and Mu≥1, the LNA is unconditionally stable for the whole frequency band

Fig 4. ADS stability simulation results of 5-6 GHz WLAN LNA

4. Implementation

4.1 Schematic

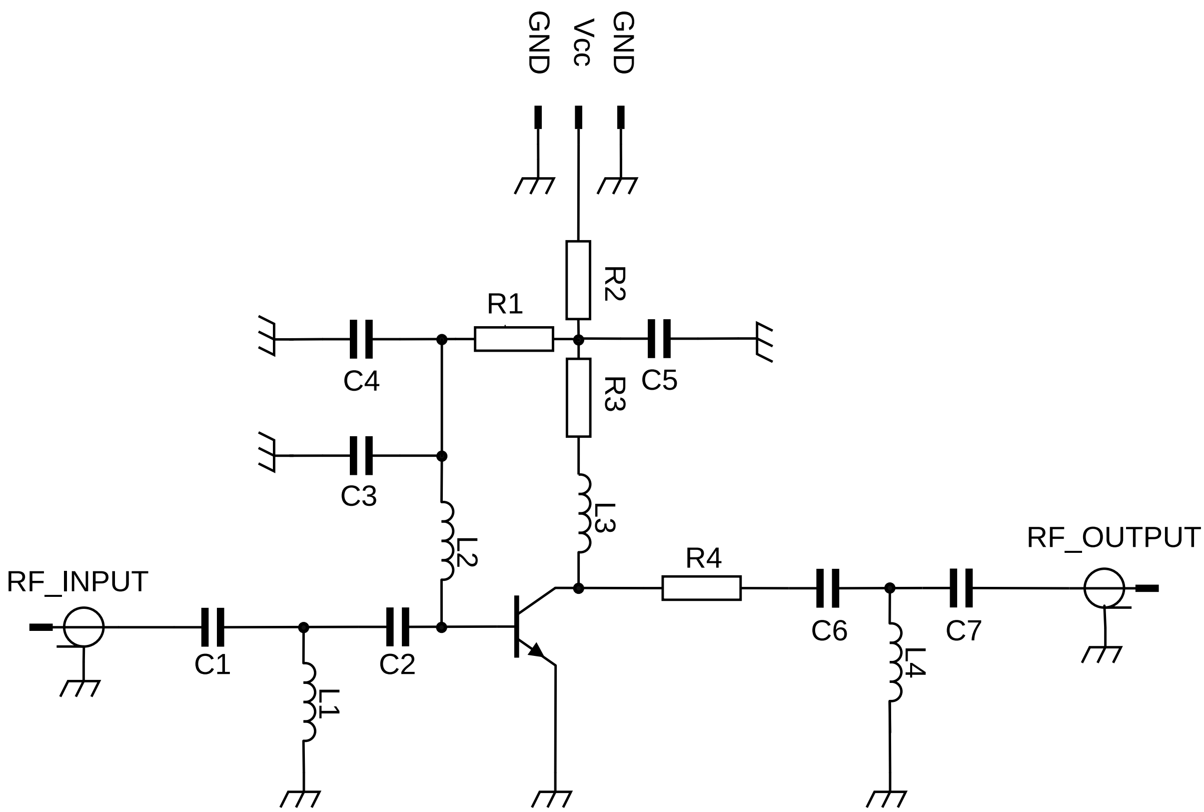


Fig 5. 5-6 GHz LNA schematic (019aab113)

4.2 Layout and assembly

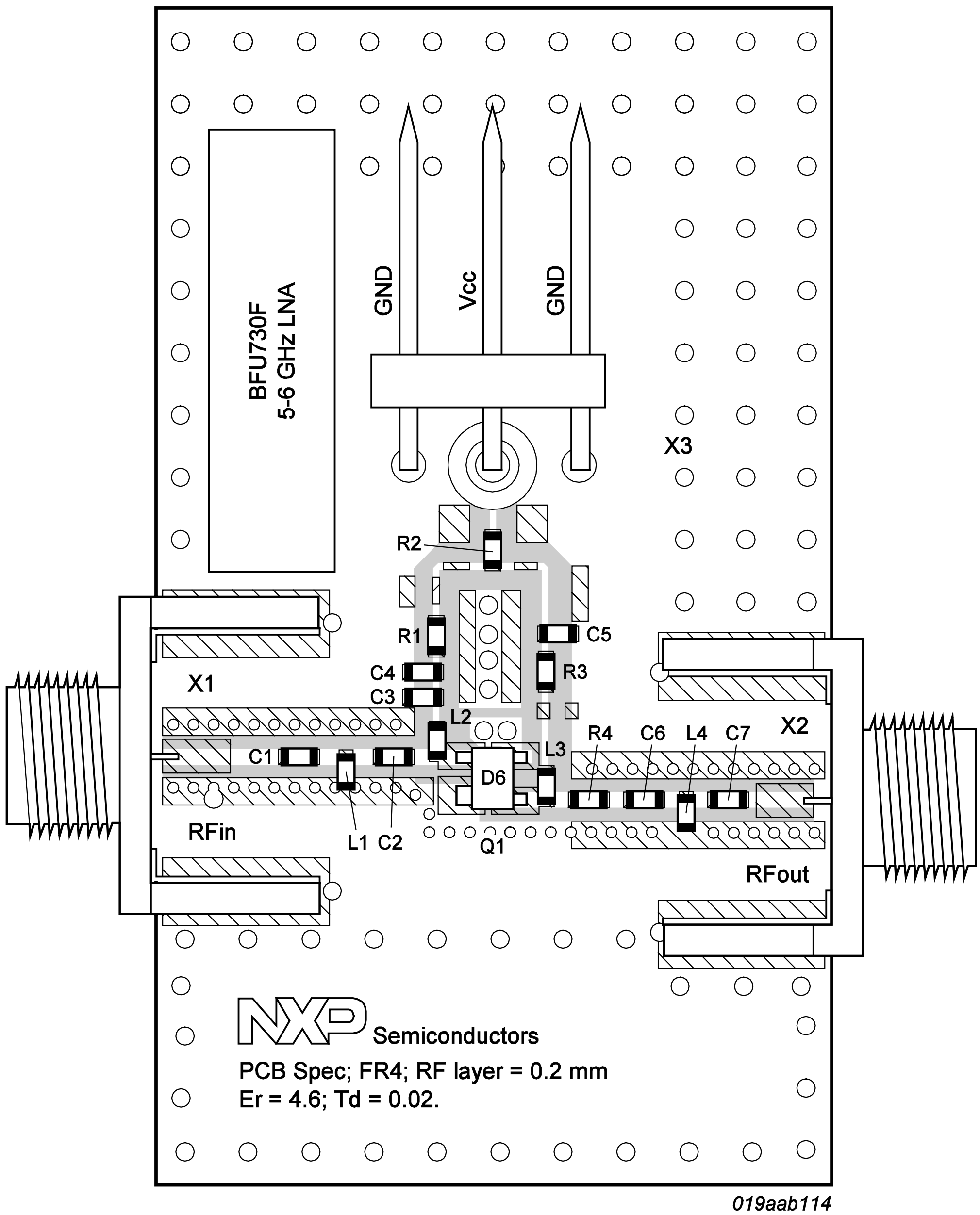


Fig 6. Layout and assembly info of 5-6 GHz LNA

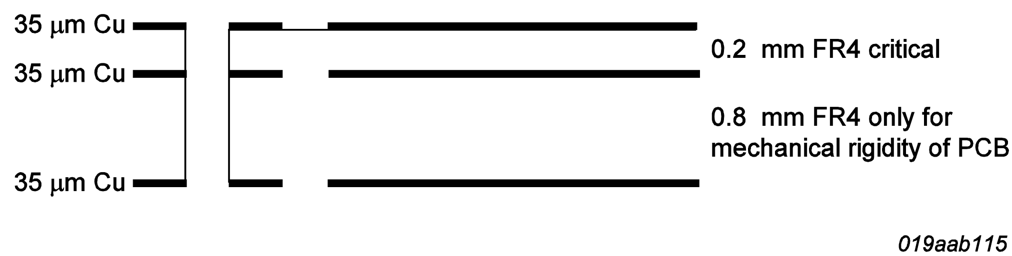
Table 2. Bill of materials

Designator	Description	Size	Value	Type	Note
Q1	BFU730F	2X2 mm		NXP Semiconductors	HBT
PCB		20X35 mm			
C1,C7	Capacitor	0402	3.9 pF	MurataGRM1555	input/output match
C2,C6	Capacitor	0402	0.75 pF	MurataGRM1555	input/output match
C3	Capacitor	0402	15 nF	MurataGRM1555	
C4	Capacitor	0402	1.5 pF	MurataGRM1555	
C5	Capacitor	0402	1.5 pF	MurataGRM1555	
L1,L4	Inductor	0402	1.5 nH	Murata LQP15	input/output match
L2	Inductor	0402	9.1 nH	Murata LQW15	input match
L3	Inductor	0402	5.1 nH	Murata LQW15	output match
R1	Resistor	0402	37 K		Bias Setting
R2	Resistor	0402	100 Ohm		Bias Setting Hfe and Temp spread cancellation
R3	Resistor	0402	10 Ohm		Stability
R4	Resistor	0402	0 Ohm		NA
X1,X2	SMA RF connector	-		Johnson, End launch SMA 142-0701-841	RF input/ RF output
X3	DC header	-		Molex, PCB header, Right Angle, 1 row, 3 way 90121-0763	Bias connector

4.3 PCB layout.

A good PCB Layout is an essential part of an RF circuit design. The EVB of the BFU730 can serve as a guideline for laying out a board using either the BFU730 or one of the other SiGe.C HBTs in the SOT343F package. Use controlled impedance lines for all high frequency inputs and outputs. Bypass V_{CC} with decoupling capacitors, preferable located as close as possible to the device. For long bias lines it may be necessary to add decoupling capacitors along the line further away from the device. Proper grounding the emitters is also essential for the performance. Either connect the emitters directly to the ground plane ore through vias, or do both.

The material that has been used for the EVB is FR4 using the stack shown in Fig 7.



(1) Material supplier is Isola Duraver; Er=4.6-4.9 Tδ=0.02

Fig 7. PCB material stack

4.4 LNA View

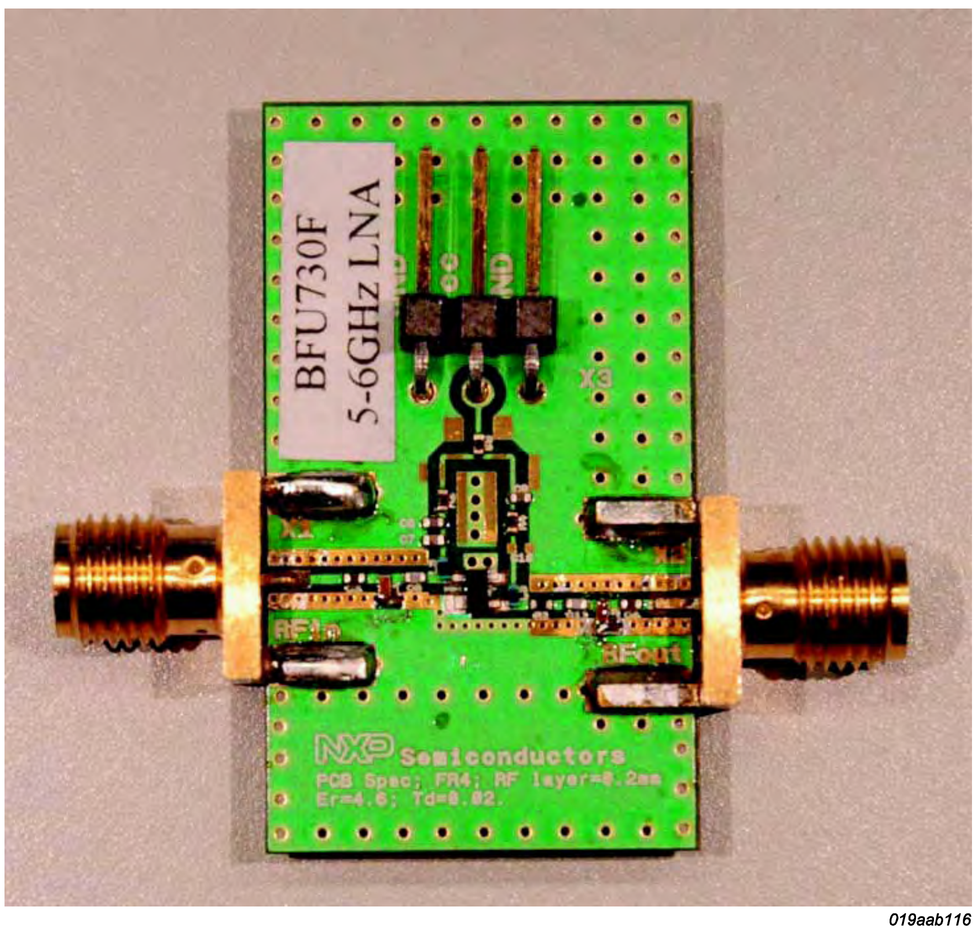


Fig 8. 5-6 GHz LNA EVB

4.5 Measurement results

Table 3. Typical measurement results measured on the evaluation board.

Temp=25 ℃, frequency is 5.5 GHz unless otherwise specified.

Parameter		Symbol	Value	Unit	Remarks
Supply Voltage		V_{cc}	3	V	
Supply Current		I_{cc}	10	mA	
Noise Figure		NF [1]	1.3	dB	
Power Gain	5.0 GHz	G_P	15.8	dB	
	5.5 GHz		14.7	dB	
	6.0 GHz		13.7	dB	
Input return Loss		IRL	12	dB	
Output return Loss		ORL	13.5	dB	
Input 1 dB Gain compression Point		P_i1dB	-7.5	dBm	
Output 1 dB Gain compression Point		P_o1dB	+6.5	dBm	
Input third order intercept point		$IP3_i$	+10	dBm	
Output third order intercept point		$IP3_o$	+24	dBm	
Power settling time		Ton	160	μs	
		Toff	28	ns	

[1] The NF and Gain figures are being measured at the SMA connectors of the evaluation board, so the losses of the connectors and the PCB of approximately 0.1dB are not subtracted.

4.5.1 Faster switching time. <1 μs

If no switching speed is required in the application, the recommendation is to keep the BOM as is presented in this application not. However if the LNA is applied in e.g. a WLAN application where power settling time is required to be <1 μs, the value of C3 should be changed to 67pF. This will result in a Ton power settling time of 890ns and the Toff power settling time stays 28ns. However this change in capacitor values will result in about 5dB of degradation of the IP3 figures reported in Table 3

4.5.2 Gain and match – typical results

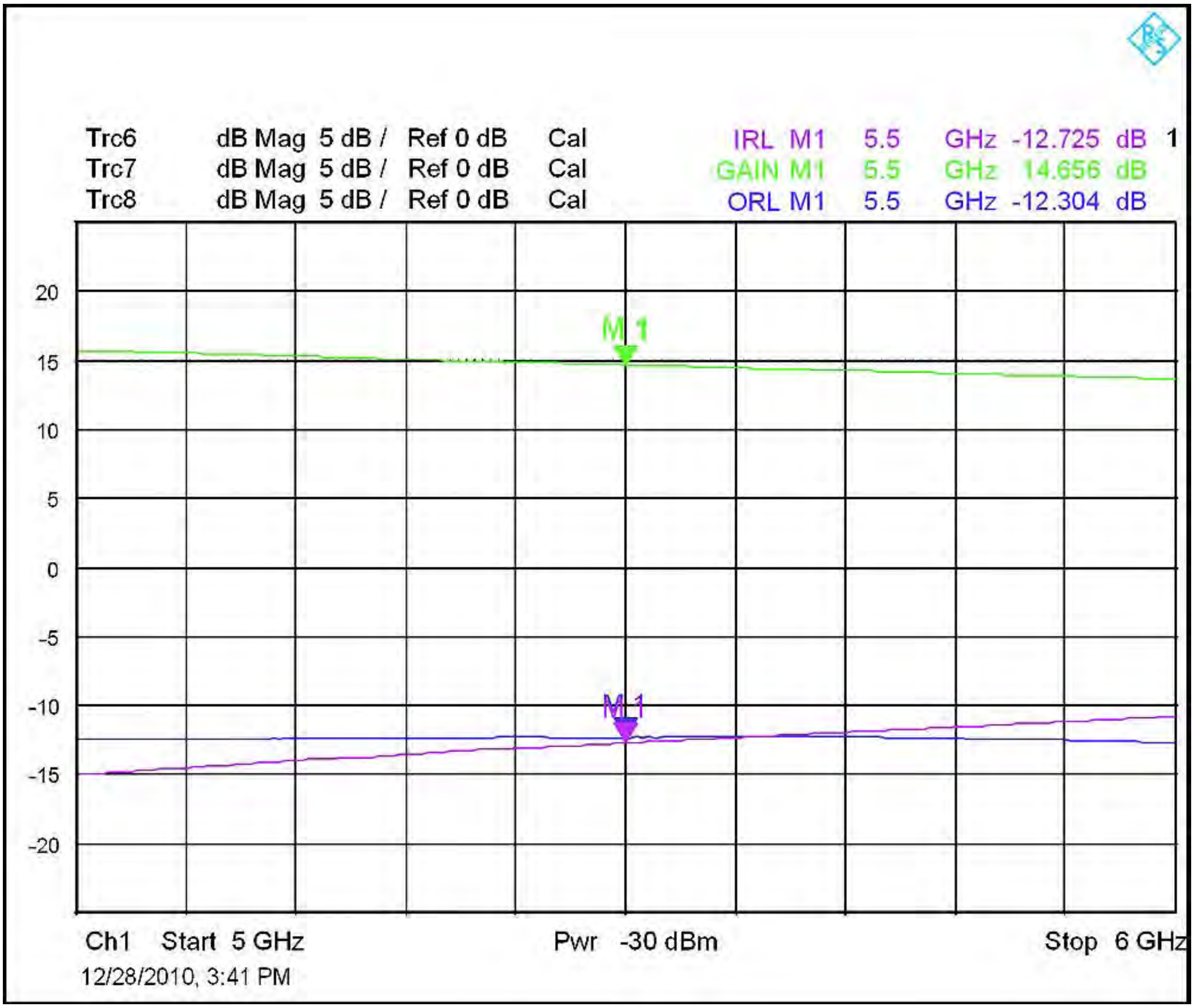


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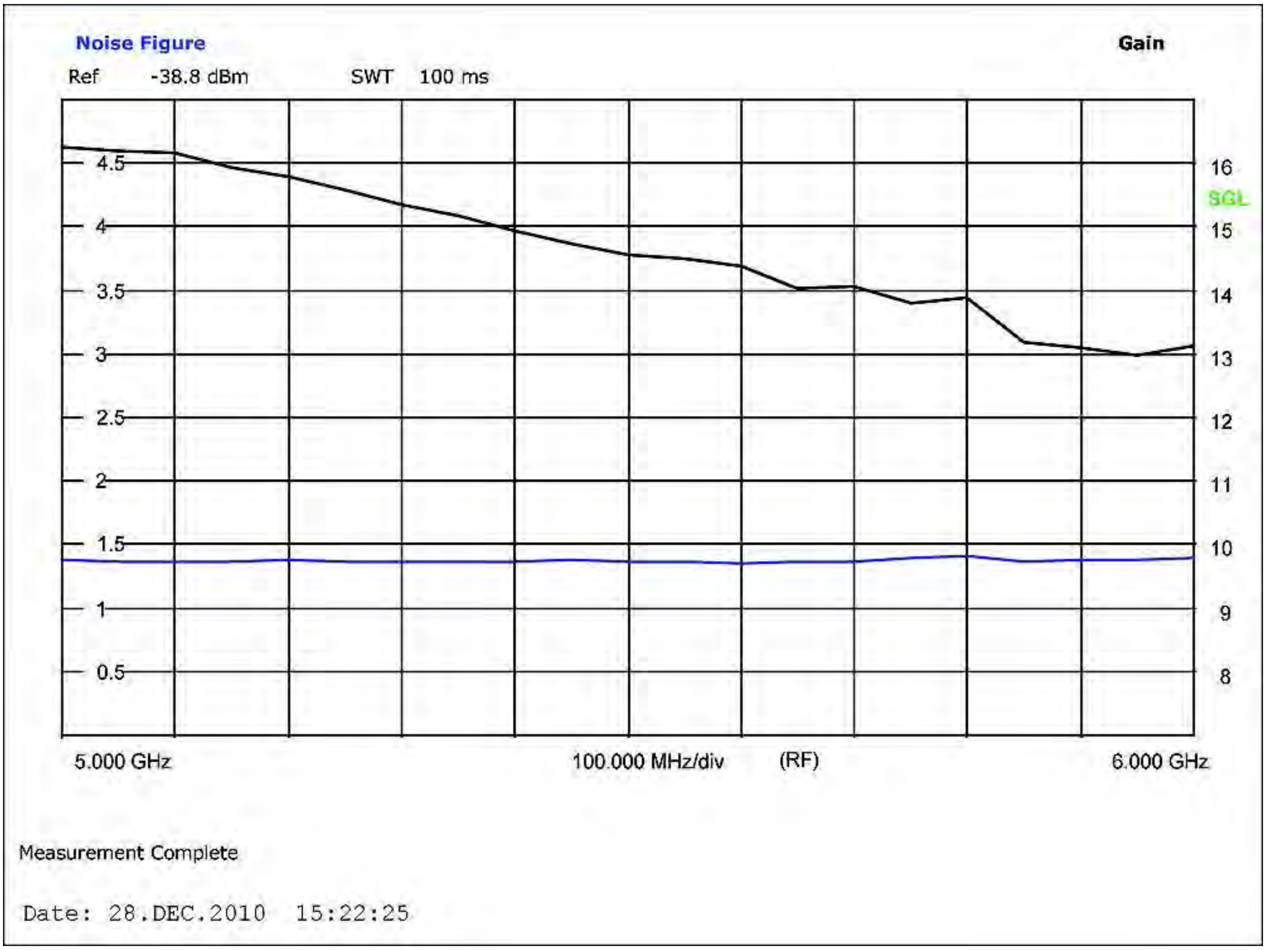
Fig 9. Gain and match measured values

4.5.3 NF and Gain- typical values



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(1) NF is measured at SMA connectors so no correction was done.

Fig 10. Typical NF curve

4.5.4 Stability

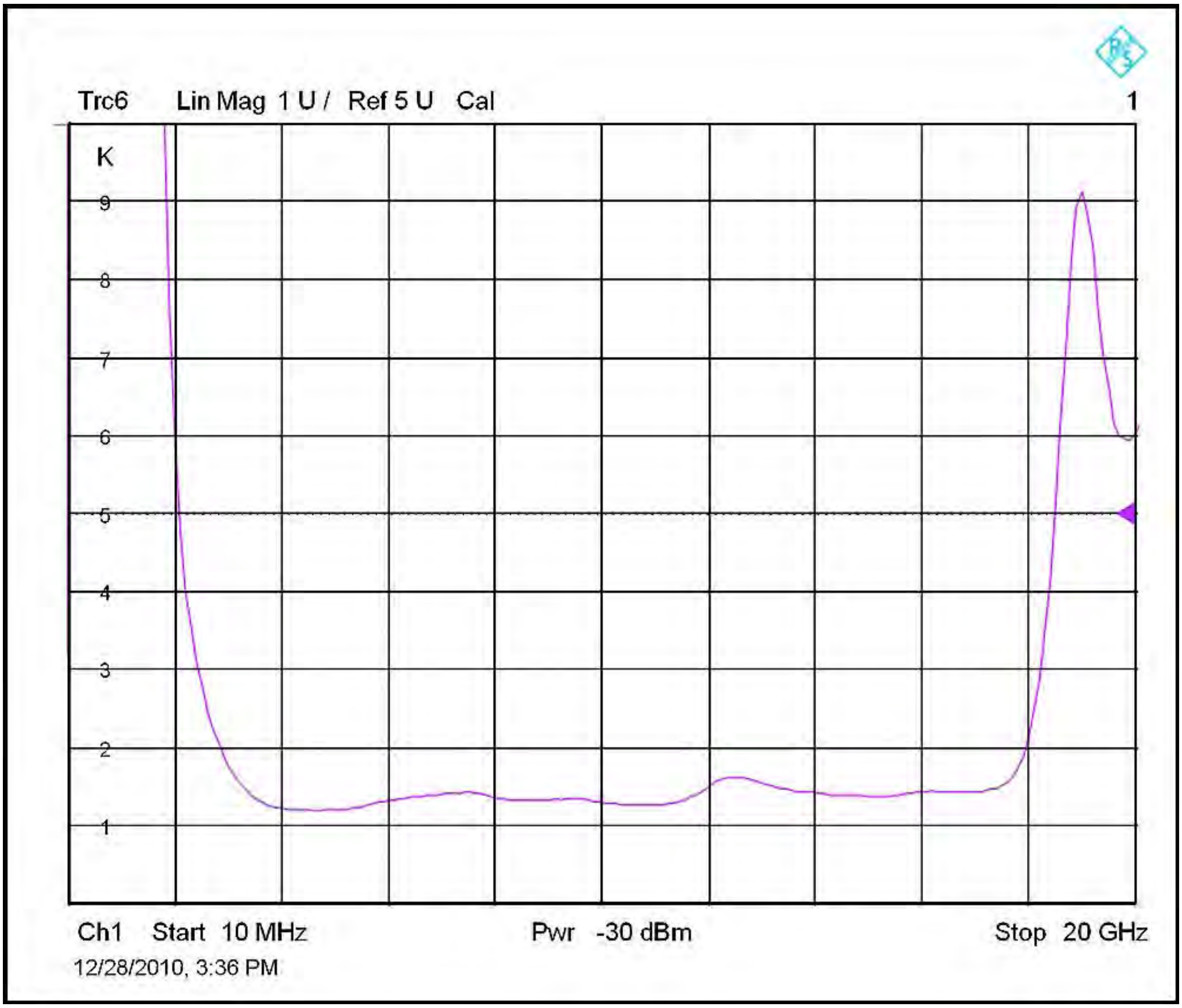

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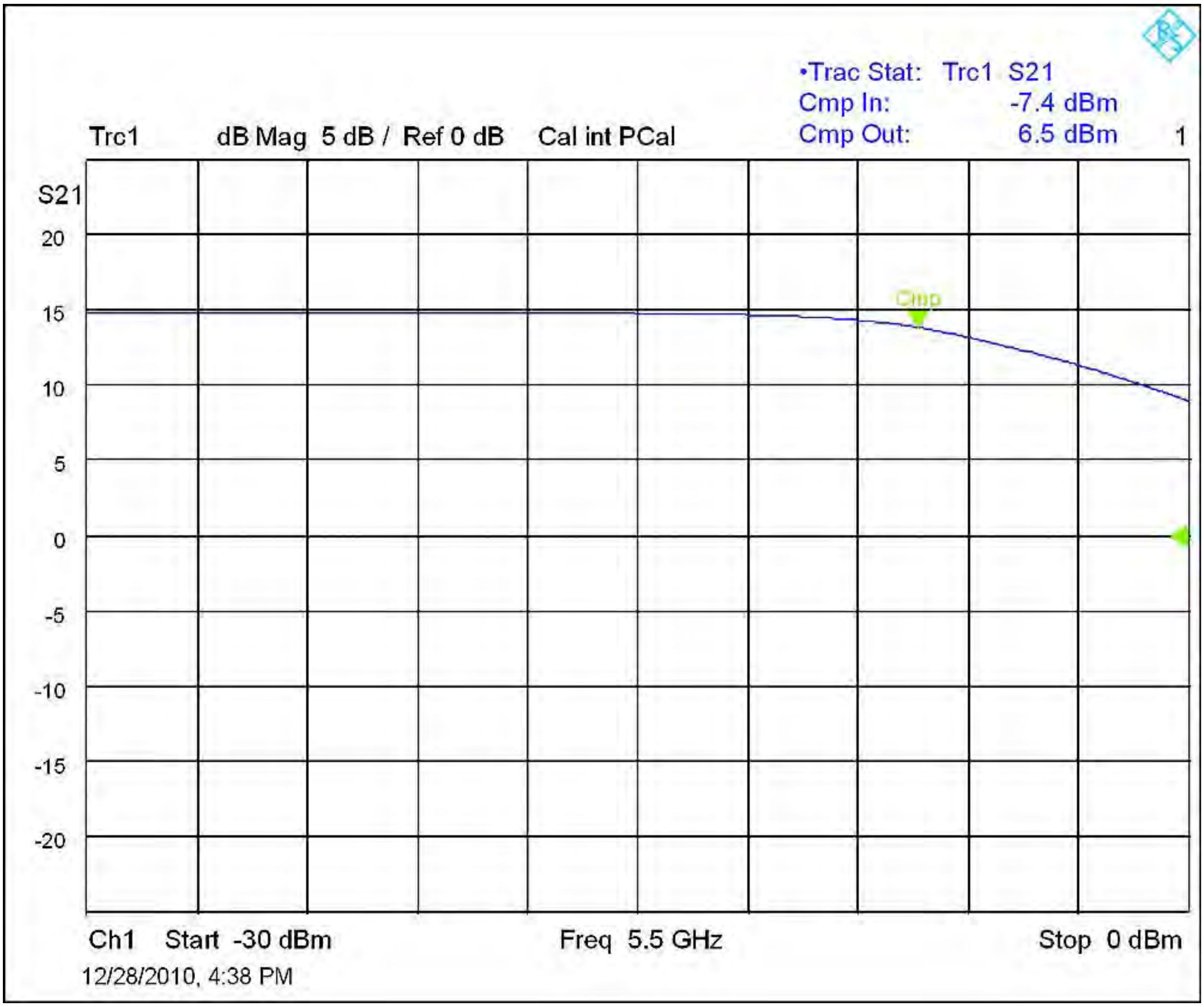
Fig 11. Stability typical measurement results

4.5.5 1dB compression point- typical values.



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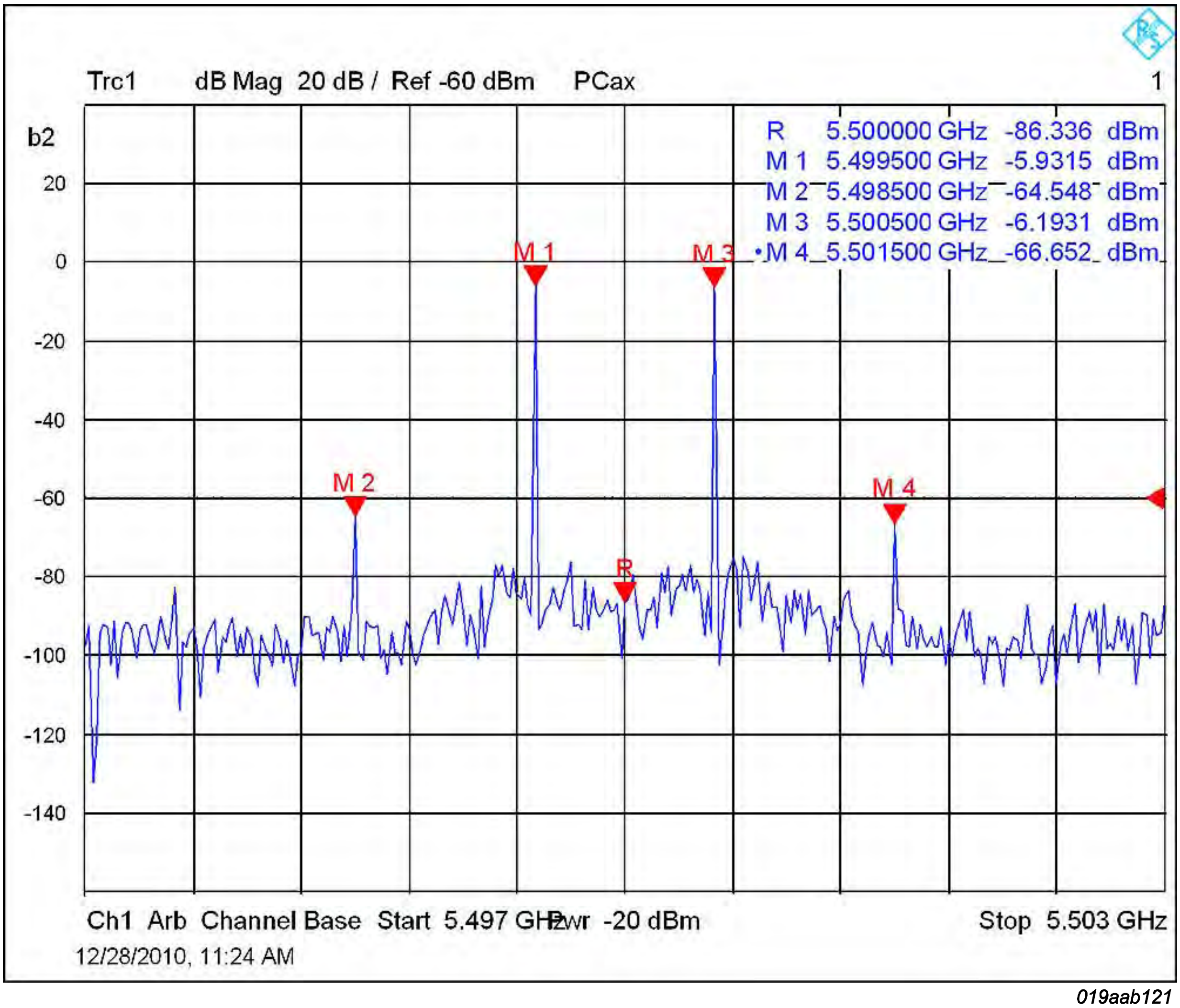
(1) P_i1dB=-7.4 dBm P_o1dB=6.5 dBm

Fig 12. Typical 1 dB compression point curve.

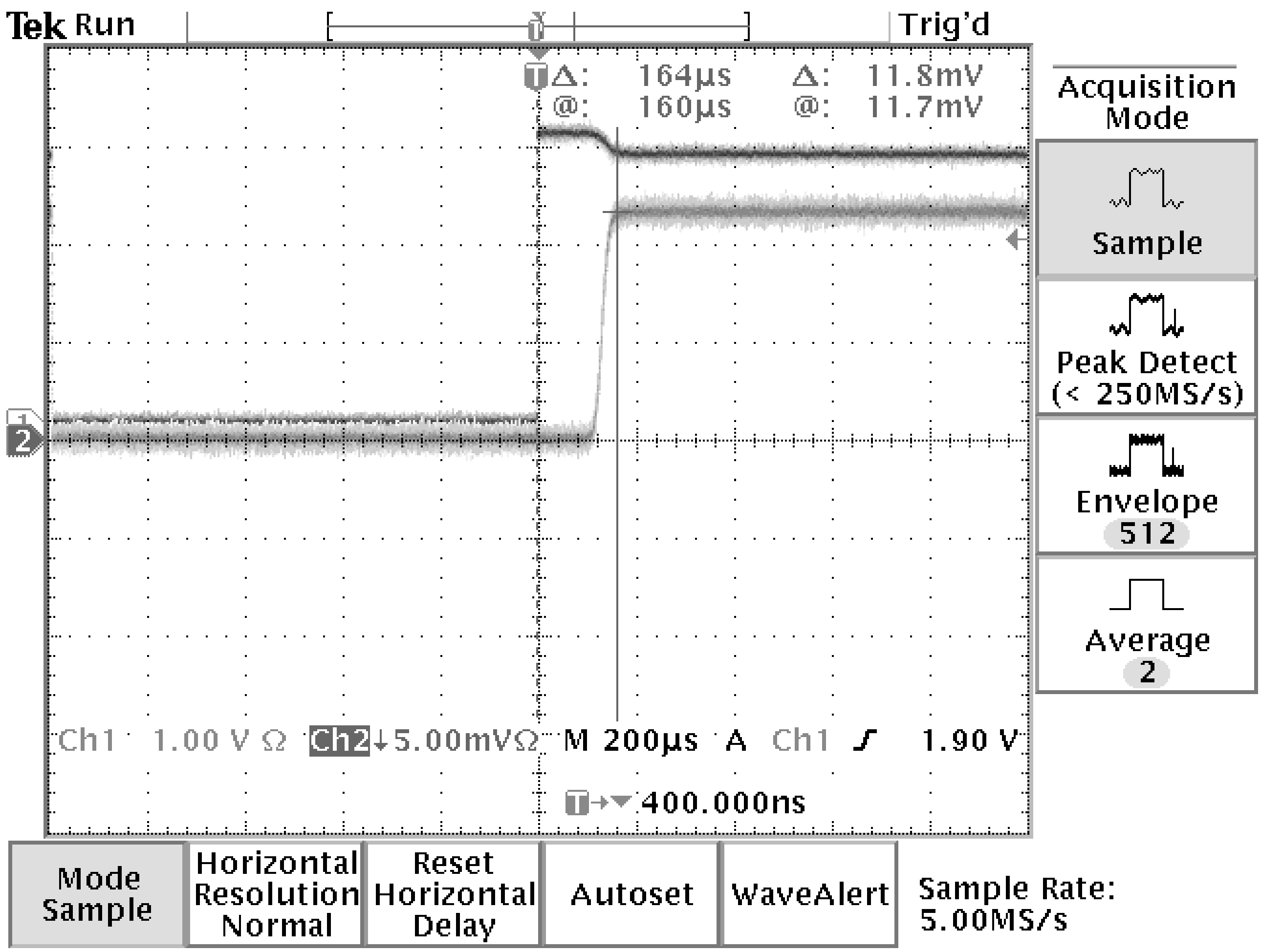
4.5.6 Linearity IP3 – typical values



(1) $IP3_o$=-6.2+((66.7-6.2)/2)=+24 dBm; $IP3_i$= -20 dBm+60.5/2=-20+30.25=+10.25

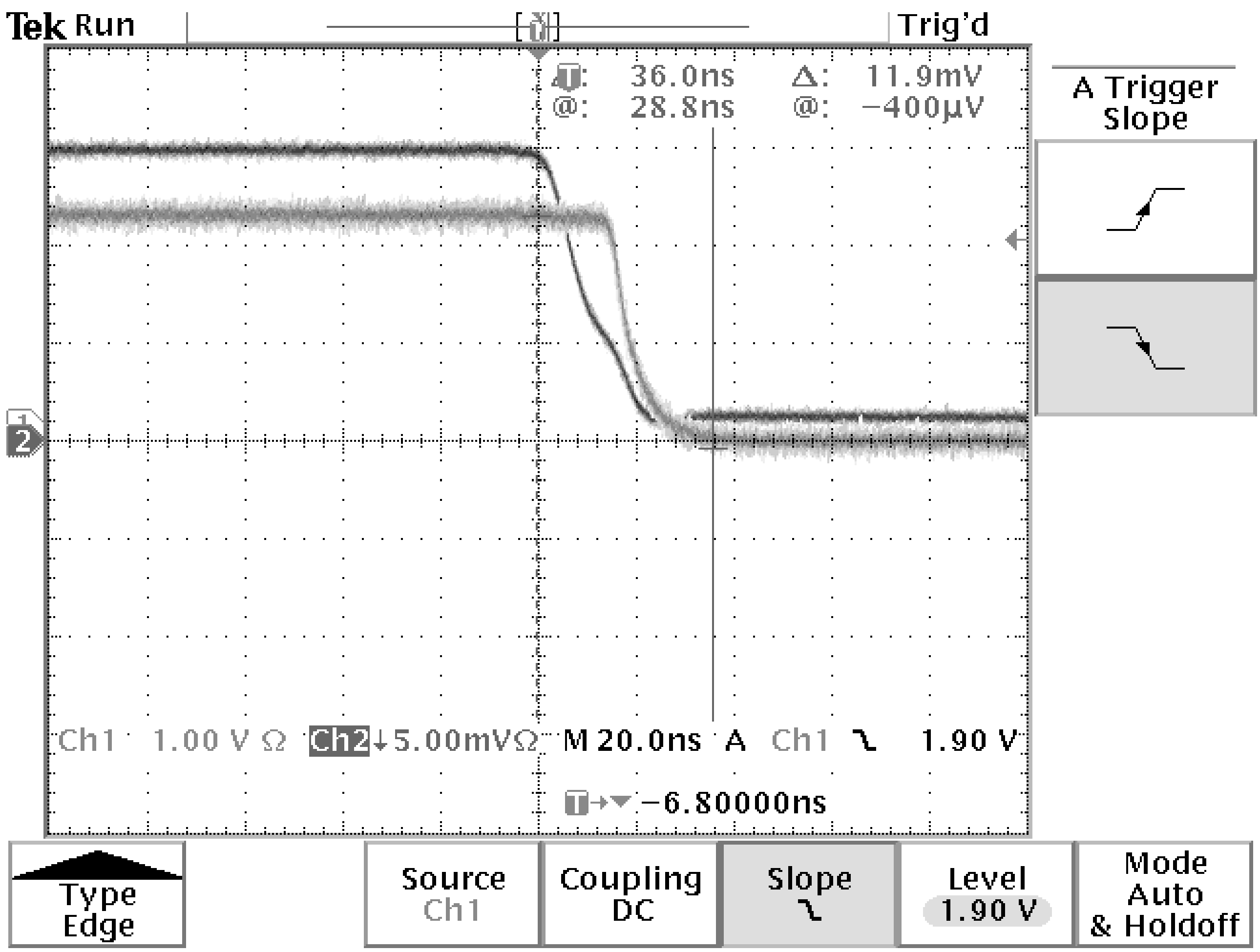
Fig 13. IM3 - typical values

4.5.7 Power settling time



(1) Curve1 is power supply; curve 2 is output of the detector diode.

Fig 14. t_{on} Power on settling time



(1) curve1 is power supply; curve 2 is de output of the detection diode.

Fig 15. t_{off} Power off settling time

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6. List of figures

7. List of tables

8. Contents

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