MCP19122/3

MCP19122/3 Flash Memory Programming Specification

This document includes the programming specifications for the following devices:

- MCP19122
- MCP19123

1.0 PROGRAMMING THE MCP19122/3 DEVICES

The MCP19122/3 devices are programmed using a serial method. The Serial mode will allow these devices to be programmed while in the user's system. These programming specifications apply to all of the above devices in all packages.

1.1 Hardware Requirements

This family of devices requires one power supply for V_{IN} (see Table 6-1). The V_{DD} that is used to bias all internal circuitry is internally generated and regulated to 5V. A 1 µF ceramic capacitor must be placed between the V_{DD} and P_{GND} pins.

1.2 Program/Verify Mode

The Program/Verify mode for this family of devices allows programming of user program memory, user ID locations, the Calibration Word and the Configuration Word.

FIGURE 1-1: PIN DIAGRAM – 24-PIN QFN (MCP19122)

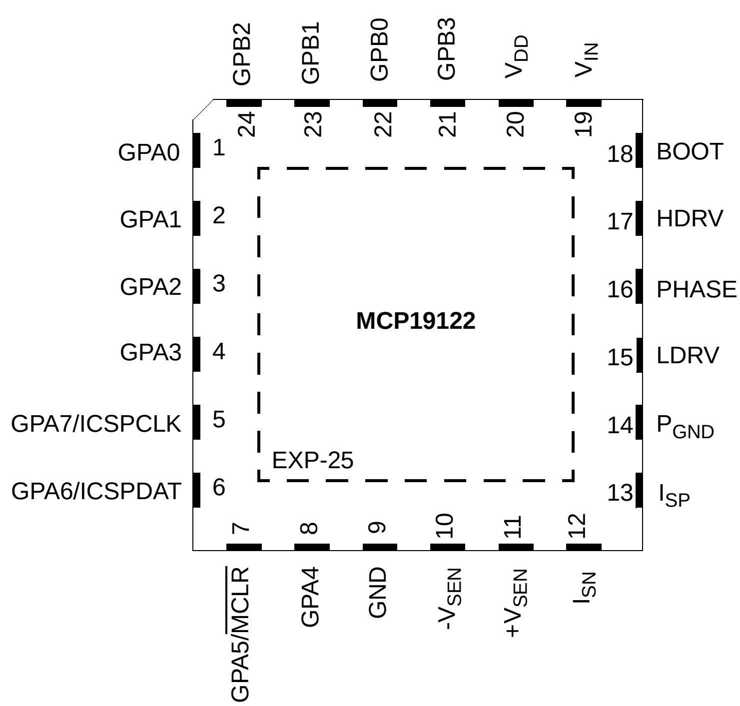


TABLE 1-1: PIN DESCRIPTIONS IN PROGRAM/VERIFY MODE: MCP19122

Pin Name	During Programming		
	Function	**Pin Type**	**Pin Description**
GPA7	ICSPCLK	I	Clock Input – Schmitt Trigger Input
GPA6	ICSPDAT	I/O	Data Input/Output – Schmitt Trigger Input
$\overline{MCLR}$	Program/Verify mode	P(1)	Program Mode Select
V_{IN}	V_{IN}	P	Device Power Supply Input
V_{DD}	V_{DD}	P	Power Supply Output
GND	V_{SS}	P	Ground

Legend: I = Input, O = Output, P = Power

Note 1: In the MCP19122, the programming high voltage is internally generated. To activate the Program/Verify mode, a voltage of V_{IHH} and a current of I_{IHH} (see Table 6-1) need to be applied to the $\overline{MCLR}$ input.

FIGURE 1-2: MCP19122 PROGRAMMING WIRING DIAGRAM

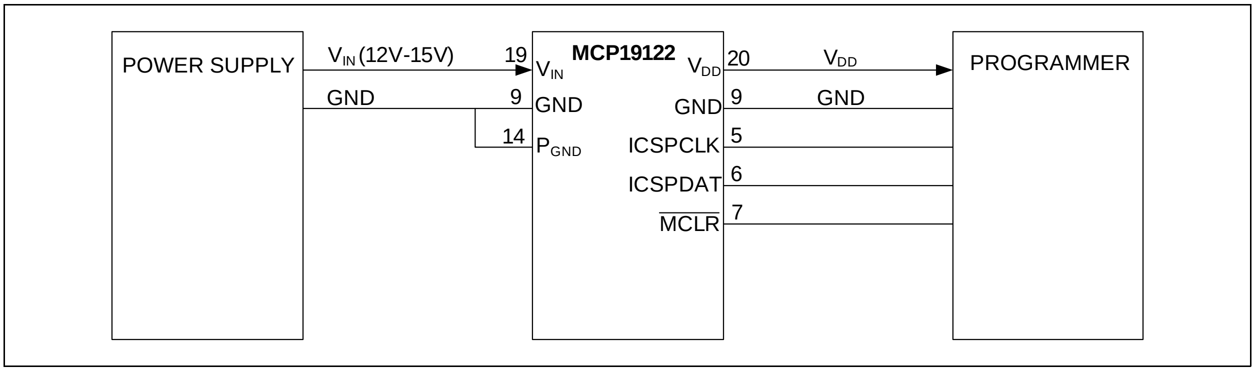


FIGURE 1-3: PIN DIAGRAM - 28-PIN QFN (MCP19123)

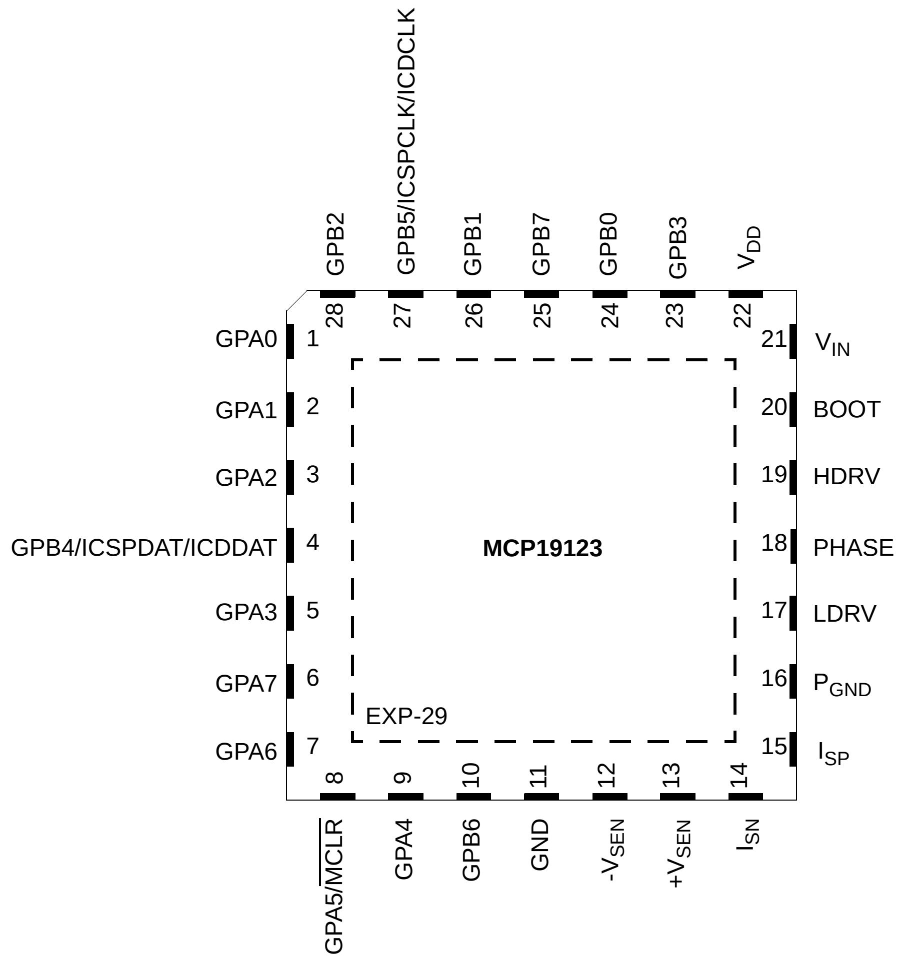


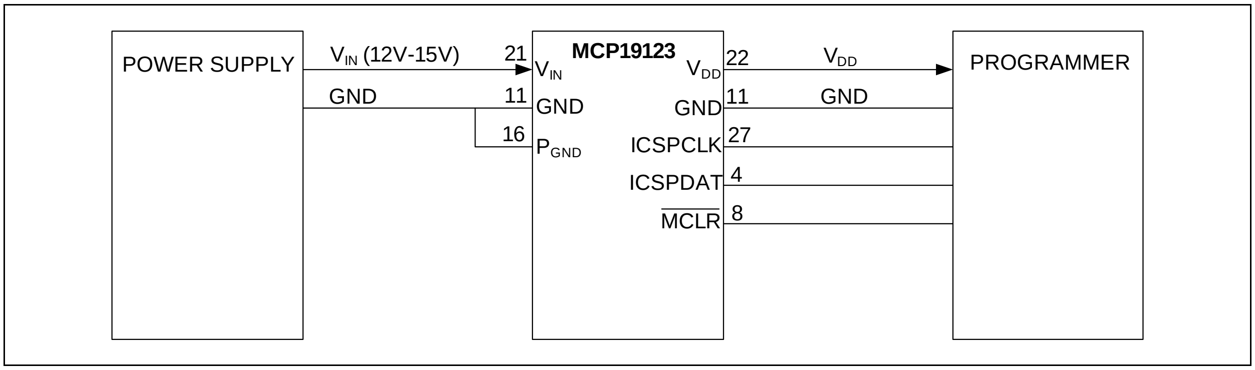
TABLE 1-2: PIN DESCRIPTIONS IN PROGRAM/VERIFY MODE: MCP19123

Pin Name	During Programming		
	Function	Pin Type	Pin Description
GPB5	ICSPCLK	I	Clock Input – Schmitt Trigger Input
GPB4	ICSPDAT	I/O	Data Input/Output – Schmitt Trigger Input
$\overline{MCLR}$	Program/Verify mode	P(1)	Program Mode Select
V_{IN}	V_{IN}	P	Device Power Supply Input
V_{DD}	V_{DD}	P	Power Supply Output
GND	V_{SS}	P	Ground

Legend: I = Input, O = Output, P = Power

Note 1: In the MCP19123, the programming high voltage is internally generated. To activate the Program/Verify mode, a voltage of V_{IHH} and a current of I_{IHH} (see Table 6-1) need to be applied to the $\overline{MCLR}$ input.

FIGURE 1-4: MCP19123 PROGRAMMING WIRING DIAGRAM



2.0 MEMORY DESCRIPTION

2.1 Program Memory Map

The user memory space extends from 0x0000 to 0x1FFF. In Program/Verify mode, the program memory space extends from 0x0000 to 0x3FFF, with the first half (0x0000-0x1FFF) being user program memory and the second half (0x2000-0x3FFF) being configuration memory. The Program Counter (PC) will increment from 0x0000 to 0x1FFF and wrap to 0x0000. If the PC is between 0x2000 to 0x3FFF, it will wrap-around to 0x2000 (not to 0x0000). Once in configuration memory, the highest bit of the PC stays a '1', thus always pointing to the configuration memory. The only way to point to user program memory is to reset the part and re-enter Program/Verify mode as described in **Section 3.0 "Program/Verify Mode"**.

For all of the devices covered in this document, the configuration memory space, 0x2000 to 0x208F, is physically implemented. However, only locations 0x2000 to 0x2003, 0x2007, and 0x2080 to 0x208F are available. Other locations are reserved.

2.2 User ID Locations

A user may store identification information (user ID) in four designated locations. The user ID locations are mapped in 0x2000 to 0x2003. It is recommended that the user use only the seven Least Significant bits (LSbs) of each user ID location. The user ID locations read out normally, even after code protection is enabled. It is recommended that ID locations are written as 'xx xxxx xbbb bbbb', where 'bbb bbbb' is the user ID information.

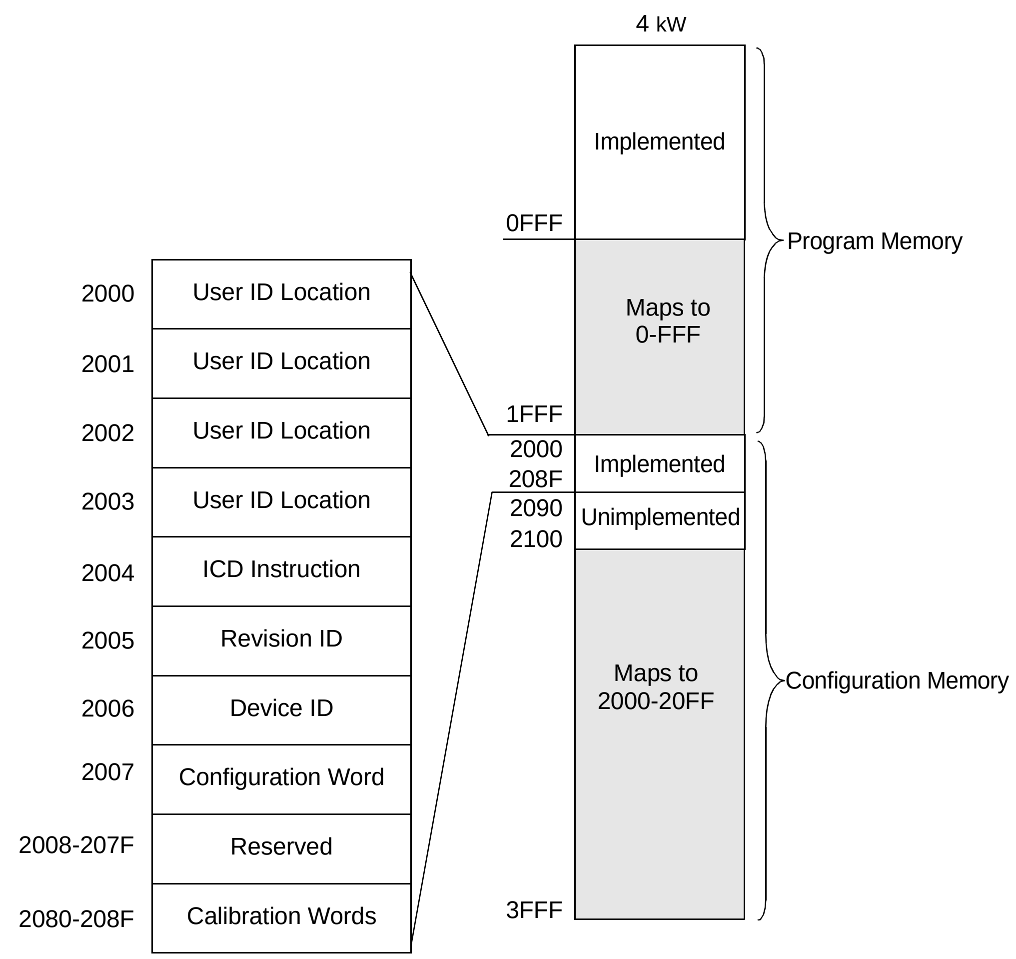
The 14 bits may be programmed, but only the seven LSbs are read and displayed by the MPLAB® Integrated Development Environment (IDE).

2.3 Calibration Word

For all of the devices covered in this document, Calibration Words are included to allow storing the trim values for various analog peripherals (e.g., INTOSC module) at final test. These values are stored in the Calibration Words 0x2080 to 0x208F. See the applicable device data sheet for more information.

The Calibration Words do not necessarily participate in the erase operation, unless a specific procedure is executed. Therefore, the device can be erased without affecting the Calibration Words. This simplifies the erase procedure, since these values do not need to be read and restored after the device is erased.

FIGURE 2-1: MCP19122/3 PROGRAM MEMORY MAPPING



3.0 PROGRAM/VERIFY MODE

Two methods are available to enter the Program/Verify mode. "V_{PP}-first" is entered by holding ICSPDAT and ICSPCLK low while raising the $\overline{MCLR}$ pin from V_{IL} to V_{IHH} (high voltage), then applying V_{DD} and data. This method can be used for any Configuration Word selection and **must** be used if the internal $\overline{MCLR}$ option is selected (MCLRE = 0). The TEST_EN-first entry prevents the device from executing code prior to entering the Program/Verify mode. See the timing diagram in Figure 3-1.

The second entry method, "V_{DD}-first", is entered by applying V_{DD}, holding ICSPDAT and ICSPCLK low, then raising the $\overline{MCLR}$ pin from V_{IL} to V_{IHH} (high voltage), followed by data. This method can be used for any Configuration Word selection, **except** when the internal $\overline{MCLR}$ option is selected (MCLRE = 0). This programming technique is also useful when programming the device with V_{DD} already applied, for it is not necessary to disconnect the V_{DD} to enter the Program/Verify mode. See the timing diagram in Figure 3-2.

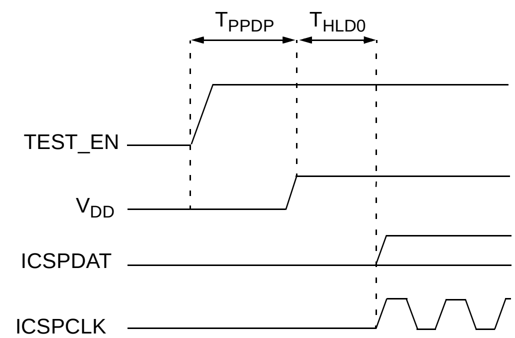
Once in Program/Verify mode, the program memory and configuration memory can be accessed and programmed in a serial fashion. ICSPDAT and ICSPCLK are Schmitt Trigger inputs in this mode.

The sequence that enters the device into the Program/Verify mode places all other logic into the Reset state (the $\overline{MCLR}$ pin was initially at V_{IL}). Therefore, all I/Os are in the Reset state (high-impedance inputs) and the PC is cleared.

To prevent a device configured with internal $\overline{MCLR}$ from executing after exiting Program/Verify mode, the V_{DD} needs to power-down before TEST_EN. See Figure 3-3 for the timing diagram.

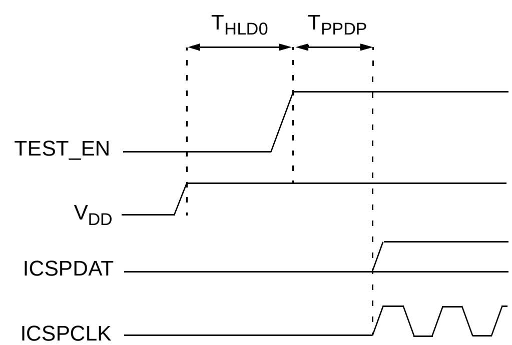
The MCP19122/3's V_{DD} is internally generated by applying voltage to the V_{IN} pin. See Table 6-1 for the appropriate range for V_{IN}. To remove V_{DD}, V_{IN} must be removed.

FIGURE 3-1: TEST_EN-FIRST PROGRAM/ VERIFY MODE ENTRY



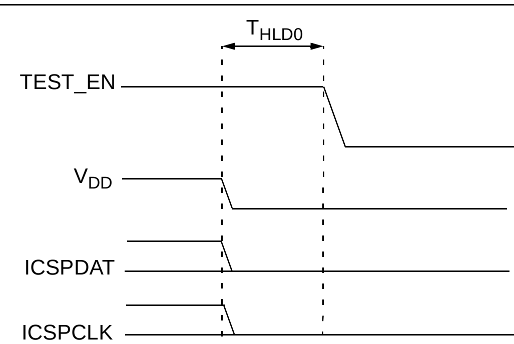
Note: This method of entry is valid, regardless of the Configuration Word selected.

FIGURE 3-2: V_{DD}-FIRST PROGRAM/ VERIFY MODE ENTRY



Note: This method of entry is valid if the internal $\overline{MCLR}$ is not selected.

FIGURE 3-3: PROGRAM/VERIFY MODE EXIT



3.1 Program/Erase Algorithms

The MCP19122/3 program memory may be written in two ways. The fastest method writes four words at a time. However, one-word writes are also supported. The four-word algorithm is used to program the program memory only. The one-word algorithm can write any available memory location (e.g., program memory, configuration memory and calibration memory).

After writing the array, the PC may be reset and read back to verify the write. It is not possible to verify immediately following the write because the PC can only increment, not decrement.

A device Reset will clear the PC and set the address to '0'. The `Increment Address` command will increment the PC. The `Load Configuration` command will set the PC to 0x2000. The available commands are shown in Table 3-1.

3.1.1 FOUR-WORD PROGRAMMING

The MCP19122/3 program memory can be written four words at a time using the four-word algorithm. Configuration memory (addresses > 0x2000) and non-aligned (Addresses Modulo 4 not equal to zero) starting addresses must use the one-word programming algorithm.

This algorithm writes four sequential addresses in program memory. The four addresses must point to a four-word block with an Address Modulo 4 of 0, 1, 2 and 3. For example, programming Addresses 4-7 can be programmed together. Programming Addresses 2-5 will create an unexpected result.

The sequence for programming four words of program memory at a time is:

1. Load a word at the current program memory address using the `Load Data For Program Memory` command. This location must be Address Modulo 4 equal to 0.
2. Issue an `Increment Address` command to point to the next address in the block.
3. Load a word at the current program memory address using the `Load Data For Program Memory` command.
4. Issue an `Increment Address` command to point to the next address in the block.
5. Load a word at the current program memory address using the `Load Data For Programming Memory` command.
6. Issue and `Increment Address` command to point to the next address in the book.
7. Load a word at the current program memory address using the `Load Data For Programming Memory` command.
8. Issue a `Begin Programming` command externally timed.
9. Wait $T_{PROG}1$.
10. Issue `End Programming`.
11. Wait T_{DIS}.
12. Issue an `Increment Address` command to point to the start of the next block of addresses.
13. Repeat steps 1 through 12 as required to write the desired range of program memory.

See Table 3-12 for more information.

3.1.2 ERASE ALGORITHMS

The MCP19122/3 devices will erase different memory locations depending on the PC and $\overline{CP}$. The following sequences can be used to erase noted memory locations. To erase the program memory and Configuration Word (0x2007), the following sequence must be performed. Note the Calibration Words (0x2080 to 0x208F) and user ID (0x2000-0x2003) **will not** be erased.

1. Do a `Bulk Erase Program Memory` command.
2. Wait T_{ERA} to complete erase.

To erase the user ID (0x2000-0x2003), Configuration Word (0x2007) and program memory, use the following sequence. Note that the Calibration Words (0x2080 to 0x208F) **will not** be erased.

1. Perform `Load Configuration` with dummy data to point the PC to 0x2000.
2. Perform a `Bulk Erase Program Memory` command.
3. Wait T_{ERA} to complete erase.

3.1.3 SERIAL PROGRAM/VERIFY OPERATION

The ICSPCLK pin is used as a clock input, and the ICSPDAT pin is used for entering command bits and data input/output during serial operation. To input a command, ICSPCLK is cycled six times. Each command bit is latched on the falling edge of the clock with the LSb of the command being input first. The data input onto the ICSPDAT pin is required to have a minimum setup and hold time (see Table 6-1), with respect to the falling edge of the clock. Commands that have data associated with them (Read and Load) are specified to have a minimum delay of 1 µs between the command and the data. After this delay, the clock pin is cycled 16 times with the first cycle being a Start bit and the last cycle being a Stop bit.

During a read operation, the LSb will be transmitted onto the ICSPDAT pin on the rising edge of the second cycle. For a load operation, the LSb will be latched on the falling edge of the second cycle. A minimum 1 µs delay is also specified between consecutive commands, except for the `End Programming` command, which requires a 100 µs (T_{DIS}).

All commands and data words are transmitted LSb first. Data is transmitted on the rising edge and latched on the falling edge of the ICSPCLK. To allow for decoding of commands and reversal of data pin configuration, a time separation of at least 1 µs ($T_{DLY}1$) is required between a command and a data word.

The commands that are available are described in Table 3-1.

TABLE 3-1: COMMAND MAPPING FOR MCP19122/3

Command	Mapping (MSb … LSb)						Data
Load Configuration	x	x	0	0	0	0	0, data (14), 0
Load Data For Program Memory	x	x	0	0	1	0	0, data (14), 0
Read Data From Program Memory	x	x	0	1	0	0	0, data (14), 0
Increment Address	x	x	0	1	1	0	
Begin Programming	x	1	1	0	0	0	Externally Timed
End Programming	x	0	1	0	1	0	
Bulk Erase Program Memory	x	x	1	0	0	1	Internally Timed
Row Erase Program Memory	x	1	0	0	0	1	Internally Timed

3.1.3.1 Load Configuration

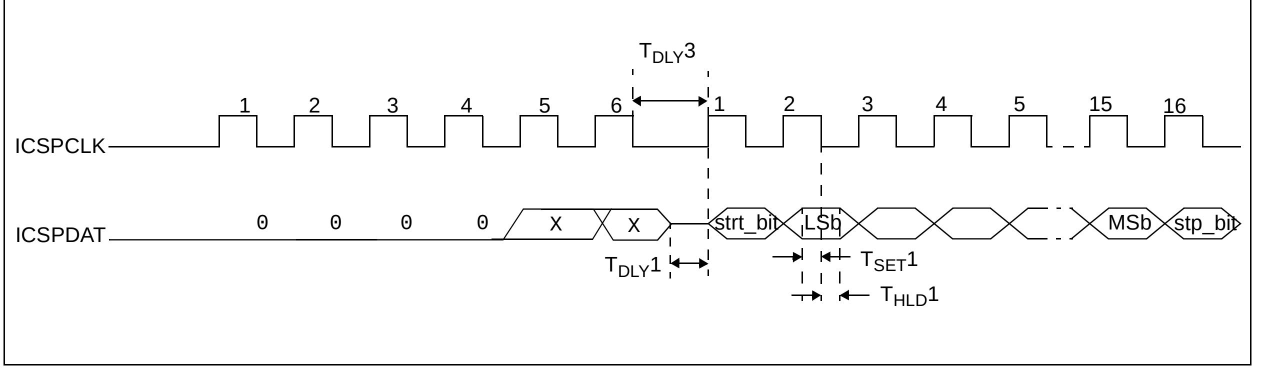
The Load Configuration command is used to access the Configuration Word (0x2007), user ID (0x2000-0x2003) and Calibration Words (0x2080 to 0x208F). This command sets the PC to address 0x2000 and loads the data latches with one word of data.

To access the configuration memory, send the Load Configuration command. Individual words within the configuration memory can be accessed by sending Increment Address commands and using Load or Read Data from Program Memory.

After the 6-bit command is input, the ICSPCLK pin is cycled an additional 16 times for the Start bit, 14 bits of data and the Stop bit (see Figure 3-4).

After the configuration memory is entered, the only way to get back to the program memory is to exit the Program/Verify mode by taking $\overline{MCLR}$ low (V_{IL}).

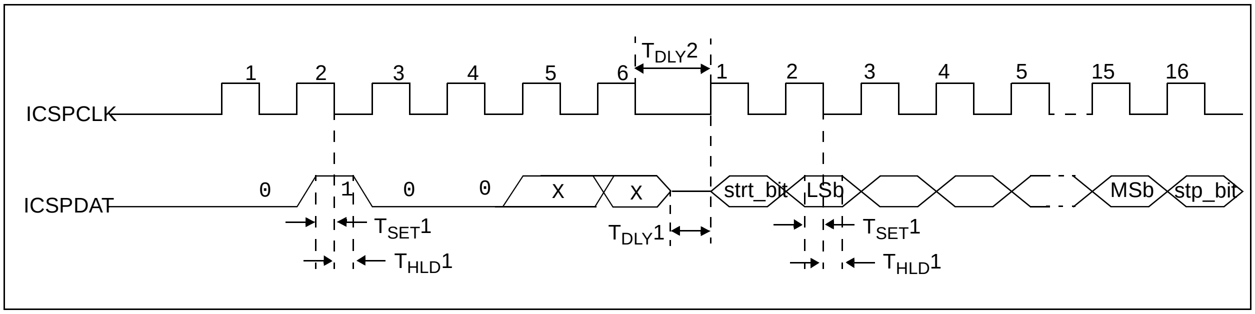
FIGURE 3-4: LOAD CONFIGURATION COMMAND



3.1.3.2 Load Data For Program Memory

After receiving this command, the chip will load in a 14-bit "data word" when 16 cycles are applied, as described in **Section 3.1.3.1 "Load Configuration"**. A timing diagram of this command is shown in Figure 3-5.

FIGURE 3-5: LOAD DATA FOR PROGRAM MEMORY COMMAND



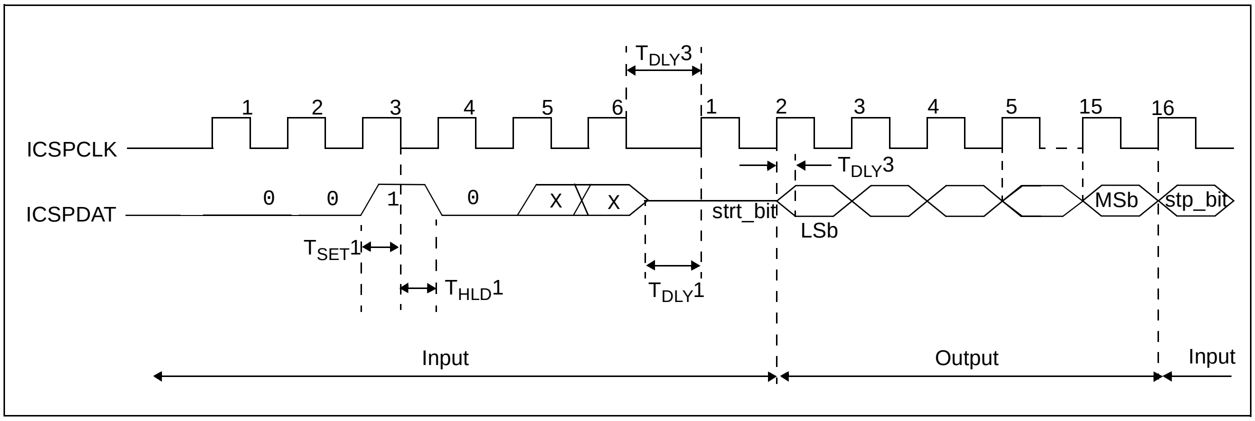
3.1.3.3 Read Data From Program Memory

After receiving this command, the chip will transmit data bits out of the program memory (user or configuration) currently accessed, starting with the second rising edge of the clock input. The data pin will go into Output mode on the second rising clock edge, and it will revert to Input mode (high-impedance) after the 16th rising edge.

If the program memory is code-protected ($\overline{CP}$ = 0), the data is read as zeros.

A timing diagram of this command is shown in Figure 3-6.

FIGURE 3-6: READ DATA FROM PROGRAM MEMORY COMMAND

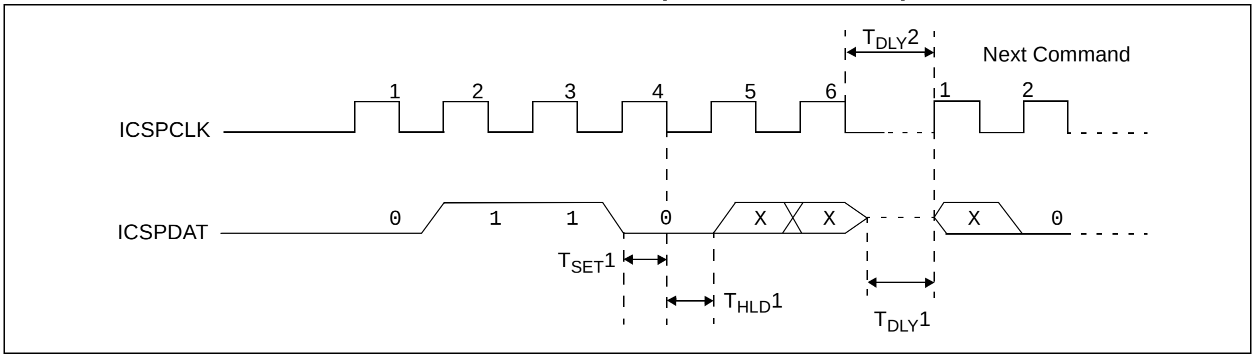


3.1.3.4 Increment Address

The PC is incremented when this command is received. A timing diagram of this command is shown in Figure 3-7. Incrementing past 0x07FF in the program memory rolls the program counter to '0'. Incrementing past 203Fh in test memory returns the Program Counter to 2000h.

It is not possible to decrement the address counter. To reset this counter, the user should exit and re-enter Program/Verify mode.

FIGURE 3-7: INCREMENT ADDRESS COMMAND (PROGRAM/VERIFY)

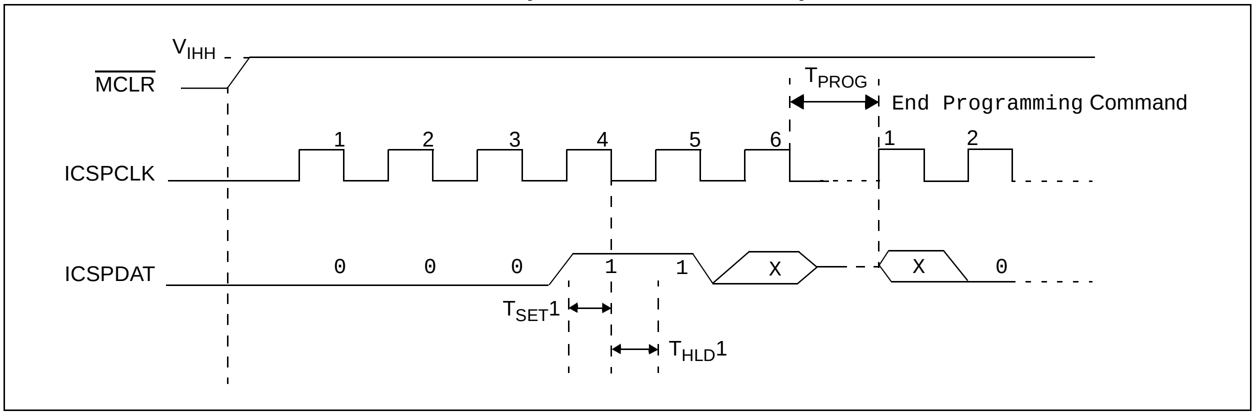


3.1.3.5 Begin Programming (Externally Timed)

A Load command must be given before every Begin Programming command. Programming of the appropriate memory (program memory, configuration or calibration memory) will begin after this command is received and decoded. Programming requires (T_{PROG}) time and is terminated using an End Programming command. A timing diagram for this command is shown in Figure 3-8.

The addressed locations are not erased before programming.

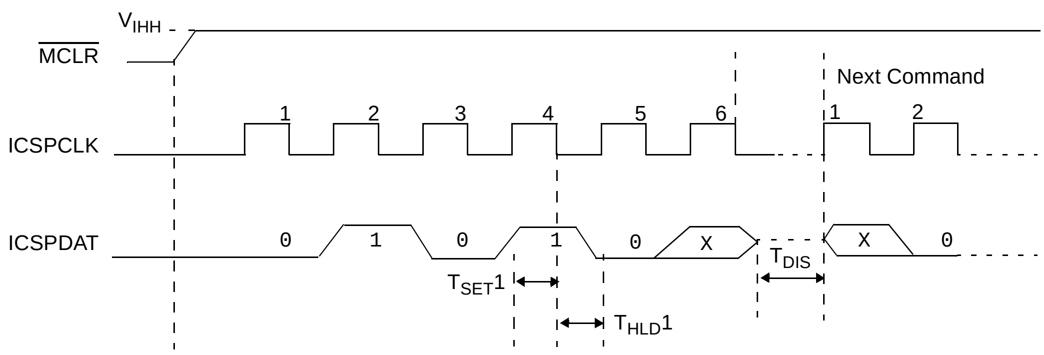
FIGURE 3-8: BEGIN PROGRAMMING (EXTERNALLY TIMED)



3.1.3.6 End Programming

After this command is performed, the write procedure will stop. A timing diagram of this command is shown in Figure 3-9.

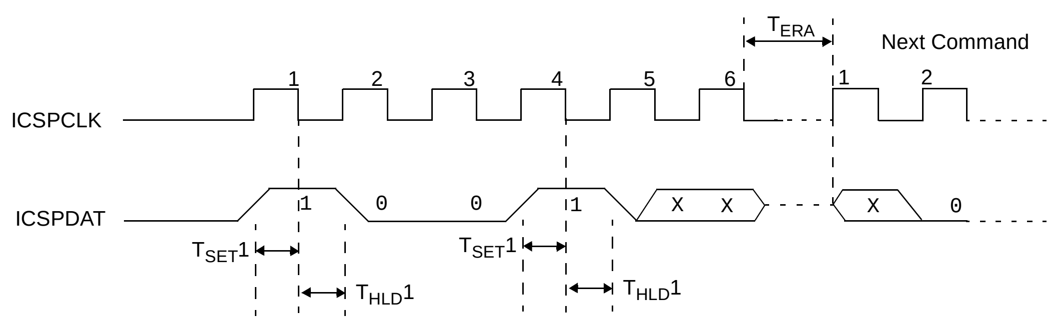
FIGURE 3-9: END PROGRAMMING (SERIAL PROGRAM/VERIFY)



3.1.3.7 Bulk Erase Program Memory

After this command is performed, the entire program memory and the Configuration Word (0x2007) are erased. The user ID and calibration memory may also be erased, depending on the value of the PC. See **Section 3.1.2 "Erase Algorithms"** for erase sequences. A timing diagram for this command is shown in Figure 3-10.

FIGURE 3-10: BULK ERASE PROGRAM MEMORY COMMAND



3.1.3.8 Row Erase Program Memory

This command erases the 16-word row of program memory pointed to by PC<11:4>. If the program memory array is protected ($\overline{CP}$ = 0), the command is ignored.

To perform a Row Erase Program Memory, the following sequence must be performed:

1. Execute a Row Erase Program Memory command.
2. Wait T_{ERA} to complete a row erase.

FIGURE 3-11: ROW ERASE PROGRAM MEMORY COMMAND

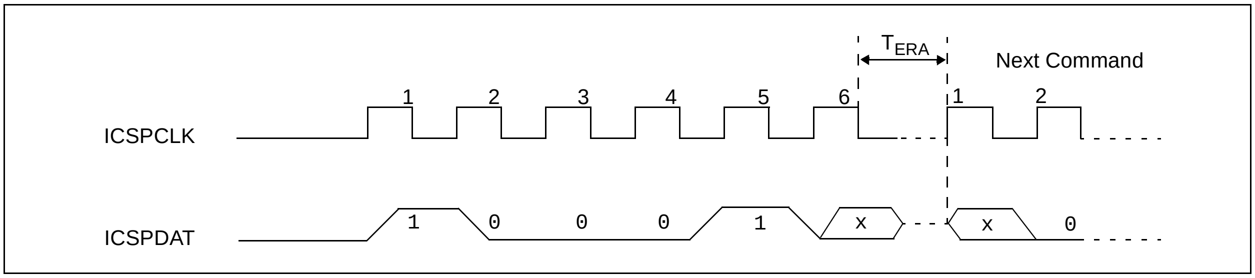
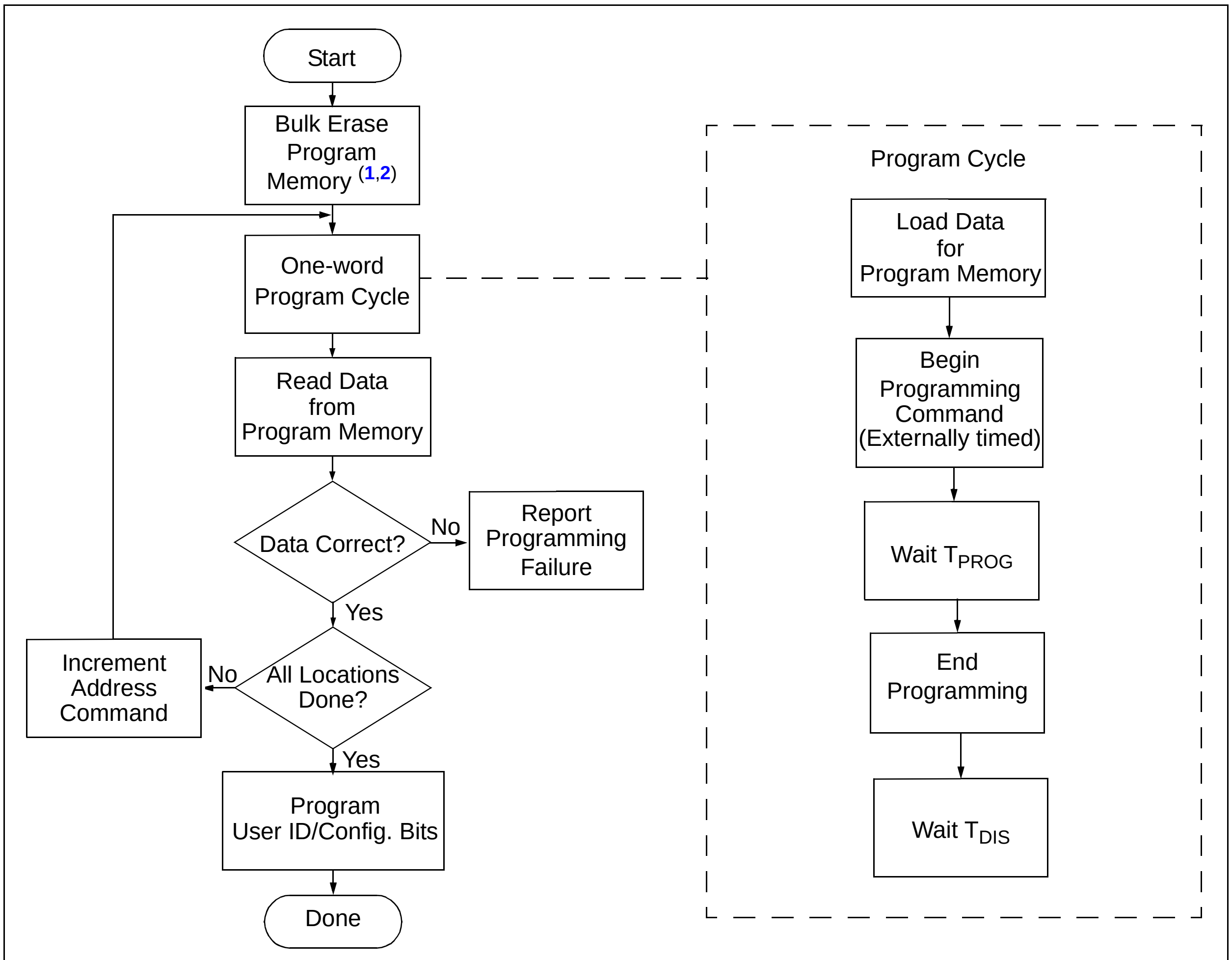


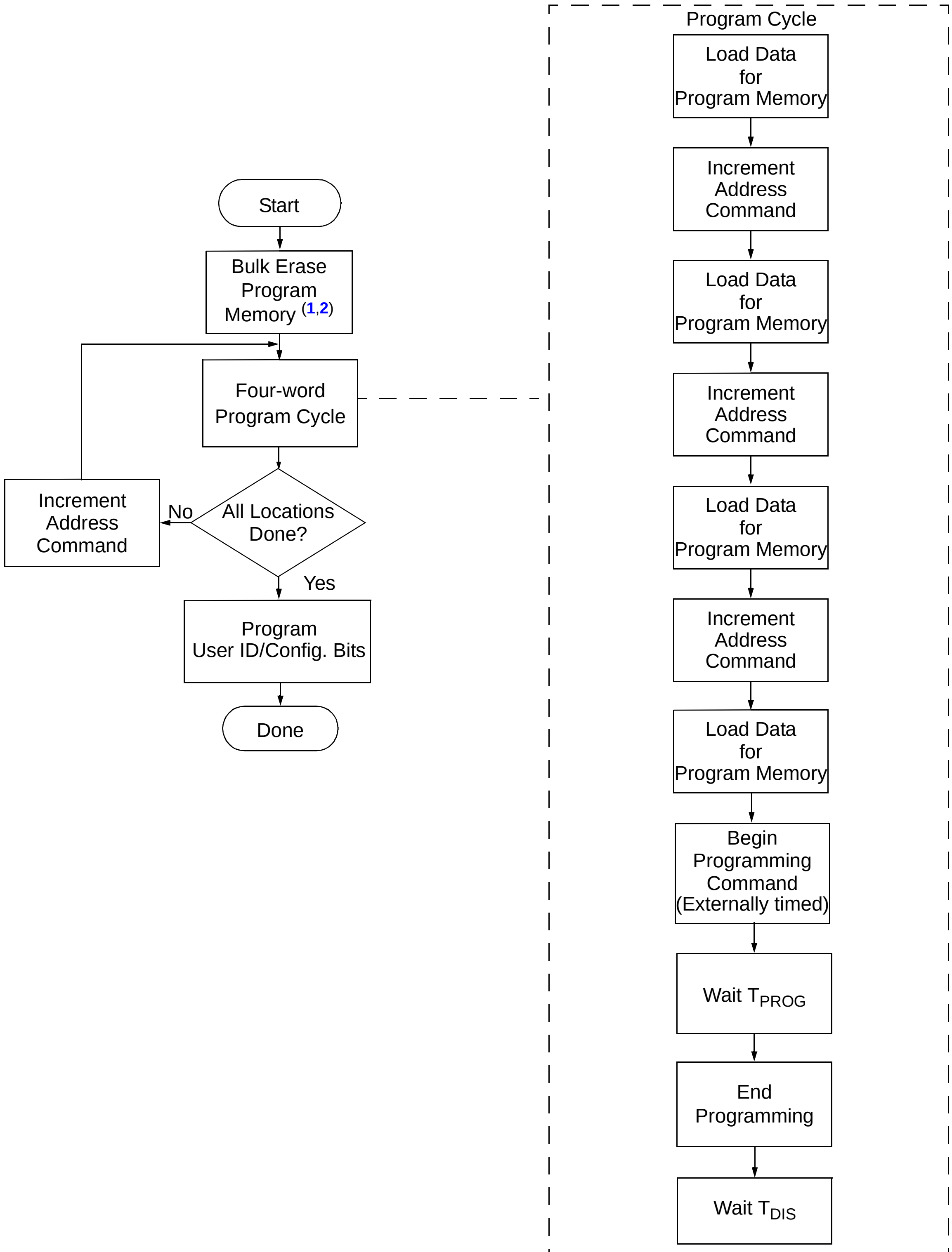
FIGURE 3-12: ONE-WORD PROGRAMMING FLOWCHART



Note 1: This step is optional if the device has already been erased or has not been previously programmed.

2: If the device is code-protected or must be completely erased, then bulk erase the device per Figure 3-15.

FIGURE 3-13: FOUR-WORD PROGRAMMING FLOWCHART



Note 1: This step is optional if the device is erased or not previously programmed.

2: If the device is code-protected or must be completely erased, then bulk erase the device per Figure 3-15.

FIGURE 3-14: PROGRAM FLOWCHART – CONFIGURATION MEMORY

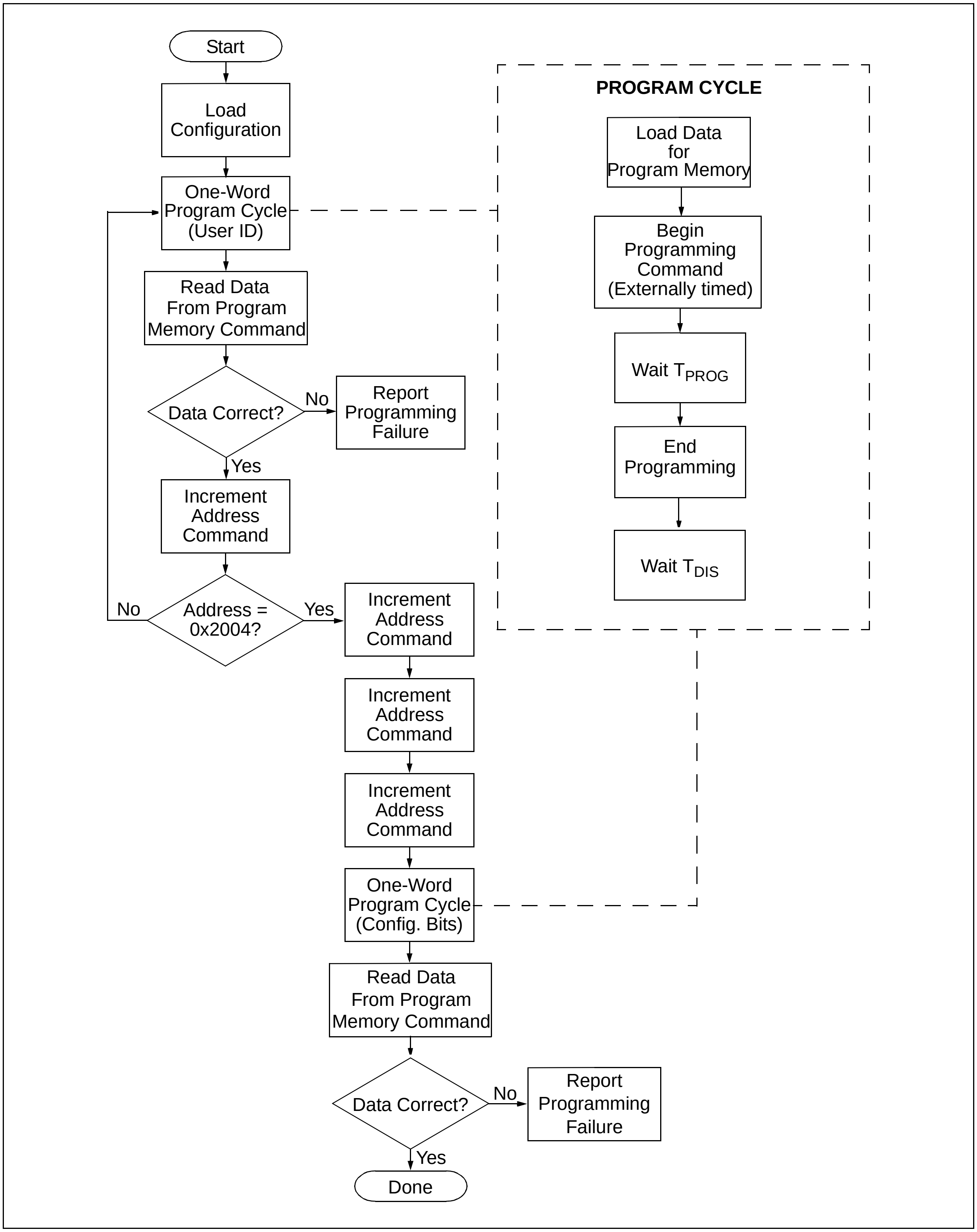
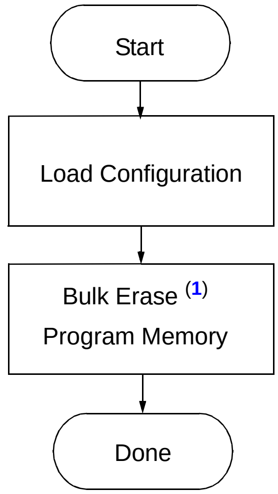


FIGURE 3-15: PROGRAM FLOWCHART – ERASE FLASH DEVICE



Note 1: See **Section 3.1.3.7 "Bulk Erase Program Memory"** for more information on the bulk erase procedure.

4.0 CONFIGURATION WORD

The MCP19122/3 devices have several Configuration bits. These bits can be programmed (read '0') or left unchanged (read '1'), to select various device configurations.

REGISTER 4-1: CONFIG: CONFIGURATION WORD (ADDRESS: 2007h)

R/P-1	U-1	R/P-1	R/P-1	U-1	R/P-1
$\overline{\text{DBGEN}}$	—	WRT1	WRT0	—	BOREN
bit 13					bit 8

U-0	R/P-1	R/P-1	R/P-1	R/P-1	U-1	U-1	U-1
—	$\overline{\text{CP}}$	$\overline{\text{MCLRE}}$	$\overline{\text{PWRTE}}$	WDTE	—	—	—
bit 7							bit 0

Legend:			
R = Readable bit	P = Programmable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 13 **$\overline{\text{DBGEN}}$:** ICD Debug bit
1 = ICD Debug mode disabled
0 = ICD Debug mode enabled

bit 12 **Unimplemented:** Read as '1'

bit 11-10 **WRT<1:0>:** Flash Program Memory Self-Write Enable bit
11 = Write protection off
10 = 000h to 3FFh write protected, 400h to FFFh may be modified by PMCON1 control
01 = 000h to 7FFh write protected, 800h to FFFh may be modified by PMCON1 control
00 = 000h to FFFh write protected, the entire program memory is write-protected

bit 9 **Unimplemented:** Read as '1'

bit 8 **BOREN:** Brown-out Reset Enable bit
1 = BOR enabled during operation and disabled in SLEEP
0 = BOR disabled

bit 7 **Unimplemented:** Read as '1'

bit 6 **$\overline{\text{CP}}$:** Code Protection bit
1 = Program memory is not code-protected
0 = Program memory is external read and write-protected

bit 5 **$\overline{\text{MCLRE}}$:** $\overline{\text{MCLR}}$ Pin Function Select bit
1 = $\overline{\text{MCLR}}$ pin is $\overline{\text{MCLR}}$ function and weak internal pull-up is enabled
0 = $\overline{\text{MCLR}}$ pin is alternate function, $\overline{\text{MCLR}}$ function is internally disabled

bit 4 **$\overline{\text{PWRTE}}$:** Power-up Timer Enable bit(1)
1 = PWRT disabled
0 = PWRT enabled

bit 3 **WDTE:** Watchdog Timer Enable bit
1 = WDT enabled
0 = WDT disabled

bit 2-0 **Unimplemented:** Read as '1'

Note 1: Bit is reserved and not controlled by user.

4.1 Device ID Word

The device ID word for the MCP19122/3 is loaded at 2006h. This location cannot be erased.

4.2 Revision ID Word

The 5-bit Revision ID is hard coded in silicon and is stored at memory location 2005h.

TABLE 4-1: DEVICE/REVISION ID VALUES

Device	Device ID	Revision ID
MCP19122	3010h	00xxh
MCP19123	3011h	00xxh

5.0 CODE PROTECTION

For the MCP19122/3, once the $\overline{CP}$ bit is programmed to '0', all program memory locations read all '0's. The user ID locations and the Configuration Word read out in an unprotected fashion. Further programming is disabled for the entire program memory.

The user ID locations and the Configuration Word can be programmed regardless of the state of the $\overline{CP}$ bit.

5.1 Disabling Code Protection

It is recommended to use the procedure in Figure 3-15 to disable code protection of the device. This sequence will erase the program memory, Configuration Word (0x2007) and user ID locations (0x2000-0x2003). The Calibration Words (0x2080 to 0x208F) **will not** be erased.

5.2 Embedding Configuration Word and User ID Information in the Hex File

To allow portability of code, the programmer is required to read the Configuration Word and user ID locations from the hex file when loading it. If Configuration Word information was not present in the hex file, a simple warning message may be issued. Similarly, while saving a hex file, Configuration Word and user ID information must be included. An option to not include this information may be provided.

5.3 Checksum Computation

The checksum is calculated by two different methods dependent on the setting of the $\overline{CP}$ Configuration bit.

5.3.1 PROGRAM CODE PROTECTION DISABLED

With the program code protection disabled, the checksum is computed by reading the contents of the program memory locations and adding up the program memory data starting at address 0x0000h, up to the maximum user addressable location. Any Carry bit exceeding 16 bits is ignored. Additionally, the relevant bits of the Configuration Words are added to the checksum. All unimplemented Configuration bits are masked to '0'.

EXAMPLE 5-1: CHECKSUM COMPUTED WITH PROGRAM CODE PROTECTION DISABLED ($\overline{CP}$ = 1), MCP19122 AND MCP19123 BLANK DEVICES

Sum of Memory addresses 000h-0FFFh		F000h (1)
Configuration Word		3FFFh (2)
Configuration Word mask		2D78h (3)
Checksum	= F000h + (3FFFh and 2D78h) (4)	
	= F000h + 2D78h	
	= 1D78h	

Note 1: This value is obtained by taking the total number of program memory locations (0x000h to 0x0FFFh, which is 0x1000h) and multiplying it by the blank memory value of 0x3FFF to get the sum of 3FF F000h. Then truncate to 16 bits, thus having a final value of F000h.

2: This value is obtained by making all bits of the Configuration Word a '1', then converting it to hex, thus having a value of 3FFFh.

3: This value is obtained by making all used bits of the Configuration Word a '1', then converting it to hex, thus having a value of 2D78h.

4: This value is obtained by ANDing the Configuration Word value with the Configuration Word Mask value and adding it to the sum of memory addresses (3FFFh and 2D78) + F000h = 11D78h. Then truncate to 16 bits, thus having a final value of 1D78h.

5.3.2 PROGRAM CODE PROTECTION ENABLED

With the program code protection enabled, the checksum is computed in the following manner. The Least Significant nibble of each user ID is used to create a 16-bit value. The masked value of user ID location 2000h is the Most Significant nibble. This sum of user IDs is summed with the Configuration Word (all unimplemented Configuration bits are masked to '0').

EXAMPLE 5-2: CHECKSUM COMPUTED WITH PROGRAM CODE PROTECTION ENABLED (CP = 0), MCP19122 AND MCP19123 BLANK DEVICES

Configuration Word	3FBFh[1]
Configuration Word mask	2D38h[2]
User ID (2000h)	0006h[3]
User ID (2001h)	0007h[3]
User ID (2002h)	0001h[3]
User ID (2003h)	0002h[3]

Sum of User IDs = (0006h and 000Fh) << 12 + (0007h and 000Fh) << 8 +
(0001h and 000Fh) << 4 + (0002h and 000Fh)[4]
= 6000h + 0700h + 0010h + 0002h
= 6712h

Checksum = (3FBFh and 2D38h) + Sum of User IDs[5]
= 2D38h + 6712h
= 944Ah

Note 1: This value is obtained by making all bits of the Configuration Word a '1', but the code protection bit is '0' (thus, enabled), then converting it to a hex, thus having a value of 3FBFh.

2: This value is obtained by making all used bits of the Configuration Word a '1', but the code protection bit is '0' (thus, enabled), then converting to hex, thus having a value of 2D38h.

3: These values are picked at random for this example; they can be any 16-bit value.

4: In order to calculate the sum of user IDs, take the 16-bit value of the first user ID location (0006h), AND the address to (000Fh), thus masking the MSB. This gives you the value 0006h. Then shift left 12 bits, giving you 6000h. Do the same procedure for the 16-bit value of the second user ID location (0007h), except shift left eight bits. Also do the same for the third user ID location (0001h), except shift left four bits. For the fourth user ID location, do not shift. Finally, add up all four user ID values to get the final sum of user IDs of 6712h.

5: This value is obtained by ANDing the Configuration Word value with the Configuration Mask value and adding it to the sum of user IDs: (3FBFh and 2D38h) + (6712h) = 944Ah.

6.0 PROGRAM/VERIFY MODE ELECTRICAL CHARACTERISTICS

TABLE 6-1: AC/DC CHARACTERISTICS TIMING REQUIREMENTS FOR PROGRAM/VERIFY MODE

AC/DC CHARACTERISTICS		**Standard Operating Conditions (unless otherwise stated)** Operating Temperature: -40°C ≤ T_A ≤ +85°C Operating Voltage: 4.5V ≤ V_{DD} ≤ 5.5V				
Characteristics	**Sym.**	**Min.**	**Typ.**	**Max.**	**Units**	**Conditions/Comments**
General						
V_{IN} level for read/write operations, program and data memory	V_{IN}	4.5	—	40	V	
V_{IN} level for Bulk Erase operations, program and data memory		4.5	—	40	V	
High voltage on $\overline{MCLR}$ for Program/Verify mode entry	V_{IHH}	V_{DD} + 3.5	—	13	V	V_{DD} regulated internally to 5V
$\overline{MCLR}$ current during programming	I_{IHH}	—	300	1000	µA	Current into the $\overline{MCLR}$ pin
$\overline{MCLR}$ rise time (V_{SS} to V_{HH}) for Program/Verify mode entry	T_{VHHR}	—	—	1.0	µs	
Hold time after V_{PP} changes	T_{PPDP}	5	—	—	µs	
(ICSPCLK, ICSPDAT) input high level	$V_{IH}1$	0.8 V_{DD}	—	—	V	Schmitt Trigger input
(ICSPCLK, ICSPDAT) input low level	$V_{IL}1$	0.2 V_{DD}	—	—	V	Schmitt Trigger input
ICSPCLK, ICSPDAT setup time before $\overline{MCLR}$↑ (Program/Verify mode selection pattern setup time)	$T_{SET}0$	100	—	—	ns	
Hold time after V_{DD} changes	$T_{HLD}0$	5	—	—	µs	
Serial Program/Verify						
Data in setup time before clock↓	$T_{SET}1$	100	—	—	ns	
Data in hold time after clock↓	$T_{HLD}1$	100	—	—	ns	
Data input not driven to next clock input (delay required between command/data or command/command)	$T_{DLY}1$	1.0	—	—	µs	
Delay between clock↓ to clock↑of next command or data	$T_{DLY}2$	1.0	—	—	µs	
Clock↓ to data out valid (during a Read Data command)	$T_{DLY}3$	—	—	80	ns	
Erase cycle time	T_{ERA}	—	5	6	ms	
Programming cycle time	T_{PROG}	3	—	—	ms	+10°C ≤ T_A ≤ +40°C
Time delay from program to compare (HV discharge time)	T_{DIS}	100	—	—	µs	

NOTES:

APPENDIX A: REVISION HISTORY

Revision A (May 2017)

- Original Release of this Document.

NOTES:

Note the following details of the code protection feature on Microchip devices:

- Microchip products meet the specification contained in their particular Microchip Data Sheet.
- Microchip believes that its family of products is one of the most secure families of its kind on the market today, when used in the intended manner and under normal conditions.
- There are dishonest and possibly illegal methods used to breach the code protection feature. All of these methods, to our knowledge, require using the Microchip products in a manner outside the operating specifications contained in Microchip's Data Sheets. Most likely, the person doing so is engaged in theft of intellectual property.
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