

## NPN POWER SWITCHING SILICON TRANSISTOR

Qualified per MIL-PRF-19500/374

**DEVICES**
**2N3996**
**2N3997**
**2N3998**
**2N3999**
**LEVELS**
**JAN**
**JANTX**
**JANTXV**
**ABSOLUTE MAXIMUM RATINGS ( $T_C = +25^\circ\text{C}$  unless otherwise noted)**

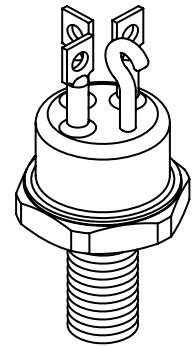
Parameters / Test Conditions	Symbol	Value	Unit
Collector-Emitter Voltage	$V_{CEO}$	80	Vdc
Collector-Base Voltage	$V_{CBO}$	100	Vdc
Emitter-Base Voltage	$V_{EBO}$	8.0	Vdc
Base Current	$I_B$	0.5	A dc
Collector Current	$I_C$	10 <sup>(1)</sup>	A dc
Total Power Dissipation	$P_T$	2.0 30	W
		@ $T_A = +25^\circ\text{C}$ <sup>(2)</sup> @ $T_C = +100^\circ\text{C}$ <sup>(3)</sup>	
Operating & Storage Junction Temperature Range	$T_J, T_{stg}$	-65 to +200	$^\circ\text{C}$
Thermal Resistance, Junction-to-Case	$R_{\theta JC}$	3.33	$^\circ\text{C}/\text{W}$

**Note:**

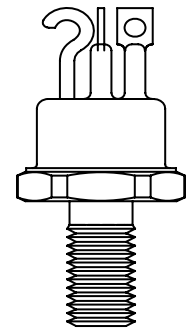
- (1) This value applies for  $T_p \leq 1.0\text{ms}$ , duty cycle  $\leq 50\%$
- (2) Derate linearly 11.4 mW/ $^\circ\text{C}$  for  $T_A > +25^\circ\text{C}$
- (3) Derate linearly 300 mW/ $^\circ\text{C}$  for  $T_C > +100^\circ\text{C}$

**ELECTRICAL CHARACTERISTICS ( $T_A = +25^\circ\text{C}$ , unless otherwise noted)**

Parameters / Test Conditions	Symbol	Min.	Max.	Unit
<b>OFF CHARACTERISTICS</b>				
Collector-Emitter Breakdown Voltage $I_C = 50\text{mA dc}$	$V_{(BR)CEO}$	80		Vdc
Collector-Emitter Breakdown Voltage $I_C = 10\mu\text{A dc}$	$V_{(BR)CBO}$	100		Vdc
Collector-Emitter Cutoff Current $V_{CE} = 60\text{Vdc}$	$I_{CEO}$		10	$\mu\text{A dc}$
Collector-Emitter Cutoff Current $V_{CE} = 80\text{Vdc}, V_{BE} = 0\text{V}$	$I_{CES}$		200	$\eta\text{A dc}$
Emitter-Base Cutoff Current $V_{EB} = 5.0\text{Vdc}$ $V_{EB} = 8.0\text{Vdc}$	$I_{EBO}$		200 10	$\eta\text{A dc}$ $\mu\text{A dc}$



**TO-111**  
**2N3996, 2N3997**



**TO-59**  
**2N3998, 2N3999**

**ELECTRICAL CHARACTERISTICS** ( $T_A = +25^\circ\text{C}$ , unless otherwise noted)

Parameters / Test Conditions	Symbol	Min.	Max.	Unit
<b>ON CHARACTERISTICS</b> <sup>(2)</sup>				
Forward-Current Transfer Ratio $I_C = 50\text{mA dc}, V_{CE} = 2.0\text{V dc}$ $I_C = 1.0\text{A dc}, V_{CE} = 2.0\text{V dc}$ $I_C = 5.0\text{A dc}, V_{CE} = 5.0\text{V dc}$ $I_C = 50\text{mA dc}, V_{CE} = 2.0\text{V dc}$ $I_C = 1.0\text{A dc}, V_{CE} = 2.0\text{V dc}$ $I_C = 5.0\text{A dc}, V_{CE} = 5.0\text{V dc}$	2N3996, 2N3998    2N3997, 2N3999	   30 40 15 60 80 20	   120 240	
Collector-Emitter Saturation Voltage $I_C = 1.0\text{A dc}, I_B = 0.1\text{A dc}$ $I_C = 5.0\text{A dc}, I_B = 0.5\text{A dc}$	$V_{CE(\text{sat})}$		0.25 2.0	Vdc
Base-Emitter Saturation Voltage $I_C = 1.0\text{A dc}, I_B = 0.1\text{A dc}$ $I_C = 5.0\text{A dc}, I_B = 0.5\text{A dc}$	$V_{BE(\text{sat})}$	0.6	1.2 1.6	Vdc

**DYNAMIC CHARACTERISTICS**

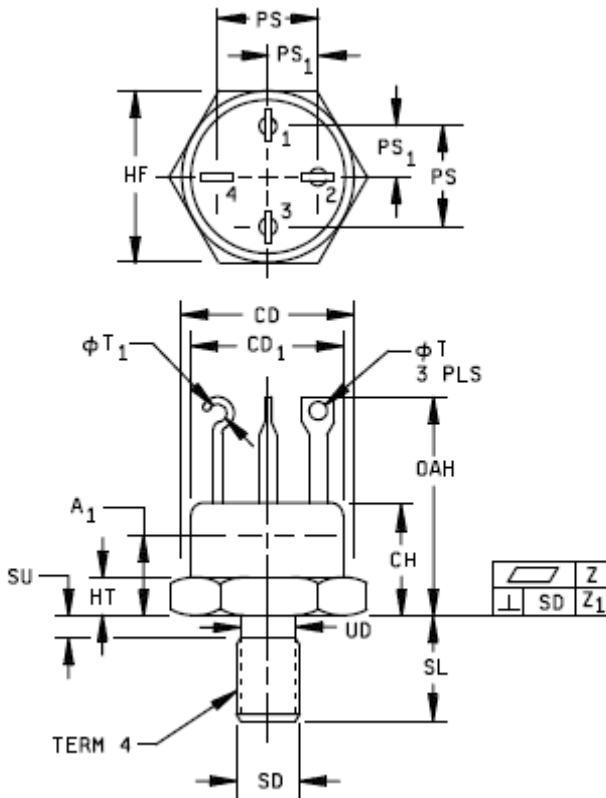
Parameters / Test Conditions	Symbol	Min.	Max.	Unit
Magnitude of Common Emitter Small-Signal Short-Circuit Forward Current Transfer Ratio $I_C = 1.0\text{A dc}, V_{CE} = 5.0\text{V dc}, f = 10\text{MHz}$	$ h_{fe} $	3.0	12	
Output Capacitance $V_{CB} = 10\text{V dc}, I_E = 0, 100\text{kHz} \leq f \leq 1.0\text{MHz}$	$C_{obo}$		150	pF

**SAFE OPERATING AREA**

<p><b>DC Tests</b>  <math>T_C = +100^\circ\text{C}</math>, 1 Cycle, <math>t = 1.0\text{s}</math>  <b>Test 1</b>  <math>V_{CE} = 80\text{V dc}, I_C = 0.08\text{A dc}</math>  <b>Test 2</b>  <math>V_{CE} = 20\text{V dc}, I_C = 1.5\text{A dc}</math></p>
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(4) Pulse Test: Pulse Width = 300 $\mu\text{s}$ , Duty Cycle  $\leq 2.0\%$ .

## PACKAGE DIMENSIONS

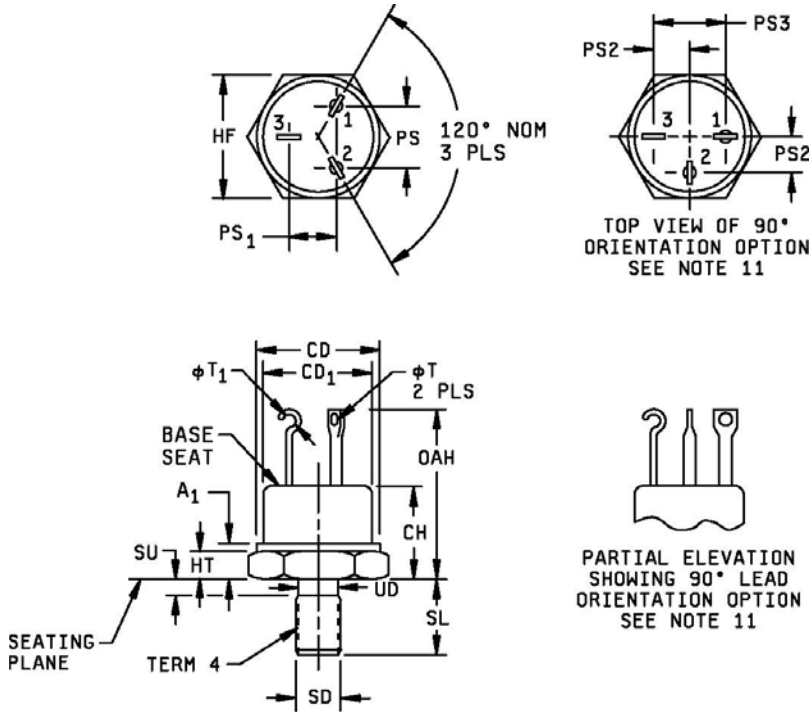


Ltr	Dimensions				Notes
	Inches		Millimeters		
	Min	Max	Min	Max	
CH	.345	.400	8.76	10.16	
A <sub>1</sub>		.250		6.35	3
CD	.370	.437	9.40	11.10	3
CD <sub>1</sub>	.318	.380	8.08	9.65	
HF	.424	.437	10.77	11.10	
PS	.180	.215	4.57	5.46	5
PS <sub>1</sub>	.080	.110	2.03	2.79	5
HT	.090	.140	2.29	3.56	2, 6
OAH	.575	.675	14.61	17.15	1
UD	.155	.189	3.94	4.80	
SL	.400	.455	10.16	11.56	
SU		.078		1.98	7
φT	.040	.065	1.02	1.65	
φT <sub>1</sub>	.040	.065	1.02	1.65	4
SD	.190-32 UNF-2A				8
Z		.002		0.05	
Z <sub>1</sub>		.006		0.15	

### NOTES:

1. Terminal 1, emitter; terminal 2, base; terminal 3, collector; terminal 4, case.
2. Chamfer or undercut on one or both ends of hexagonal portion is optional.
3. The outline contour with the exception of the hexagon is optional within cylinder defined by CD1 and A1.
4. Terminal r can be flattened and pierced or hook type. A visual index is required when the flattened and pierced tab terminal contour (identical to the adjacent terminals) option is used. The case terminal (hook) is mechanically connected to the case. The other three terminals shall be electrically isolated from the case.
5. Angular orientation of terminals with respect to hexagon is optional.
6. HT dimension does not include sealing flanges.
7. SU is the length of incomplete or undercut threads.
8. SD is the pitch diameter of coated threads. Reference: Screw threads standards for Federal Service Handbook H28, part I.
9. Dimensions are in inches.
- \* 10. Millimeters are giving for general information only.
- \* 11. In accordance with ASME Y14.5M, diameters are equivalent to φx symbology.

\* **FIGURE 1.** Physical dimensions for transistor types 2N3996 and 2N3997 - Continued.



Ltr	Dimensions				Notes
	Inches		Millimeters		
	Min	Max	Min	Max	
CH	.345	.400	8.76	10.16	
A <sub>1</sub>		.250		6.35	
CD <sub>1</sub>	.318	.380	8.08	9.65	
CD	.370	.437	9.40	11.10	
HF	.424	.437	10.77	11.10	
PS	.125	.165	3.18	4.19	4, 7, 8
PS <sub>1</sub>	.110	.145	2.79	3.68	4, 7
PS <sub>2</sub>	.090	.140	2.29	3.56	4, 7, 8
PS <sub>3</sub>	.185	.215	4.70	5.46	4, 7, 8
HT	.090	.140	2.29	3.56	
OAH	.575	.675	14.61	17.15	5
UD	.155	.189	3.94	4.80	
SL	.400	.455	10.16	11.56	
SU		.078		1.98	9
φT	.040	.065	1.02	1.65	
φT <sub>1</sub>	.040	.065	1.02	1.65	
SD	.190-32 UNF-2A				3

**NOTES:**

1. Dimensions are in inches. Millimeters are given for general information only
2. Collector shall be electrically connected to the case. This terminal may be flattened and pierced only when the 90 degree option is used.
3. SD is the pitch diameter of coated threads. Reference: Screw thread standards for Federal Service Handbook H28, part I.
4. The orientation of the terminals in relation to the hex flats is not controlled.
5. All three terminals.
6. The case temperature may be measured anywhere on the seating plane within .125 (3.18 mm) of the stud.
7. Terminal spacing measured at the base seat only.
8. Dimensions PS, PS<sub>1</sub>, PS<sub>2</sub>, and PS<sub>3</sub> are measured from the centerline of terminals.
9. Maximum unthreaded dimension.
10. This dimension applies to the location of the center line of the terminals.
11. A 90 degree angle lead orientation as shown may be used at the option of the manufacturer. All dimensions of the basic outline except PS, PS<sub>1</sub>, and the 120° lead angle apply to this option.
12. Terminal 1, emitter; terminal 2, base; terminal 3, collector.
13. A slight chamfer or undercut on one or both ends of the hexagonal is optional.
- \* 14. In accordance with ASME Y14.5M, diameters are equivalent to φx symbology.

\* **FIGURE 2.** Physical dimensions for transistor types 2N3998 and 2N3999