NXP

Freescale Semiconductor
Product Brief

MPC5676R Product Brief

32-Bit Power Architecture™ Microcontrollers for Powertrain Applications

The MPC5600 family of devices is closely compatible with the MPC5500 families, while introducing new features coupled with high performance CMOS technology to provide substantial reduction of cost per feature and significant performance improvement. This document describes the features of the MPC5676R and highlights important electrical and physical characteristics of this device.

The two e200z7 host processor cores of the MPC5676R are compatible with the Power Architecture™ Book E architecture. They are 100% user-mode compatible (with floating point library) with the classic PowerPC instruction set. The Book E architecture has enhancements that improve the architecture's fit in embedded applications. In addition to the standard and VLE Power Architecture instruction sets, this core has additional instruction support for digital signal processing (DSP).

The MPC5676R has two levels of memory hierarchy; separate 16K instruction and 16K data caches for each of two cores and 384KB of on-chip SRAM. 6MB of internal flash memory is provided. An external bus interface is also available for special packaged parts to support application development and calibration.

Contents

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1 Device Description

1.1 Family Comparison

The following table lists a summary of major features of the family of devices defined in this document, and their comparison with devices in earlier families of similar devices. The feature column represents a combination of module names and capabilities of certain modules. A summary of the functionality provided by each on chip module is given later in this document.

Table 1. Family Comparison

Feature	MPC5554	MPC5565	MPC5567	MPC5566	MPC5674F	MPC5676R
Process	130 nm	130 nm	130 nm	130 nm	90 nm	90 nm
Core	z6	z6	z6	z6	z7	z7[1]
Number of Cores	1	1	1	1	1	2
Single Precision Floating Point	Yes	Yes	Yes	Yes	Yes	Yes
SIMD	Yes	Yes	Yes	Yes	Yes	Yes
VLE	No	Yes	Yes	Yes	Yes	Yes
Cache	32KB Unified	8KB Unified	8KB Unified	32KB Unified	16KB Instruction + 16KB Data	16KB Instruction + 16KB Data
Non-maskable Interrupt	No	No	No	No	NMI, Critical	NMI, Critical
MMU Entries	32	32	32	32	64	32
MMU Tool Control	No	No	No	No	No	Yes
MPU	No	No	No	No	Yes	Yes
Semaphores	No	No	No	No	No	16
CRC Channels	No	No	No	No	No	3
Software Watchdog Timer	No	No	No	No	1	2
Core Nexus Class	3+	3+	3+	3+	3+	3+
SRAM	64KB (32K Standby)	64KB (32K Standby)	64KB (32K Standby)	128KB (32K Standby)	256KB (32K Standby)	384KB (48K Standby)
Flash	2MB	2MB	2MB	3MB	4MB	6MB
Flash fetch accelerator	2 x 256 bit	2 x 256 bit	2 x 256 bit	2 x 256 bit	4 x 256 bit	4 x 256 bit
External bus	32 bit	32 bit	32 bit	32 bit	Yes[2]	Yes[2]
Calibration bus	No	16 bit	16 bit	16 bit	16 bit non-mux 16, 32 bit muxed[3]	16 bit non-mux 16, 32 bit muxed[3]
DMA channels	64	32	32	64	64 + 32	64 + 64
DMA Nexus Class	3	3	3	3	3	3
Serial Interface	2	2	2	2	3	3

Table 1. Family Comparison

Feature	MPC5554	MPC5565	MPC5567	MPC5566	MPC5674F	MPC5676R
FlexCAN	3	3	5	4	4	4
SPI	4	3	3	4	4	5
Microsecond bus downlink	No	No	No	No	Yes	Yes
FlexRay	No	No	Yes	No	Yes	Yes
Ethernet	No	No	Yes	Yes	No	No
System Timers	No	No	No	No	8 PIT chan 4 AutoSAR	8 PIT chan 4 AutoSAR
eMIOS channels	24	24	24	24	32	32
eTPU channels	64	32	32	64	64	96
eTPU Version	2 x eTPU	1 x eTPU	1 x eTPU	2 x eTPU	2 x eTPU2	3 x eTPU2
eTPU Code memory	16KB	12KB	12KB	12KB	24KB	24KB + 12KB
eTPU Data memory	3KB	2.5KB	2.5KB	3KB	6KB	6KB + 3KB
Interrupt controller	308 sources	210 sources	210 sources	308 sources	448 sources	500 sources
ADC Input Pins	40	40	40	40	64	64
ADC Input diagnostics	No	No	No	No	Yes	Yes
ADC Resolution	12 bit	12 bit	12 bit	12 bit	12 bit	12 bit
ADC Quantity	2	2	2	2	4	4
ADC variable gain amp.	No	No	No	No	Yes	Yes
Temp. sensor	No	No	No	No	Yes	Yes
Decimation filters	No	No	No	No	8	12
Protected Port Output	No	No	No	No	No	4
Self Test Controller	No	No	No	No	No	Yes
Dev Tool Semaphores	No	No	No	No	No	32
PLL	FM	FM	FM	FM	FM	FM
Integrated linear voltage regulator	1.5V	1.5V	1.5V	1.5V	3.3V, 1.2V	3.3V, 1.2V
Integrated switch mode voltage regulator	No	No	No	No	1.2V	1.2V
External Power Supplies	5V, 3.3V	5V, 3.3V	5V, 3.3V	5V, 3.3V	5V[4]	5V[4]
Low Power Modes	No	No	No	No	Stop Mode Slow Mode	Stop Mode Slow Mode

NOTES:

[1] There are 2 cores on the MPC5676R. Both cores have identical features.

[2] External Bus Interface (EBI) is not available on 416 PBGA

MPC5676R Product Brief, Rev. 2
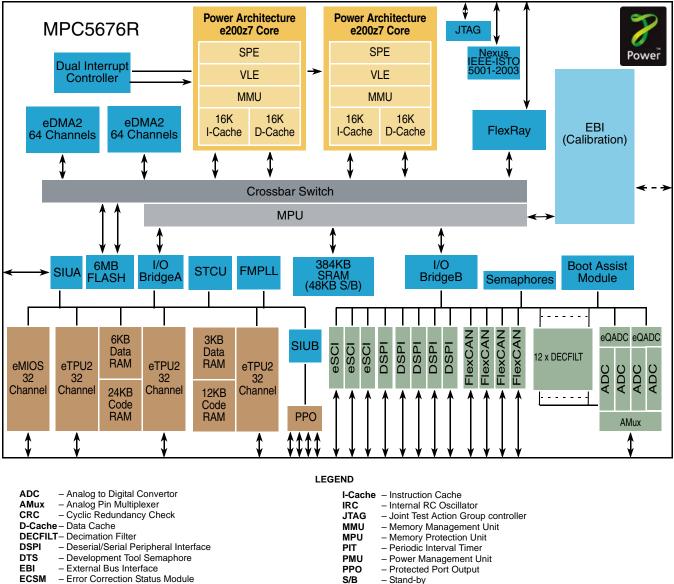
3 Cal bus is combined with EBI

4 External 3.3V may be needed for external 3.3V pins.

1.2   Block Diagram

The following figure shows a top-level block diagram of the MPC5676R. The purpose of the block diagram is to show the general interconnection of functional modules through the crossbar switch and from the Dual Interrupt Controller, and provide an indication of the modules that connect to external pins. For clarity, the following modules are omitted from the diagram: PMU, SWT, STM, PIT, ECSM, DTS, CRC.

LEGEND

ADC	– Analog to Digital Convertor	**I-Cache**	– Instruction Cache
AMux	– Analog Pin Multiplexer	**IRC**	– Internal RC Oscillator
CRC	– Cyclic Redundancy Check	**JTAG**	– Joint Test Action Group controller
D-Cache	– Data Cache	**MMU**	– Memory Management Unit
DECFILT	– Decimation Filter	**MPU**	– Memory Protection Unit
DSPI	– Deserial/Serial Peripheral Interface	**PIT**	– Periodic Interval Timer
DTS	– Development Tool Semaphore	**PMU**	– Power Management Unit
EBI	– External Bus Interface	**PPO**	– Protected Port Output
ECSM	– Error Correction Status Module	**S/B**	– Stand-by
eDMA2	– Enhanced Direct Memory Access controller version 2	**SIUA**	– System Integration Unit A
eMIOS	– Enhanced Modular I/O System	**SIUB**	– System Integration Unit B
eQADC	– Enhanced Queued Analog to Digital Converter	**SPE**	– Signal Processing Engine
eSCI	– Enhanced Serial Communications Interface	**SRAM**	– Static RAM
eTPU2	– Enhanced Time Processing Unit version 2	**STCU**	– Self Test Control Unit
FlexCAN	– Flexible Controller Area Network controller	**STM**	– System Timer Module
FMPLL	– Frequency Modulated Phase Lock Loop clock generator	**SWT**	– Software Watchdog Timer
		VLE	– Variable Length instruction Encoding

Figure 1. MPC5676R Block Diagram

1.3 Critical Performance Parameters

The critical performance parameters of the MPC5676R feature the following:

- Maximum CPU frequency: 184MHz
- Junction temperature range: –40° to 150° C
- Nominal power dissipation is less than 1.4W, while enhancements to allow reduced power operation using clock gating are included
- Separately powered stand-by SRAM

1.4 Packages

The MPC5676R is offered in the following package types:

- 416-ball PBGA, 1 mm ball pitch, 27 mm × 27 mm outline, without EBI
- 516-ball PBGA, 1 mm ball pitch, 27 mm × 27 mm outline, with EBI
- VertiCal Calibration System (includes EBI)

1.5 Features Summary

On-chip modules available within the family include the following features:

- Two identical dual issue, 32-bit CPU core complexes (e200z7), each with
  — Power Architecture embedded specification compliance
  — Instruction set enhancement allowing variable length encoding (VLE), optional encoding of mixed 16-bit and 32-bit instructions, for code size footprint reduction
  — Signal processing extension (SPE) instruction support for digital sigal processing (DSP)
  — Single-precision floating point operations
  — 16 KB I-Cache and 16 KB D-Cache
  — Hardware cache coherency between cores
- 16 Hardware semaphores
- 3 channel CRC module
- 6MB on-chip flash
  — Supports read during program and erase operations, and multiple blocks allowing EEPROM emulation
- 384KB on-chip general-purpose SRAM including 48KB of standby RAM
- Two Multi channel direct memory access controllers (eDMA)
  — 64 channels per eDMA
- Dual core Interrupt controller (INTC)
- Phase-locked loop with FM modulation (FMPLL)
- Crossbar switch architecture for concurrent access to peripherals, flash, or RAM from multiple bus masters
- External Bus Interface (EBI) for calibration and application development

- System integration unit (SIU) with error correction status module (ECSM)
- Four protected port output pins (PPO)
- Boot assist module (BAM) supports serial bootload via CAN or SCI
- Three second-generation enhanced time processor units (eTPU2)
  - 32 channels per eTPU2
  - total of 36 KB code RAM
  - total of 9 KB parameter RAM
- Enhanced modular input output system supporting 32 unified channels (eMIOS) with each channel capable of single action, double action, pulse width modulation (PWM) and modulus counter operation
- Two enhanced queued analog-to-digital converter (eQADC) modules with
  - two separate analog converters per eQADC module
  - support for a total of 64 analog input pins, expandable to 176 inputs with off-chip multiplexers
  - one absolute reference ADC channel
  - interface to twelve hardware decimation filters
  - enhanced 'Tap' command to route any conversion to two separate decimation filters
- Five deserial serial peripheral interface (DSPI) modules
- Three enhanced serial communication interface (eSCI) modules
- Four controller area network (FlexCAN) modules
- Dual-channel FlexRay controller
- Nexus development interface (NDI) per IEEE-ISTO 5001-2003 standard, with some support for 2010 standard.
- Device and board test support per Joint Test Action Group (JTAG) (IEEE 1149.1)
- On-chip voltage regulator controller regulates supply voltage down to 1.2 V for core logic
- Self Test capability

1.6   Module Summaries

The following sections provide more details of the modules implemented on the MPC5676R.

1.6.1   High-Performance e200z7 Core Processor

The e200z7 cores each include the following features:
- Dual-issue, 32-bit Power Architecture CPU
- 32-bit Power Architecture Book E programmer's model
- Full hardware cache coherency support to ensure data coherency with no software overhead
- 64-bit general-purpose registers (GPRs) that support vector instructions defined by the SPE APU
  - All arithmetic instructions that execute in the core operate on data in the GPRs

- Enhanced signal processing extension (SPE) APU that supports real-time fixed point and single-precision embedded numerics operations using the GPRs
- Variable length encoding (VLE) enhancements
  — Allows optional encoding of mixed 16-bit and 32-bit instructions
  — Results in smaller code size footprint
  — Minimizes impact on performance
- Six read and three write operations per clock
  — Integrates a pair of integer execution units, a branch control unit, instruction fetch unit and load/store unit, and a multi-ported register file
- Branch target prefetching performed by the branch unit allows single-cycle branches in many cases
- 16 KB instruction cache and 16 KB data cache, both supporting error detection hardware.
- Memory management unit (MMU) with 32-entry fully-associative translation look-aside buffer (TLB)
  — Non-intrusive support for MMU selection from an external tool
- Nexus Class 3+ module
- Supports non-maskable interrupt (completely un-maskable and not guaranteed to be recoverable) and critical interrupt (an interrupt that can be masked and is guaranteed to be recoverable) sources
  — Routed from a single package pin, via edge detection logic in the SIU, to the CPU
- An additional Wait for Interrupt instruction:
  — Used in conjunction with low power STOP mode
  — Instruction stops the system clock
  — An external interrupt source or the system wake-up timer restart the system clock, allowing the CPU to service the interrupt
- Includes multiple input signature register (MISR) hardware which can be accessed by software to implement CPU self test functionality

1.6.2   Crossbar Switch

The following summarizes the MPC5676R's implementation of the crossbar switch:

- Supports simultaneous connections between master ports and slave ports
- Supports a 32-bit address bus width and a 64-bit data bus width
- Seven master ports:
  — core 0 instruction
  — core 0 data
  — core 1 instruction
  — core 1 data
  — eDMA2 module A
  — eDMA2 module B
  — FlexRay

- Six slave ports
  - core 0 flash
  - flash
  - EBI
  - SRAM
  - peripheral bridge A
  - peripheral bridge B
- Arbitration logic for when a slave port is simultaneously requested by more than one master
- Includes memory protection unit (MPU) hardware to guard against unintended SRAM or peripheral accesses by the cores, eDMA2 modules, EBI and FlexRay module.

1.6.3   Enhanced Direct Memory Access Controller (eDMA2)

The MPC5676R implements an enhanced direct memory controller with the following features:

- Second-generation module capable of performing complex data movements via a total of 64 programmable channels, without intervention from the host processor
- DMA engine
  - Performs source and destination address calculations
  - Performs data movement operations
- Includes SRAM-based memory containing the transfer control descriptors (TCD) for the channels.
- All data movement via dual-address transfers: read from source, write to destination
- Programmable source and destination addresses, transfer size, plus support for enhanced addressing modes
- TCD organized to support two-deep, nested transfer operations
- An inner data transfer loop defined by a "minor" byte transfer count
- An outer data transfer loop defined by a "major" iteration count
- Channel activation via one of three methods:
  - Explicit software initiation
  - Initiation via a channel-to-channel linking mechanism for continuous transfers
  - Peripheral-paced hardware requests (one per channel)
- Support for programmable priority and round-robin channel arbitration
- Channel completion reported via optional interrupt requests
- One interrupt per channel, optionally asserted at completion of major iteration count
- Error termination interrupts are optionally enabled
- Support for scatter/gather DMA processing
- Channel transfers can be suspended by a higher priority channel
- Nexus data trace support on each DMA

1.6.4 Dual Interrupt Controller (INTC)

The MPC5676R implements an interrupt controller that features the following:

- Priority-based preemptive scheduling of interrupt service requests (ISRs), suitable for statically scheduled hard real-time systems
- Ample number of priorities so that lower priority ISRs do not delay the execution of higher priority ISRs
- Software-configurable priorities of ISR or tasks
  — Modifying the priority can be used to implement the priority ceiling protocol for accessing shared resources
- A unique vector for each interrupt request source for quick determination of which ISR needs to be executed
- Support for a critical or non maskable interrupt
- Interrupt steering between cores
  — Independent selection of any interrupt source to be routed to either or both cores
  — Interrupts share same priority level between cores

1.6.5 Frequency-Modulated PLL (FMPLL)

The FMPLL allows the user to generate high speed system clocks using a 4 MHz to 40 MHz crystal oscillator or external clock generator. Further, the FMPLL supports programmable frequency modulation of the system clock to reduce electromagnetic emission. The PLL multiplication factor and output clock divider ratio are all software configurable. The PLL has the following major features:

- Voltage controlled oscillator (VCO) range from 192 MHz to 680 MHz
- Reduced frequency divider (RFD) for reduced frequency operation without requiring PLL relock
- Three modes of operation
  — Bypass mode with PLL off
  — Bypass mode with PLL running
  — PLL normal mode
- Each of the three modes may be run with a crystal oscillator or an external clock reference
- Programmable frequency modulation [1]
  — Modulation enabled/disabled through software
  — Triangle wave modulation
  — Programmable modulation depth
  — Programmable modulation frequency dependent on reference frequency
- Lock detect circuitry reports when the PLL has achieved frequency lock and continuously monitors lock status to report loss of lock conditions
- Programmable interrupt request or system reset on loss of lock
- Self-clocked mode (SCM) operation allows continued operation after failure of crystal clock

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1. You must configure the FMPLL to ensure that the maximum specified system frequency is not exceeded when frequency modulation is enabled.

- Configuration registers defined as an upwardly compatible superset of MPC5500 FMPLL registers
- After reset, the device starts up from an internal RC oscillator, trimmed to 16MHz. User software may then configure and enable use of the PLL.

1.6.6 External Bus Interface (EBI)

The external bus supports calibration and/or standard external memory mapped peripherals, static RAM or non-volatile memory.

The bus consists of :

- 32 address/data signals to support 16-bit or 32-bit multiplexed address/data transfers.
- 1 ALE (address latch enable) signal to support address/data demultiplexing.
- 4 CS (chip selects) signals to support up to four 8 MB banks of data space
- 1 RD_WR (read/write) signal
- 4 WE/BE (write enable/byte enable) signals to support different sized accesses to external memory (byte, halfword and word)
- 1 OE (output enable) signal
- 1 BDIP (burst data in progress) signal to support burst memory
- 1 TS (transfer start) signal typically used to latch the address in synchronous memories
- 1 TA (transfer acknowledge) signal, used in rare applications to receive data transfer acknowledgement from an external memory
- 1 CLKOUT (clock out) signal
- 1 TEA (transfer error acknowledge) signal for custom external logic or external data memory error detection

The external bus signals are available in the 516 PBGA package and the VertiCal Calibration System.

1.6.7 System Integration Unit

The SIU is accessed by the e200z7 cores through the crossbar switch and provides the following features:

- System configuration
  — MCU reset configuration via external pins
  — Pad configuration control for each pad
  — Control of virtual IO via DSPI serialization
- System reset monitoring and generation
  — Power-on reset support
  — Reset status register provides last reset source to software
  — Glitch detection on reset input
  — Software controlled reset assertion
- External interrupt
  — Sixteen interrupt requests per core
  — Rising or falling edge event detection

- — Programmable digital filter for glitch rejection
- — Critical interrupt request
- — Non maskable interrupt request
- GPIO
  - — Virtual GPIO via DSPI serialization (requires external deserialization device)
  - — Dedicated input and output registers for setting each GPIO and virtual-GPIO pin
- Internal multiplexing
  - — Allows serial and parallel chaining of DSPIs
  - — Allows flexible selection of eQADC trigger inputs
  - — Allows selection of interrupt requests between external pins and DSPI
- Protected Port Output
  - — Four GPIOs which may be reserved exclusively by one core

1.6.8   Error Correction Status Module (ECSM)

The ECSM provides the following:

- Status information regarding platform memory errors reported by error detection code (EDC) and error correcting code (ECC) hardware
- Includes facilities to allow CPU software to test the ECC and EDC operation for on-chip memories by supporting injection of arbitrary error patterns

1.6.9   On-Chip Flash

The flash module provides the following:

- 6MB of programmable, non-volatile, flash memory
  - — Nonvolatile memory (NVM) can be used for instruction and/or data storage
- A fetch accelerator dedicated to each core optimizes the performance of the flash array to match the CPU architecture
  - — Architected to optimize the performance of the flash with the CPUs to provide single-cycle random access operation
  - — Configurable read buffering and line prefetch support
- An interface between the system bus and a dedicated flash memory array controller
- Supports a 64-bit data bus width at the system bus port for CPU loads, DMA transfers and CPU instruction fetch
  - — Byte, halfword, word, and doubleword reads are supported
  - — Only aligned word and doubleword writes are supported
- Hardware and software configurable read and write access protections on a per-master basis
- Interface to the flash array controller is pipelined allowing overlapped accesses to proceed in parallel for interleaved or pipelined flash array designs
- Configurable access timing allowing use in a wide range of system frequencies

- Multiple-mapping support and mapping-based block access timing (0–31 additional cycles) allowing use for emulation of other memory types
- Software programmable block program/erase restriction control
- ECC with single-bit correction, double-bit detection
- Minimum program size is two consecutive 32-bit words, aligned on a 0-modulo-8 byte address
- Embedded hardware program and erase algorithm
- Erase suspend, program suspend and erase-suspended program
- Shadow information stored in non-volatile shadow block
- Independent program/erase of the shadow block

1.6.10 General-Purpose Static RAM (SRAM)

The SRAM includes these features:

- 384KB of static RAM
- Supports read/write accesses mapped to the SRAM memory from any master
- 48 KB block may be powered by separate supply for standby operation (contents retained)
- Byte, halfword, word, and doubleword addressable
- ECC performs single-bit correction, double-bit detection on 64-bit data elements
- ECC single-bit error corrections are optionally visible to software

1.6.11 Cyclic Redundancy Check Module (CRC)

The MPC5676R implements a CRC module that has the following features:

- Three independent engines for concurrent CRC computation of up to three memory contexts
- Two choices of polynomials (CRC-32 ethernet and CRC-16-CCITT) per context
- Support for byte, half-word and word width of the input data stream
- Optional bit-swap and bit-inversion operations of the final CRC signature
- Support for DMA data transfers

1.6.12 Semaphore Module

The semaphores module implements hardware-enforced semaphores as a peripheral device and has these major features:

- Support for 16 hardware-enforced gates in a dual-processor configuration
- Optionally enabled interrupt notification after a failed lock write provides a mechanism to indicate the gate is unlocked
- Secure reset mechanisms are supported to clear the contents of semaphore gates or notification logic

1.6.13 Protected Port Output Module (PPO)

The MPC5676R implements a protected port output module that has the following features:

- Four general purpose I/O pins
- Configurable after reset for restricted access by one core
- Default configuration provides unrestricted access by either core

1.6.14 Boot Assist Module (BAM)

The BAM is a block of read-only memory containing code that is executed every time the MCU is powered-on or reset in normal mode. The BAM supports multiple boot modes:

- Booting from internal flash memory
- Single-master booting from external memory
- Serial boot loading (a program is downloaded into on-chip general-purpose SRAM via eSCI or the FlexCAN and then executed)

The BAM also reads the reset configuration half word (RCHW) from memory (either internal flash or external user-implemented memory) and configures the MPC5676R hardware accordingly. The BAM provides the following features:

- Sets up MMU to map all resources with the minimum physical-to-logical address translations
- Sets up the MMU to allow application code to execute as either Power Architecture Book E code (default) or as Freescale VLE code
- Locates and branches to application code start address
- Automatic switch to serial boot mode if internal flash is blank or invalid
- Supports software-programmable 64-bit password protection for serial boot mode
- Autobaud function in SCI and CAN download mode
- Supports censorship protection for internal flash memory
- Provides an option to enable the software watchdog timer

1.6.15 Enhanced Modular Input Output System (eMIOS)

The eMIOS module provides the functionality to generate or measure time events. A unified channel (UC) module is employed that provides a superset of the functionality of all of the eMIOS channels used on MPC5500 family devices, while providing a consistent user interface. This allows more flexibility as each unified channel can be programmed for different functions in different applications. To identify up to two timed events, each UC contains two comparators, a time base selector and registers. This structure is able to produce match events, which can be configured to measure or generate a waveform. Alternatively, input events can be used to capture the time base, allowing measurement of an input signal. The eMIOS provides the following features:

- 32 unified channels, featuring:
  - 24-bit registers for capture/match values
  - 24-bit internal counter
  - Global prescaler

- — Pin for input/output (each channel signal is routed to a pin, however, most pins are also multiplexed with other signals)
- — Dedicated output pin for buffer direction control
- — Selectable time base
- — Can generate its own time base
- Five 24-bit wide counter buses
  - — Counter bus A can be driven by unified channel 23
  - — Counter bus B, C, D and E are driven by unified channels 0, 8, 16, and 24, respectively
  - — Counter bus A can be shared among all unified channels. UCs 0 to 7, 8 to 15, 16 to 23, and 24 to 31 can share counter buses B, C, D and E, respectively
- Shared time bases with the eTPU2
- Synchronization among internal and external time bases
- State of timer can be frozen for debug purposes

1.6.16   Enhanced Timing Processor Unit (eTPU2)

The eTPU2 is the second generation of the enhanced timing co-processor (eTPU) that was used on the MPC5500 family. eTPU2 is fully upward compatible with eTPU, runs the same binary code image, and can be used with the same tool suite. eTPU2 includes many enhancements to improve efficiency of compilers, functionality, ease of programming and operability while maintaining the same overall architecture. Some of these enhancements may be accessed using the existing compiler tool chain, while other enhancements require updates to the compiler.

The eTPU2 includes these features:

- 32 standard channels, each channel is associated with one input and one output signal
- Two independent 24-bit time bases for channel synchronization:
- Event-triggered microengine
- Resource sharing features support channel use of common channel registers, memory and microengine execution time
  - — Hardware scheduler works as a task management unit, dispatching event service routines by pre-defined, host-configured priority
  - — Channel context switch time is six system cycles. Each channel has its own context of static data memory and timer hardware resources consisting of programmable flags, timer control and status hardware
  - — SPRAM shared between host CPU and eTPU, supporting communication either between channels and host or inter-channel
  - — Dual-parameter coherency hardware support allows atomic access to two parameters by host
  - — Enhancements to DMA and interrupt structure to allow any channel to assert any interrupt source or DMA trigger
- Test and development support features:
  - — IEEE-ISTO 5001-2003 standard class 3 compliant for the eTPU (Nexus)
  - — Data trace via data write messaging and data read messaging

— Ownership trace via ownership trace messaging (OTM)

— Program trace via branch trace messaging

— Watchpoint messaging via the auxiliary port

— SCM continuous signature-check built-in self test (MISC — multiple input signature calculator), runs concurrently with eTPU normal operation

1.6.16.1 eTPU2 Configuration

On this device, the eTPU2 modules are partitioned into two configurations.

- One configuration that contains two eTPU2s that share 24K bytes of program space and 6K bytes of data space (parameter RAM)
- One configuration that contains a single eTPU2 with a private 6K bytes of program space and 3K bytes of data space (parameter RAM)

1.6.17 Enhanced Queued Analog to Digital Converter (eQADC)

The enhanced queued analog to digital converter (eQADC) block provides accurate and fast conversions for a wide range of applications. The eQADC provides a parallel interface to two on-chip analog to digital converters (ADC).

The ADCs include features designed to allow the direct connection of high impedance acoustic sensors that can be used to detect engine knock, for example. These features include differential inputs, integrated variable gain amplifiers for increasing the dynamic range, programmable pullup and pulldown resistors for biasing and sensor diagnostics.

The eQADC supports access to the programmable decimation filters.

Each eQADC provides the following features:

- Two on-chip ADC converters
  - A maximum of 12 bit ADC resolution
  - Programmable resolution for increased conversion speed (12 bit, 10 bit, 8 bit)
    - 12-bit conversion time = 1 uS (1M sample/sec)
    - 10-bit conversion time = 867 nS (1.2M sample/sec)
    - 8-bit conversion time = 733 nS (1.4M sample/sec)
  - Up to 10-bit accuracy at 500 KSample/s and 8-bit accuracy at 1 MSample/s
  - Differential conversions
  - Single-ended signal range from 0 to 5 V
  - Variable gain amplifiers on differential inputs (x1, x2, x4)
  - Sample times of 2 (default), 8, 64, or 128 ADC clock cycles
  - Time stamp information when requested
  - Right-justified unsigned or signed formats for conversion results
- 40 input channels
- 8 additional internal channels for measuring control and monitoring voltages inside the device

- — Including core voltage, IO voltage, and low-voltage interrupt (LVI) voltages
- Up to 8 inputs can be configured as 4 pairs of differential analog input channels
  - — Programmable pull-up/pull-down resistors on each differential input
- Silicon die temperature sensor
  - — provides temperature of silicon as an analog value
  - — read using an internal ADC analog channel
- Priority based queues
- Trigger sources include software, timer channels and input pins
- Support for an additional channels via external multiplexing

1.6.17.1   eQADC Configuration

On this device, there are two separate eQADC modules with identical characteristics. A total of 64 analog input signals can be accessed using the on-chip analog multiplexer. The input signals are partitioned between the two eQADC modules:

- Both have access to 16 input signals that are shared between the modules
- Each has access to 24 signals that are not shared.

On-chip analog and digital interface signals are provided to expand the number of analog signals to 176 using external multiplexers.

1.6.18   Decimation Filters

Each decimation filter is capable of high speed processing of ADC conversion results, either directly from the ADC hardware, or from results stored in memory. The filter supports optional down-sampling to lower the data rate of the filter output, cascading and windowed integration, as well as windowing of the non-integrated result.

Each decimation filter includes the following features:

- Programmable decimation factor (2 to 16)
- Fully programmable 4th order IIR or 8th order FIR
- Saturated or non-saturated modes
- Programmable rounding (convergent; two's complement; truncated)
- Pre-fill mode to pre-condition the filter before the sample window opens
- Filters may be cascaded to increase filter order
- ADC conversions may be routed to one or two selected filters
- Filter output may be routed to a windowed absolute integrator

1.6.19   Deserial Serial Peripheral Interface Module (DSPI)

The deserial serial peripheral interface (DSPI) block provides a synchronous serial interface for communication to external devices. The DSPI features the following:

- Supports pin count reduction through serialization and deserialization of eTPU and eMIOS channels and memory-mapped registers
- Channels and register content are transmitted using a SPI protocol
  — The protocol is completely configurable for baud rate, polarity, phase, frame length, chip select assertion, etc.
  — Each bit in the frame may be configured to serialize either eTPU channels, eMIOS channels or GPIO signals
- Can be configured to serialize data to an external device that is compatible with the Microsecond Bus protocol
- DSPI pins support 5 V logic levels or low voltage differential signalling (LVDS) to improve high-speed operation on data and clock signals

The DSPIs have multiple configurations:

- Serial peripheral interface (SPI) configuration where the DSPI operates as an up-to-16-bit SPI with support for queues
- Deserial serial interface (DSI) configuration where the DSPI serializes up to 32 bits from eTPU, eMIOS or GPIO output channels and deserializes the received data by placing it on the eTPU, eMIOS or GPIO input channels
- Combined serial interface (CSI) configuration where the DSPI operates in both SPI and DSI configurations interleaving DSI frames with SPI frames, giving priority to SPI frames
- Enhanced deserial serial interface (DSI) configuration where DSPI serializes up to 32 bits with three possible sources per bit
  — eTPU, eMIOS, new virtual GPIO registers as possible bit source
  — programmable inter-frame gap in coutinuous mode
  — bit source selection allows microsecond bus downlink with command or data frames up to 32 bits
  — microsecond bus dual receiver mode

For queued operations, the SPI queues reside in system memory external to the DSPI. Data transfers between the memory and the DSPI FIFOs are accomplished through the use of the eDMA2 controller or through host software.

1.6.20   Enhanced Serial Communication Interface Module (eSCI)

Each eSCI allows asynchronous serial communications with peripheral devices and other MCUs. It includes special support to interface to local interconnect network (LIN) slave devices. The eSCI block provides the following features:

- Full-duplex operation
- Standard mark/space non-return-to-zero (NRZ) format

- 13-bit baud rate selection
- Programmable 8-bit, 9-bit, 12-bit, 13-bit data format
- Automatic parity generation
- Compatible with external devices that support the Microsecond Bus upstream protocol
- LIN support
  — Autonomous transmission of entire frames
  — Configurable to support all revisions of the LIN standard
  — Automatic parity bit generation
  — Double stop bit after bit error
  — 10- or 13-bit break support
- Separately enabled transmitter and receiver
- Programmable transmitter output parity
- Two receiver wake-up methods, idle line and address mark
- Interrupt-driven operation with flags
- Receiver framing error detection
- Hardware parity checking
- 1/16 bit-time noise detection
- DMA support for both transmit and receive data
  — Global error bit stored with receive data in general-purpose SRAM to allow post processing of errors

1.6.21   FlexCAN

The FlexCAN module is a communication controller implementing the CAN protocol according to Bosch Specification version 2.0B. The CAN protocol was designed to be used primarily as a vehicle serial data bus, meeting the specific requirements of this field: real-time processing, reliable operation in the EMI environment of a vehicle, cost-effectiveness and adequate bandwidth.

Each FlexCAN module provides the following features:

- 64 message buffers (MB) of zero to eight bytes data length
- Based on and including all existing features of the Freescale TouCAN module
- Full implementation of the CAN protocol specification, Version 2.0B
  — Standard data and remote frames
  — Extended data and remote frames
  — Zero to eight bytes data length
  — Programmable bit rate up to 1 Mb/sec
  — Content-related addressing
- Each MB configurable as receive (Rx) or transmit (Tx), all supporting standard and extended messages
- Individual Rx mask registers per message buffer
- Includes 1056 bytes of RAM used for message buffer storage

- Includes 256 bytes of RAM used for individual Rx mask registers
- Full featured Rx FIFO with storage capacity for six frames and internal pointer handling
- Powerful Rx FIFO ID filtering, capable of matching incoming IDs against either eight extended, 16 standard, or 32 partial (8 bits) IDs, with individual masking capability
- Selectable backwards compatibility with previous FlexCAN version
- Programmable clock source to the CAN protocol interface, either bus clock or crystal oscillator
- Unused message buffer and Rx mask register space can be used as general-purpose RAM space
- Listen-only mode capability
- Programmable loop-back mode supporting self-test operation
- Programmable transmission priority scheme: lowest ID, lowest buffer number or local priority on individual Tx message buffers.
- Hardware cancellation on Tx message buffers.
- Time stamp based on 16-bit free-running timer
- Global network time, synchronized by a specific message
- Maskable interrupts
- Independent of the transmission medium (an external transceiver is assumed)
- Short latency time due to an arbitration scheme for high-priority messages
- Low-power modes, with programmable wake-up on bus activity

1.6.22   Dual-Channel FlexRay Controller

The FlexRay controller fully implements the FlexRay Protocol Specification Version 2.1 Rev A. The FlexRay protocol is designed to facilitate implementation of fault tolerant, time-triggered, and highly dependable automotive control systems by offering a fault tolerant clock synchronization mechanism. The FlexRay protocol maintains the global time across the functional nodes of a network with a precision (jitter) of maximum 1 µs at a data rate of 10 Mbit/s and redundant communication channels.

The FlexRay controller provides the following features:

- FlexRay Communications System Protocol Specification, Version 2.1 Rev A compliant protocol implementation
- FlexRay Communications System Electrical Physical Layer Specification, Version 2.1 Rev A compliant bus driver interface
- Single channel support
  — FlexRay Port A can be configured to be connected either to physical FlexRay channel A or physical FlexRay channel B.
- FlexRay bus data rates of 10 Mbit/s, 8 Mbit/s, 5 Mbit/s, and 2.5 Mbit/s supported
- 128 configurable message buffers with
  — individual frame ID filtering
  — individual channel ID filtering
  — individual cycle counter filtering
- Message buffer header, status and payload data stored in dedicated FlexRay memory

- — allows for flexible and efficient message buffer implementation
- — consistent data access ensured by means of buffer locking scheme
- — application can lock multiple buffers at the same time
- Size of message buffer payload data section configurable from 0 to 254 bytes
- Two independent message buffer segments with configurable size of payload data section
  - — each segment can contain message buffers assigned to the static segment and message buffers assigned to the dynamic segment at the same time
- Zero padding for transmit message buffers in static segment
  - — applied when the frame payload length exceeds the size of the message buffer data section
- Transmit message buffers configurable with state/event semantics
- Message buffers can be configured as
  - — receive message buffer
  - — single buffered transmit message buffer
  - — double buffered transmit message buffer (combines two single buffered message buffer)
- Individual message buffer reconfiguration supported
  - — means provided to safely disable individual message buffers
  - — disabled message buffers can be reconfigured
- Two independent receive FIFOs
  - — one receive FIFO per channel
  - — up to 255 entries for each FIFO
  - — global frame ID filtering, based on both value/mask filters and range filters
  - — global channel ID filtering
  - — global message ID filtering for the dynamic segment
- Four configurable slot error counters
- Four dedicated slot status indicators
  - — used to observe slots without using receive message buffers
- Measured value indicators for the clock synchronization
  - — internal synchronization frame ID and synchronization frame measurement tables can be copied into the FlexRay memory
- Fractional macroticks are supported for clock correction
- Maskable interrupt sources provided via individual and combined interrupt lines
- One absolute timer
- One timer that can be configured as absolute or relative
- Nexus data trace support

1.6.23 System Timer Module (STM)

The system timer module (STM) is a 32-bit timer designed to support commonly required operating system and application software timing functions. The STM includes a 32-bit up counter and four 32-bit compare channels with a separate interrupt source for each channel.

The following features are implemented:

- One 32-bit up counter with 8-bit prescaler
- Four 32-bit compare channels
- Independent interrupt source for each channel
- Counter can be stopped in debug mode

1.6.24 Software Watchdog Timer (SWT)

The software watchdog timer (SWT) is a second watchdog module to complement the standard Power Architecture watchdog integrated in the CPU core. When enabled, the SWT requires periodic execution of a watchdog servicing sequence. Writing the sequence resets the timer to a specified time-out period. If this servicing action does not occur before the timer expires the SWT generates an interrupt or hardware reset. The SWT can be configured to generate a reset or interrupt on an initial time-out, a reset is always generated on a second consecutive time-out.

The following features are implemented:

- 32-bit time-out register to set the time-out period
- Programmable selection of system or oscillator clock for timer operation
- Programmable selection of window mode or regular servicing
- Programmable selection of reset or interrupt on an initial time-out
- Master access protection
- Hard and soft configuration lock bits
- Reset configuration inputs allow timer to be enabled out of reset

1.6.25 Periodic Interrupt Timer (PIT)

The periodic interrupt timer (PIT) is an array of timers that can be used to generate interrupts and trigger DMA channels. It also provides a dedicated real-time interrupt timer (RTI), which runs on a separate clock and can be used for system wake-up.

The following features are implemented:

- Eight independent timer channels
- Each channel includes 32 bit wide down counter with automatic reload
- Seven channels clocked from system clock
- One channel clocked from crystal clock (wake-up timer)
- Wake-up timer remains active when system enters stop mode. Used to restart system clock after predefined time-out period
- Each channel can optionally generate interrupt request when timer reaches zero

- Channels can optionally produce trigger event when timer reaches zero (used to trigger eQADC queues)

1.6.26   Development Trigger Semaphore (DTS)

The DTS module provides semaphores and an identification register that can be used as part of a cooperative high speed triggered data acquisition protocol established between application software executing on the MPC5676R and an external tool.

The DTS includes the following features:

- A 32 bit semaphore register
- A 32 bit restricted access identification register that can be written by an external tool and read by application software

1.6.27   Self Test Control Unit (STCU)

The STCU provides a programming interface that allows software to initiate certain built in hardware self tests during execution of the application. The STCU includes the following features:

- A control register to configure and start the self test
- A status register to report the result of a self test
- An integrated watchdog timer to limit self test execution time

1.6.28   JTAG Controller (JTAGC)

The JTAG controller (JTAGC) block provides the means to test chip functionality and connectivity while remaining transparent to system logic when not in test mode. Testing is performed via a boundary scan technique, as defined in the IEEE 1149.1-2001 standard. All data input to and output from the JTAGC block is communicated in serial format. The JTAGC block is compliant with the IEEE 1149.1-2001 standard, and supports the following features:

- IEEE 1149.1-2001 Test Access Port (TAP) interface five pins (JCOMP, TDI, TMS, TCK, and TDO)
- A 5-bit instruction register that supports the following IEEE 1149.1-2001 defined instructions:
  — BYPASS, IDCODE, EXTEST, SAMPLE, SAMPLE/PRELOAD, HIGHZ, CLAMP
- A 5-bit instruction register that supports the additional following public instructions:
  — ACCESS_AUX_TAP_NPC, ACCESS_AUX_TAP_ONCE, ACCESS_AUX_TAP_eTPU, ACCESS_AUX_TAP_NXDM, ACCESS_AUX_TAP_NXDM_B, ACCESS_AUX_TAP_NXFR, ACCESS_AUX_TAP_ONCE_B, ACCESS_AUX_TAP_MULTI, ACCESS_CENSOR, ACCESS_AUX_TAP_eTPU_C
- Three test data registers: a bypass register, a boundary scan register, and a device identification register. The size of the boundary scan register is parameterized to support a variety of boundary scan chain lengths.
- A TAP controller state machine that controls the operation of the data registers, instruction register and associated circuitry.

- Censorship inhibit register
  — 64-bit censorship password register
  — If the external tool writes a 64-bit password that matches the serial boot password stored in the internal flash shadow block, censorship is disabled until the next JTAG reset

1.6.29 Nexus

The Nexus debug interface (NDI) block provides real-time development support capabilities for the MPC5676R in compliance with the IEEE-ISTO 5001-2010 standard. This development support is supplied for MCUs without requiring external address and data pins for internal visibility. The NDI block is an integration of several individual Nexus blocks that are selected to provide the development support interface for the MPC5676R. The NDI block interfaces to the host processors, the eTPUs, and internal buses to provide development support as per the IEEE-ISTO 5001-2003 standard. The development support provided includes program trace, data trace, watchpoint trace, ownership trace, run-time access to the MCU's internal memory map and access to the Power Architecture and eTPU internal registers during halt. The Nexus interface also supports a JTAG-only mode using only the JTAG pins. Nexus also provides data trace support for FlexRay and both eDMA2s. The following features are implemented:

- 23 or 27 full duplex pin interface for medium and high visibility throughput
  — One of two modes selected by register configuration: reduced port mode (RPM) and full port mode (FPM). RPM comprises 12 MDO (message data out) pins and FPM comprises 16 MDO pins
  — Auxiliary output port
- Debug support pins
  — 1 MCKO (message clock out) pin
  — 12 or 16 MDO (message data out) pins
  — 2 $\overline{\text{MSEO}}$ (message start/end out) pins
  — 1 $\overline{\text{RDY}}$ (ready) pin
  — 1 $\overline{\text{EVTO}}$ (event out) pin
    – Auxiliary input port
  — 1 $\overline{\text{EVTI}}$ (event in) pin
  — 5-pin JTAG port (JCOMP, TDI, TDO, TMS, and TCK)
- Host processors (e200z7) standard class 3 (IEEE-ISTO 5001-2010) compliant
- eTPUs development support standard class 3 (IEEE-ISTO 5001-2003) compliant
- Supports data trace for the FlexRay controller and both eDMA2 modules with IEEE-ISTO 5001-2003 compliant messages
- Run-time access to the on-chip memory map via the Nexus read/write access protocol
- All features are independently configurable and controllable via the IEEE 1149.1 I/O port
- The NDI block reset is controlled with JCOMP, power-on reset, and the TAP state machine. All these sources are independent of system reset.
- Hardware support for triggered semaphore based data acquisition via an external tool.

- Power-on-reset status indication during reset via MDO[0] in disabled and reset modes

1.6.30   Power Management Unit (PMU)

The MPC5676R's power management unit includes the following features:

- Internally the chip has four supply voltages, nominally 5V, 3.3V, 1.2V and V_{stby}
- An external 5V supply is required. The 3.3V may be supplied by an on-chip regulator powered from the 5V supply
    - Optionally, an external 3.3V supply may replace the on-chip 3.3V regulator
- An on-chip 1.2V regulator controller via either an external bipolar pass transistor (for linear regulation) or an NMOS FET with external inductor switch-mode regulator power
- Option to power on-chip standby RAM from a wide range of external power supply voltages
- All supply voltages have voltage monitors and both the 1.2V regulator and all monitors except Vstby are adjustable
- On chip POR to ensure execution does not occur outside the device operating voltage limits

2   Developer Environment

The MPC5676R supports similar tools and third party developers as other Freescale MPC5500 products, offering a widespread, established network of tools and software vendors. It also features a high-performance Nexus debug interface.

The following development support will be available.

- Automotive evaluation boards (EVB) featuring CAN, LIN interfaces, and more
- Compilers
- Debuggers
- JTAG and Nexus interfaces
- RAppID™ Initialization tool
- OSEK solutions will be available from multiple third parties
- FlexRay, CAN and LIN drivers
- AUTOSAR package including OS, MCAL, and communication drivers

3 Revision History

Table 2. Revision History of this document

Version	Description
1	Initial release. Freescale Confidential Proprietary, NDA Required.
2	Removed Freescale Confidential footer. Changed Calibration Bus entry in the "MPC5500 and MPC5600 Family Comparison" table to be "16 bit non-mux; 16, 32 bit muxed" for MPC5676R.

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