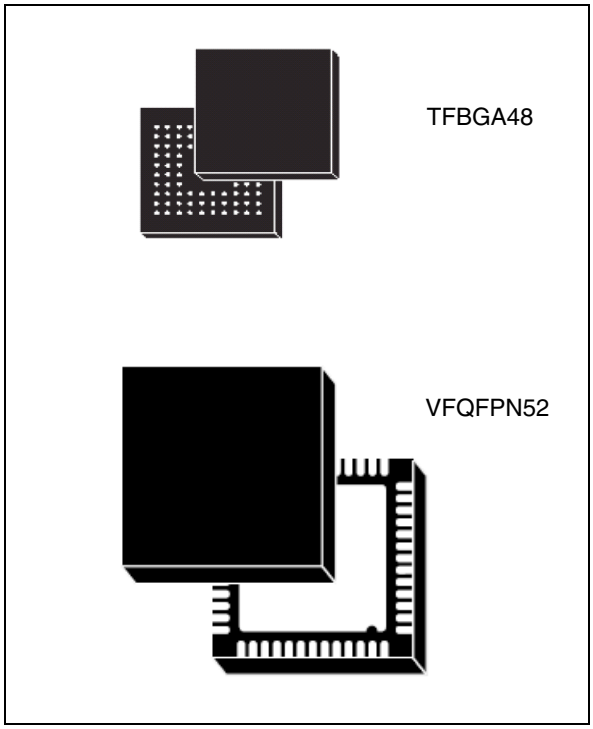
STA529

FFX™ audio codec with analog and digital inputs and 2 x 1.2 W (or 2 x 100 mW HP) class-D amplifier

Datasheet – production data

Features

- Up to 96 dB dynamic range
- Sample rates from 8 kHz to 192 kHz
- FFX™ class-D driver
- 1.55 V to 1.95 V digital power supply
- 1.80 V to 3.60 V analog and I/O power supply
- 18-bit audio processing and class-D FFX™ modulator
- >90-dB SNR analog-to-digital converter
- Digital volume control:
  - +36 dB to -105 dB in 0.5-dB steps
  - Software volume update
- 16-bit ADC
- Individual channel and master gain/attenuation
- Automatic invalid input detect mute
- 2-channel I^2S input/output data interface
- Digitally controlled pop-free operation
- 90% efficiency
- Output power for stereo headphones or stereo speakers applications (at THD = 10% and V_{CC} = 3.3 V):
  - 45 mW with 32-Ω headphones
  - 85 mW with 16-Ω headphones
  - 720 mW with 8-Ω speakers
  - 1.1 W with 4-Ω speakers



Applications

- Portable devices
  - Laptops
  - Digital cameras
  - Microless applications

Table 1. Device summary

Order code	Operating temp. range	Package	Packaging
STA529Q	-40 to 85 °C	VFQFPN52	Tray
STA529	-40 to 85 °C	TFBGA48	Tray

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1 Description

The STA529 is a digital stereo class-D audio amplifier. It includes an audio DSP, an ST proprietary high-efficiency class-D driver and CMOS power output stage. It is intended for high-efficiency digital-to-power-audio conversion for portable applications. The STA529 also provides output capabilities for FFX™. In conjunction with a power device, the STA529 provides high-quality digital amplification.

The STA529 contains an on-chip volume/gain control.

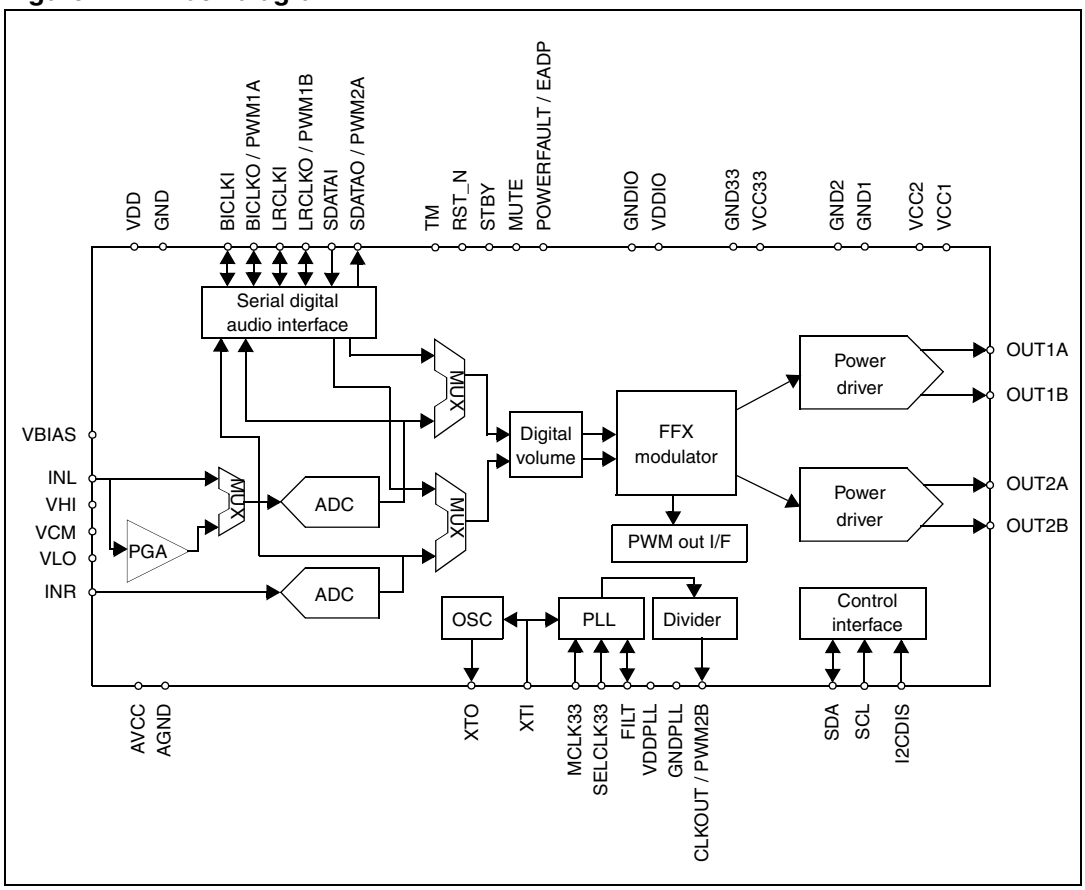
The PWM amplifier achieves greater than 90% efficiency for longer battery life for portable systems.

The innovative class-D modulation, allows the STA529 to work without external LC filters and without a heatsink.

The STA529 I2CDIS pin disables the audio DSP functions and the I^2C interface provides a direct conversion of the input signal into output power. This conversion is done without the microcontroller.

The STA529 is designed for low-power operation with extremely low-current consumption in standby mode. It is available in packages TFBGA48 and VFQFPN52. These are very thin packages (1.2 mm thick) ideal for small portable applications.

Figure 1. Block diagram



2 Connection diagrams and pin descriptions

This section includes connection diagrams and pin descriptions for the following packages:

- TFBGA48
- VFQFPN52

2.1 TFBGA48 package

Figure 2. Connection diagram for TFBGA48 (bottom view)

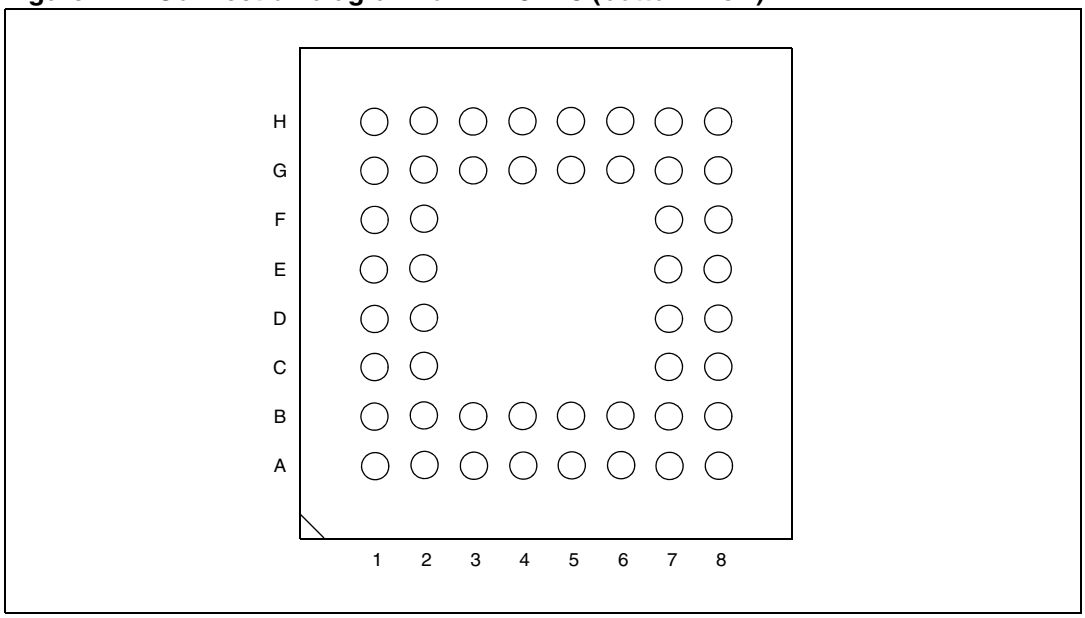


Table 2. Pin description for TFBGA48

Pin	Name	Type	Description
A1	VCC2	Supply	Channel 2 power supply
A2	GND2	Ground	Channel 2 power ground
A3	OUT2A	Analog output	Channel 2 half-bridge A output
A4	OUT2B	Analog output	Channel 2 half-bridge B output
A5	OUT1B	Analog output	Channel 1 half-bridge B output
A6	OUT1A	Analog output	Channel 1 half-bridge A output
A7	GND1	Ground	Channel 1 power ground
A8	VCC1	Supply	Channel 1 power supply
B1	GNDIO	Ground	I/O ring ground
B2	GND33	Ground	Pre-driver ground
B3	OUT2A	Analog output	Channel 2 half-bridge A output
B4	OUT2B	Analog output	Channel 2 half-bridge B output

Table 2. Pin description for TFBGA48 (continued)

Pin	Name	Type	Description
B5	OUT1B	Analog output	Channel 1 half-bridge B output
B6	OUT1A	Analog output	Channel 1 half-bridge A output
B7	MUTE	Digital input	Mute (active high)
B8	GND	Ground	Digital ground
C1	VDDIO	Supply	I/O ring supply
C2	VCC33	Supply	Pre-driver supply
C7	CLKOUT / PWM2B	Digital output	Buffered clock output / PWM2B FFX
C8	VDD	Supply	Digital supply
D1	XTI	Digital input 1.8V	Crystal input or master clock input
D2	XTO	Digital output 1.8V	Crystal output
D7	RST_N	Digital input	Reset (active low)
D8	VCM	Analog I/O	ADC common mode voltage
E1	MCLK33	Digital input	Master clock input 3.3-V capable
E2	SDATAI	Digital input	Input serial audio interface data
E7	VLO	Analog input	ADC low reference voltage
E8	AGND	Ground	ADC analog ground
F1	SCL	Digital input	I^2C serial clock
F2	POWERFAULT / EAPD	Digital output	Power fault signal (active high) / external audio power-down signal
F7	VHI	Analog input	ADC high reference voltage
F8	AVDD	Supply	ADC analog supply
G1	SDA	Digital I/O	I^2C serial data
G2	I2CDIS	Digital input	I^2C disable pin (active high)
G3	SELCLK33	Digital input	Master clock input selector: 0: XTI selected 1: MCLK33 selected
G4	SDATAO / PWM2A	Digital output	Output serial audio interface data / PWM2A FFX
G5	LRCLKO / PWM1B	Digital I/O	Output serial audio interface L/R-clock (volume increases when I2CDIS = 1) / PWM1B FFX
G6	BICLKO / PWM1A	Digital I/O	Output serial audio interface bit-clock (volume decreases when I2CDIS = 1) / PWM1A FFX
G7	VBIAS	Analog I/O	ADC microphone bias voltage
G8	STBY	Digital input	Standby (active high)
H1	FILT	Analog I/O	PLL loop filter terminal

Table 2. Pin description for TFBGA48 (continued)

Pin	Name	Type	Description
H2	TM	Digital input	Test mode (active high)
H3	GNDPLL	Ground	PLL analog ground
H4	VDDPLL	Supply	PLL analog supply
H5	LRCLKI	Digital I/O	Input serial audio interface L/R-clock
H6	BICLKI	Digital I/O	Input serial audio interface bit-clock
H7	INL	Analog input	ADC left channel line input or microphone input
H8	INR	Analog I/O	ADC right channel line input

2.2 VFQFPN52 package

Figure 3. Connection diagram for VFQFPN52 (bottom view)

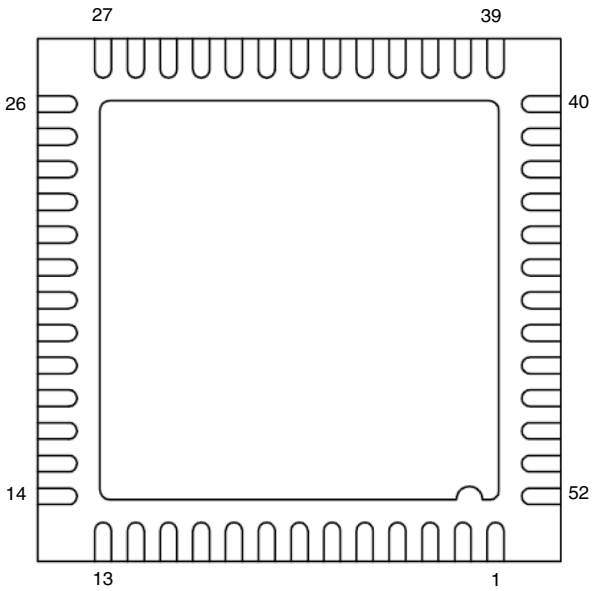


Table 3. Pin description for VFQFPN52

Pin	Name	Type	Description
1	STBY	Digital input	Standby (active high)
2	INL	Analog input	ADC left channel line input or microphone input
3	INR	Analog I/O	ADC right channel line input
4	VBIAS	Analog I/O	ADC microphone bias voltage
5	AVDD	Supply	ADC analog supply
6	VHI	Analog input	ADC high reference voltage
7	VLO	Analog input	ADC low reference voltage

Table 3. Pin description for VFQFPN52 (continued)

Pin	Name	Type	Description
8	AGND	Ground	ADC analog ground
9	VCM	Analog I/O	ADC Common mode voltage
10	RST_N	Digital input	Reset (active low)
11	CLKOUT / PWM2B	Digital output	Buffered clock output / PWM2B FFX
12	GND1	Ground	Digital ground
13	VDD1	Supply	Digital supply
14	MUTE	Digital input	Mute (active high)
15	VCC1A	Supply	Channel 1 half-bridge A power supply
16	OUT1A	Analog output	Channel 1 half-bridge A output
17	GND1A	Ground	Channel 1 half-bridge A power ground
18	GND1B	Ground	Channel 1 half-bridge B power ground
19	OUT1B	Analog output	Channel 1 half-bridge B output
20	VCC1B	Supply	Channel 1 half-bridge B power supply
21	VCC2B	Supply	Channel 2 half-bridge B power supply
22	OUT2B	Analog output	Channel 2 half-bridge B output
23	GND2B	Ground	Channel 2 half-bridge B power ground
24	GND2A	Ground	Channel 2 half-bridge A power ground
25	OUT2A	Analog output	Channel 2 half-bridge A output
26	VCC2A	Supply	Channel 2 half-bridge A power supply
27	GND33	Ground	Pre-driver ground
28	GNDIO1	Ground	I/O ring ground
29	VDDIO1	Supply	I/O ring supply
30	VCC33	Supply	Pre-driver supply
31	POWERFAULT / EAPD	Digital output	Power fault signal (active high) / external audio power down signal
32	TM	Digital input	Test mode (active high)
33	I2CDIS	Digital input	I^2C disable pin (active high)
34	SCL	Digital input	I^2C serial clock
35	SDA	Digital I/O	I^2C serial data
36	SELCLK33	Digital input	Master clock input selector: 0: XTI selected 1: MCLK33 selected
37	MCLK33	Digital input	Master clock input 3.3-V capable
38	XTI	Digital input 1.8V	Crystal input or master clock input

Table 3. Pin description for VFQFPN52 (continued)

Pin	Name	Type	Description
39	XTO	Digital output 1.8V	Crystal output
40	FILT	Analog I/O	PLL loop filter terminal
41	GNDPLL	Ground	PLL analog ground
42	VDDPLL	Supply	PLL analog supply
43	GND2	Ground	Digital ground
44	VDD2	Supply	Digital supply
45	SDATAI	Digital input	Input serial audio interface data
46	SDATAO / PWM2A	Digital output	Output serial audio interface data / PWM2A FFX
47	LRCLKI	Digital I/O	Input serial audio interface L/R-clock
48	LRCLKO / PWM1B	Digital I/O	Output serial audio interface L/R-clock (volume increases when I2CDIS = 1) / PWM1B FFX
49	GNDIO2	Ground	I/O ring ground
50	VDDIO2	Supply	I/O ring supply
51	BICLKI	Digital I/O	Input serial audio interface bit-clock
52	BICLKO / PWM1A	Digital I/O	Output serial audio interface bit-clock (volume decreases when I2CDIS = 1) / PWM1A FFX

3 Electrical and thermal specifications

3.1 Thermal data

Table 4. Thermal data

Device	Parameter	Min	Typ	Max	Unit
TFBGA48	Thermal resistance junction to ambient	-	40	-	°C/W
VFQFPN52	Thermal resistance junction to ambient	-	22	-	°C/W

3.2 Absolute maximum ratings

Table 5. Absolute maximum ratings

Pin/symbol	Description	Min	Max	Unit
VDD VDD1 VDD2	Digital supply voltage	-0.5	+2.5	V
AVDD	ADC supply voltage	-0.5	+4	V
VDDPLL	PLL analog supply voltage	-0.5	+2.5	V
VCC1A VCC1B VCC2A VCC2B	Power stage supply voltage	-0.5	+4	V
VCC33	Pre-driver supply	-0.5	+4	V
VDDIO	Digital I/O supply	-0.5	+4	V
T_{STG}	Storage temperature	-40	150	°C
T_J	Junction temperature	-40	150	°C

Note: All grounds must be within 0.3 V of each other.

3.3 Recommended operating conditions

Table 6. Recommended operating conditions

Symbol	Parameter	Min	Typ	Max	Unit
VDD VDD1 VDD2	Digital supply voltage	1.55	1.80	1.95	V
AVDD	ADC supply voltage	1.8	3.3	3.6	V
VDDPLL	PLL analog supply voltage	1.55	1.80	1.95	V
VCC1A VCC1B VCC2A VCC2B	Power stage supply voltage	1.8	3.0	3.3	V
VCC33	Pre-driver supply (must be at same level as VCC1A/1B/2A/2B)	1.8	3.0	3.3	V
VDDIO	Power supply for I/Os	1.8	3.0	3.6	V
GND1, GND2, GND33	Channel 1 and 2 power ground, pre-driver ground	-	0	-	V
GNDIO	Ground for I/Os	-	0	-	V
V_{IH}	3.3-V supply	2.0	-	-	V
V_{IL}	3.3-V supply	-	-	0.8	V
V_{HYST}	Schmitt trigger hysteresis (VDDIO)	0.4	-	-	V
T_{AMB}	Ambient operating temperature	-40	-	85	^{o}C

3.4 Electrical characteristics

The electrical specifications in *Table 7* below are given for operation under the recommended conditions listed in *Table 6*. Unless otherwise specified, LRCLKI frequency (fs) = 48 kHz, input frequency = 1 kHz, and R_{LOAD} = 32 Ω.

Table 7. Electrical characteristics

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
Eff	Output power efficiency	-	-	90	-	%
R_{dson}	Output stage N/PMOS on-resistance	-	-	250	380	mΩ
IstbyL	Logic power supply current at standby	-	-	1.3	-	µA
IstbyP	Bridges power supply current in standby	-	-	0.7	-	µA
IddL	Logic power supply current at operating	-	-	15	-	mA
IddP	Bridges power supply current at operating	-	-	0.5	-	mA
Tds	Low current dead time (static)	-	-	1	-	ns
Tdd	High current dead time (dynamic)	-	-	2.5	-	ns
Tr	Rise time	-	-	3	-	ns
Tf	Fall time	-	-	3	-	ns
DNR	Dynamic range A-weighted	Speaker mode	-	96	-	dB
SNR	Signal-to-noise ratio (A-weighted)	Speaker mode	-	92	-	dB
THDN	Total harmonic distortion	0 dBFS input, 8 Ω speakers	-	0.1	-	%
		-6 dBFS input, 8 Ω speakers	-	0.05	-	%
		0 dBFS input, 32 Ω headphones	-	0.1	-	%
		-6 dBFS input, 32 Ω headphones	-	0.05	-	%

The following tables give the output power for 1% and 10% THD levels for headphones and speakers.

Table 8. Load power at 1% distortion in headphone mode

Load (Ω)	P (mW) at 1.8 V	P (mW) at 3.3 V
16	20	65
32	10	32

Table 9. Load power at 10% distortion in headphone mode

Load (Ω)	P (mW) at 1.8 V	P (mW) at 3.3 V
16	25	85
32	13	42

Table 10. Load power at 1% distortion in speaker mode

Load (Ω)	P (mW) at 1.8 V	P (mW) at 3.3 V
4	310	860
8	166	560
16	86	290
32	43	147

Table 11. Load power at 10% distortion in speaker mode

Load (Ω)	P (mW) at 1.8 V	P (mW) at 3.3 V
4	400	1100
8	216	720
16	112	380
32	57	200

3.5 Lock time

Table 12 gives the typical lock time of the PLL using the suggested loop filter with 1.8 V supply and 30 ^{o}C junction temperature.

Table 12. PLL lock time

Parameter	Value
Lock time	200 µs

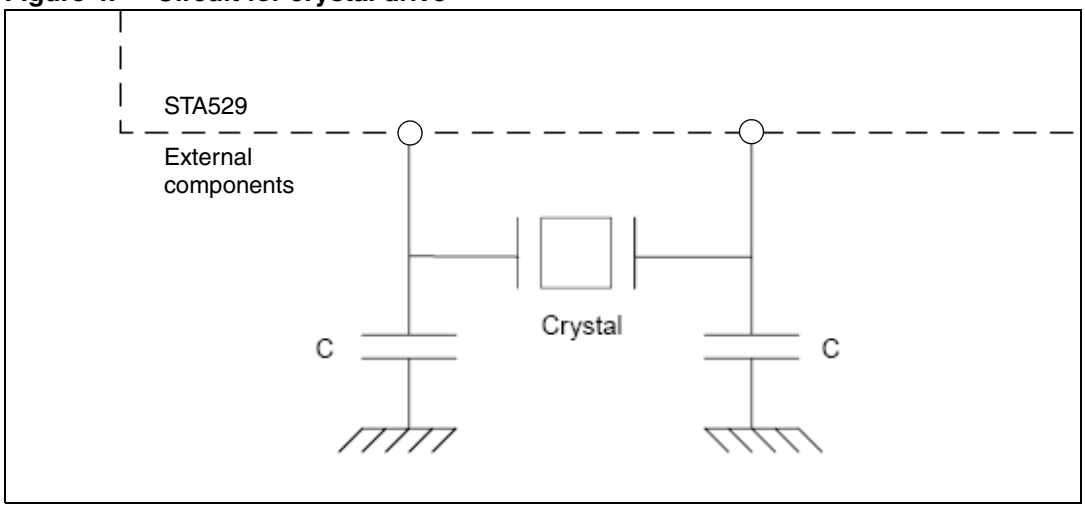
4 Input clock

4.1 SELCLK33

In STA529 the oversampling clock comes from MCLK33 or from pin XTI. The selection is done by applying the appropriate voltage to pin SELCLK33. If SELCLK33 is logical 1 then MCLK33 is selected, otherwise XTI is selected.

If an external crystal is used, SELCLK33 pin must be connected to GND and the suggested circuit shown below should be used.

Figure 4. Circuit for crystal drive



5 Digital processing

The STA529 processor block is a digital block providing two channels of audio processing and channel-mapping capability.

5.1 Signal processing flow

I^2S or stereo ADC data can be selected. The I^2S frequency range is 8 kHz to 192 kHz. The ADC sampling frequency can be selected between 8 kHz and 48 kHz.

5.2 I^2C interface disable

When pin I2CDIS = 1, the SDA, SCL, LRCLKO and BICLKO pins can be pulled high or low to change certain parameters of operation.

- SDA = 0: FFX input comes from ADC
  SDA = 1: FFX input comes from digital audio interface
- SCL = 0: binary output mode (binary soft start/stop enabled)
  SCL = 1: phase shift output mode
- LRCLKO = 0: no volume change
  LRCLKO = 1: channel volume up on both channel
- BICLKO = 0: no volume change
  BICLKO = 1: channel volume down on both xchannel.

At power up, the channel volume is set to -60 dB. When holding pin LRCLKO = 1 and pin BICLKO = 1 simultaneously, the channel volume is set to 0 dB. A high pulse on pin LRCLKO causes a channel volume change of +0.5 dB and a high pulse on pin BICLKO causes a channel volume change of -0.5 dB.

5.3 Volume control and gain

The volume control structure of the STA529 consists of individual volume registers for each channel and a master volume register that provides an offset to each channel's volume setting. The individual channel volumes are adjustable in 0.5-dB steps from +36 dB to -91.5 dB. As an example, if register LVOL = 0x00 or +36 dB and register MVOL = 0x18 or -12 dB, then the total gain for the left channel is +24 dB.

When the mute bit is set to 1, all channels are muted. The volume control provides a soft mute with the volume ramping down to mute in 4096 samples from the maximum volume setting at the internal processing rate (around 48 kHz).

Table 13. Master volume offset as a function of register MVOL

MVOL[7:0]	Volume offset from channel value
0x00	0 dB
0x01	-0.5 dB
0x02	-1dB
…	…
0x78	-60 dB
…	…
0xFE	-105 dB
0xFF	Hard master mute

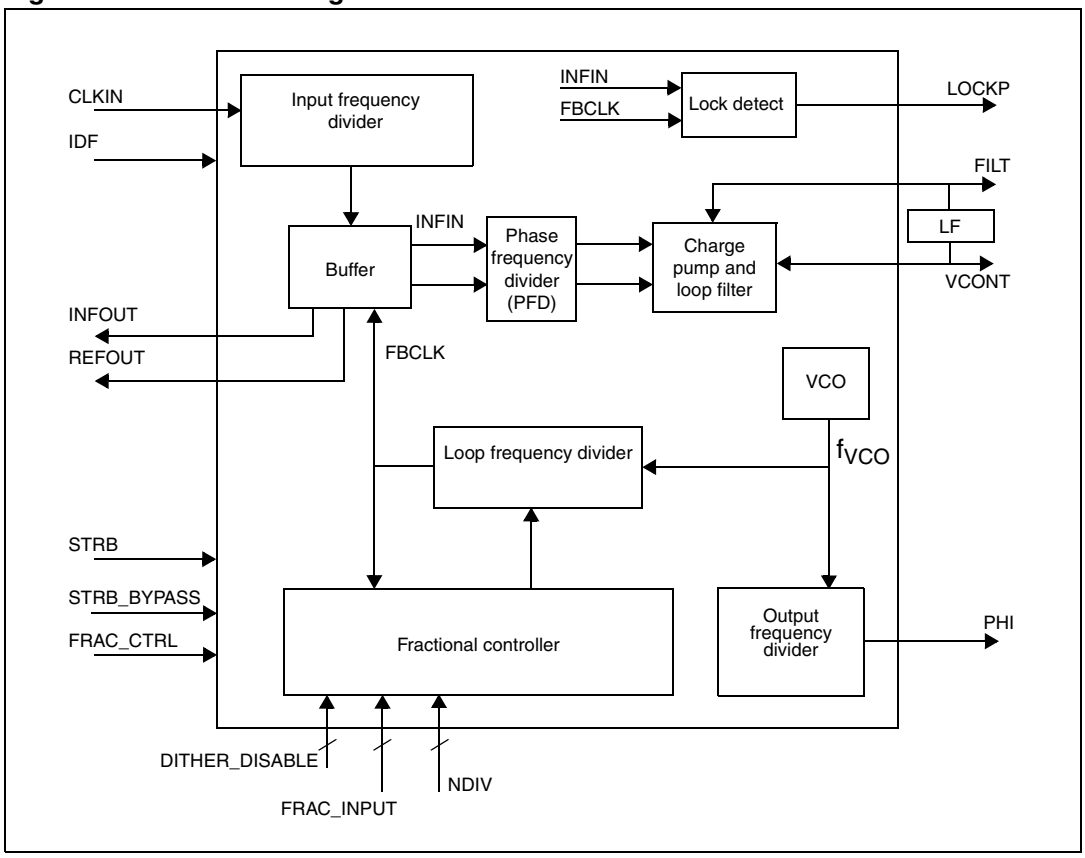
Table 14. Channel volume as a function of registers LVOL and RVOL

LVOL/RVOL[7:0]	Volume
0x00	+36 dB
0x01	+35.5 dB
0x02	+35 dB
…	…
0x47	+0.5 dB
0x48	0 dB
0x49	-0.5 dB
…	…
…	…
0xFF	-91.5 dB

6 PLL

Figure 5 shows the main components of the PLL.

Figure 5. PLL block diagram



6.1 Functional description

Phase/frequency detector

The phase/frequency detector (PFD) compares the phase difference between the corresponding rising edges of INFIN and FBCLK, (clock output from the loop frequency divider) by generating voltage pulses with widths proportional to the input phase error.

Charge pump and loop filter

This block converts the voltage pulses from the phase/frequency detector to current pulses which charge the loop filter and generate the control voltage for the voltage-controlled oscillator. The loop filter is placed external to the PLL on pin FILT.

Voltage controlled oscillator

The voltage controlled oscillator (VCO) is the oscillator inside the PLL. It produces a frequency (f_{VCO}) proportional to the input control voltage.

Input frequency divider

This frequency divider divides the PLL input clock CLKIN by a factor called the input division factor (IDF) to generate the PFD input frequency INFIN.

Loop frequency divider

This frequency divider is present within the PLL for dividing f_{VCO} by a factor called the loop division factor (LDF). The output of this block is clock FBCLK.

Output frequency divider

The output frequency divider divides f_{VCO} by the output division factor (ODF) to produce the output clock PHI and the clock to the core. In the STA529, ODF = 2 and cannot be reconfigured.

Lock-detect circuit

The output of this block (signal LOCKP) is asserted high when the PLL enters the state of Coarse Lock in which the output frequency is within ±10%, approximately, of the desired frequency. LOCKP is refreshed every 32 cycles of clock INFIN. The generated value is based on the result of comparing the number of FBCLK cycles in a window of 14 INFIN cycles. The different cases generated after comparison are as follows.

- If LOCKP is already at 0, then in the next refresh cycle LOCKP goes to 1 if the number of FBCLK cycles in the 14-cycle INFIN window is 13, 14, or 15. Otherwise LOCKP stays at 0.
- If LOCKP is already at 1, then in the next refresh cycle LOCKP goes to 0 if the number of FBCLK cycles in the 25-cycle INFIN window is less than 11 or higher than 17, otherwise LOCKP stays at 1.
- If LOCKP is already at 1 and CLKIN is lost (no longer present on the input pin), LOCKP stays at 1. In this case, the PLL is unlocked.

PLL filter

Figure 6 below shows the PLL filter circuit. Recommended values are R1 = 12.5 kΩ, C1 = 250 pF and C2 = 82 pF.

Figure 6. PLL filter circuit

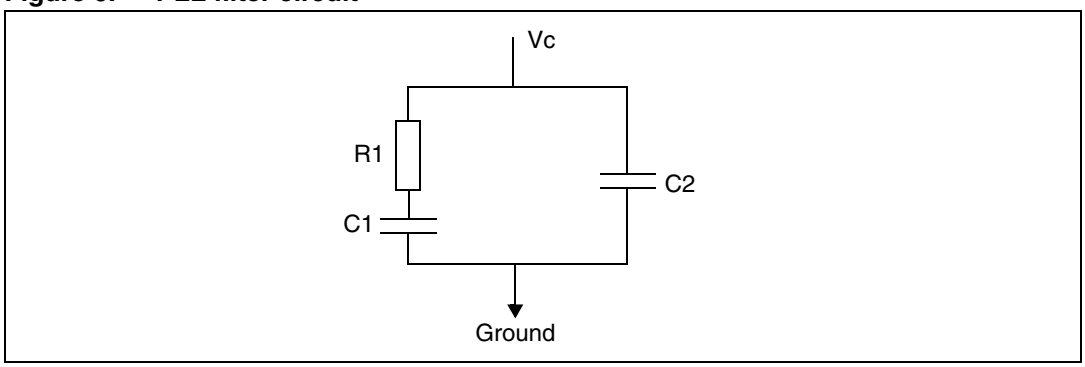


Table 12 on page 16 gives a typical lock time value for the PLL.

6.2 Configuration examples

The STA529 PLL can be configured in two ways:

- default startup configuration
- direct PLL programming

The default startup configuration reads the device defaults. With this configuration, it is not necessary to program the PLL dividers directly as preset values are used. In this mode, the oversampling ratio between pins XTI (or MCLK33) and LRCLKI is fixed to 256.

The direct PLL programming bypasses the automatic presets allowing direct programming of the PLL dividers.

The output PLL frequency can be determined by the following equations.

Output division factor:

$ODF = 2.$

Relation between input and output clock frequency:

$f_{INFIN} = f_{XTI} / IDF.$

If register bit PLLCFG0.FRAC_CTRL = 1

$f_{VCO} = f_{INFIN} * (LDF + FRACT / 2^{16} + 1 / 2^{17})$

$f_{PHI} = f_{VCO} / ODF.$

When register bit PLLCFG0.DITHER_DISABLE[1] = 1, the $1/2^{17}$ factor is not in the multiplication. This is recommended in order to keep register bit PLLCFG0.DITHER_DISABLE[1] = 0, otherwise there can be spurious signals in the output clock spectrum.

If register bit PLLCFG0.FRAC_CTRL = 0, then:

$f_{VCO} = f_{INFIN} * LDF$

$f_{PHI} = f_{VCO} / ODF.$

In the above equations:

FRACT = decimal equivalent of register bit PLLCFG1.FRAC_INPUT[15:0]

IDF = input division factor

LDF = loop division factor

ODF = output division factor = 2

f_{INFIN} = INFIN frequency

f_{XTI} = XTI frequency

f_{VCO} = VCO frequency

f_{PHI} = frequency of the PLL output clock.

When selecting the values for IDF, LDF and FRACT, ensure that the following limits are maintained:

$2.048\ MHz < f_{XTI} < 49.152\ MHz$

$2.048\ MHz < f_{INFIN} < 16.384\ MHz$

$65.536\ MHz < f_{VCO} < 98.304\ MHz$

There are also some additional constraints on IDF and LDF. IDF should be greater than 0, LDF should be greater than 5 if FRAC_CTRL = 0 and greater than 8 if FRAC_CTRL = 1.

When automatic settings are not used, the PLL must be configured to generate an internal frequency, f_{PHI}, of N * fs, where fs is the frequency of pin LRCLKI. Values for N are given in *Table 15*.

Table 15. Oversampling table

fs (kHz)	N	f_{PHI} (MHz)
8	4096	32.768
11.025	4096	45.1584
12	4096	49.152
16	2048	32.768
22.05	2048	45.1584
24	2048	49.152
32	1024	32.768
44.1	1024	45.1584
48	1024	49.152
64	512	32.768
88.2	512	45.1584
96	512	49.152
128	256	32.768
176.4	256	45.1584
192	256	49.152

Example 1

f_{XTI} = 13 MHz and fs = 44.1 kHz

IDF should be equal to 3 otherwise LDF becomes less than 8 (FRAC_CTRL must be 1):

LDF = floor(45.1584 / (13 / IDF)) = 10

FRACT = round([(45.1584 / (13 / IDF)) - floor(45.1584 / (13 / IDF))] * 2^{16}) = 27602.

where:

floor means rounded down and
round means rounded to nearest integer.

Using the above configuration, the system clock is 45.15841675 MHz, the approximate static error is 16 Hz (that is, 0.5 ppm).

Example 2

f_{XTI} = 19.2 MHz and fs = 48 kHz

IDF should be equal to 4 otherwise LDF become less than 8 (FRAC_CTRL must be 1):

LDF = floor(49.152 / (19.2 / IDF)) = 10

FRACT = round([(49.152 / (19.2 / IDF)) - floor(49.152 / (19.2 / IDF))] * 2^{16}) = 15728.

Using the above configuration, the system clock is 49.151953125 MHz, the approximate static error is 47 Hz (that is, 1 ppm).

6.3 Set fractional PLL

The following procedure is mandatory to configure the fractional PLL:

1. Set bit D7 reg 0x18 (PLL_BYP_UNL) to "1"
2. Write reg 0x17 (PLLCFG3)
3. Write reg 0x14 (PLLCFG0)
4. Write reg 0x15 (PLLCFG1)
5. Write reg 0x16 (PLLCFG2)
6. Set bit D7 reg 0x18 (PLL_BYP_UNL) to "0"

7 ADC

7.1 ADC performance values

Table 16. Programmable gain performance

Parameter	Min	Typ	Max	Unit
Dynamic range 1 kHz, A-weighted (3.3 V supply)		92		dB
Dynamic range 1 kHz, A-weighted (1.8 V supply)		84		dB
SNDR 1 kHz, A-weighted (3.3 V supply)		92		dB
SNDR 1 kHz, A-weighted (1.8 V supply)		84		dB
THD 1 kHz (-1 dB input) (3.3 V supply)		-85		dB
THD 1 kHz (-1 dB input) (1.8 V supply)		-75		dB
Cross talk (3.3 V supply)		-80		dB
Cross talk (1.8 V supply)		-60		dB

7.2 Functional description

The STA529 analog input is provided through a low-power, low-voltage, 16-bit stereo audio analog-to-digital converter front end designed for audio applications. It includes a programmable gain amplifier, anti-aliasing filter, low-noise microphone biasing circuit, third-order MASH2-1 delta-sigma modulator, digital decimating filter and a first-order DC-removal filter.

The ADC works in the microphone input (mic-in) mode and in the line-input mode. If the line input mode is selected, the ADC is configured in stereo and all conversion channels are active.

If the microphone input mode is selected, the ADC is configured in mono. The mono channel is routed through the left conversion path, and the right conversion path is kept in power-down mode to minimize power consumption. A programmable gain amplifier (PGA) is available in mic-in mode, making it possible to amplify the signal from 0 to +42 dB in steps of 6 dB.

7.2.1 Digital filter characteristics

Table 17. Digital filter characteristics

Parameter	Typical	Unit
Pass band	0.4535 * fs	kHz
Pass-band ripple: Fs mode Fs_by_2 mode Fs_by_4 mode	 0.08 at 44.1 kHz 0.08 at 22.05 kHz 0.08 at 11.025 kHz	 dB dB dB
Stop-band attenuation: Fs mode Fs_by_2 mode Fs_by_4 mode	 45 at 44.1 kHz 45 at 22.05 kHz 45 at 11.025 kHz	 dB dB dB
Group delay: Fs mode Fs_by_2 mode Fs_by_4 mode	 0.4 at 32 kHz 0.7 at 16 kHz 1.4 at 8 kHz	 ms ms ms

7.2.2 High-pass filter characteristics

Table 18. High-pass filter characteristics

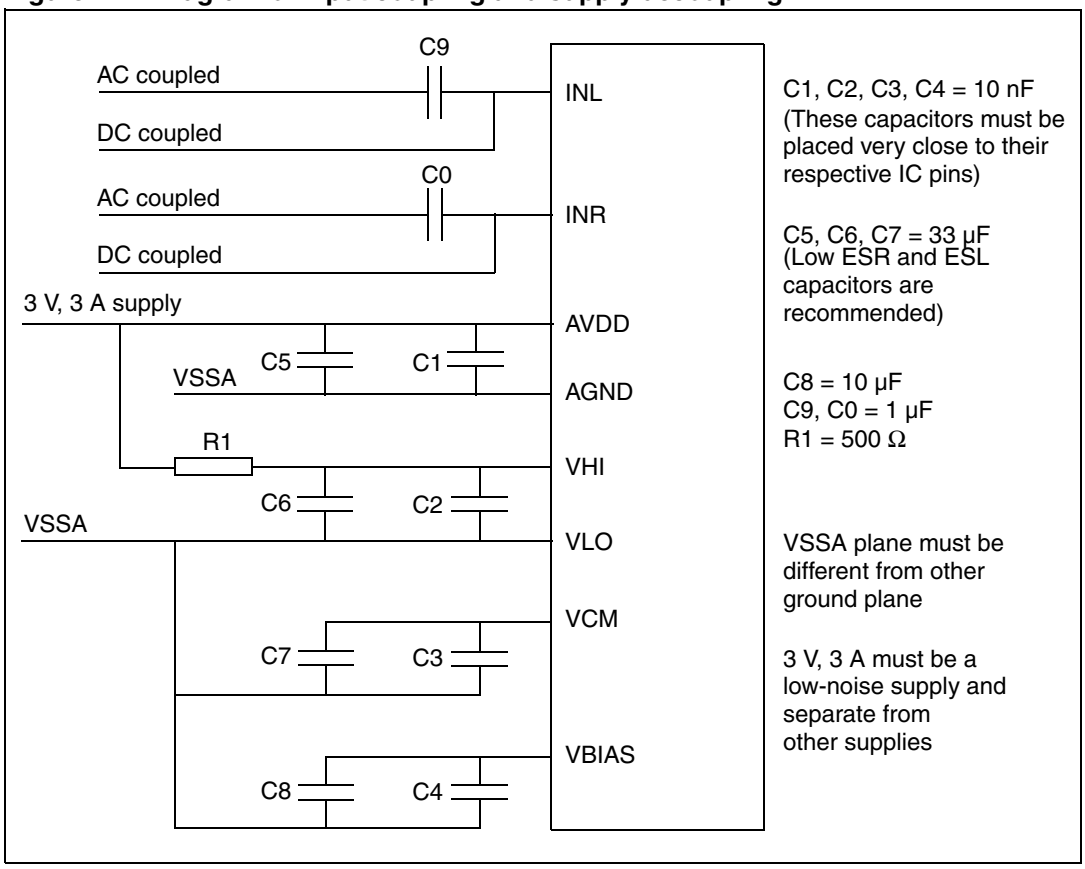
Parameter	Typical	Unit
Frequency response: -3 dB -0.08 dB	 7 50	 Hz Hz
Phase deviation at 20 Hz	19.35	degree
Passband ripple	0.08	dB

7.2.3 Programmable gain amplifier (PGA)

The PGA is available in mic-in mode only. The input signal can be amplified from 0 to 42 dB in 6-dB steps via bits PGA of register *ADCCFG on page 49*.

7.3 Applications scheme

Figure 7. Diagram of input coupling and supply decoupling



7.4 Configuration examples

The ADC sampling frequency can be selected from three values:

- normal (from 32 kHz to 48 kHz)
- low (from 16 kHz to 24 kHz)
- very-low (from 8 kHz to 12 kHz)

The setting is done through bits ADC_FS_RANGE of register *MISC on page 50*. For all other settings register *ADCCFG on page 49* is used.

8 Driver configuration

A driver configuration is available that allows PWM commands to be used on an external power device. For this purpose, the output serial audio interface is disabled and the respective pins have an alternative name and a new function, as shown in *Table 19*.

Table 19. Pin functions in driver-configuration mode

Pin	Alternative pin name and function
BICLKO	PWM1A (external bridge PWM command for output 1A)
LRCLKO	PWM1B (external bridge PWM command for output 1B)
SDATAO	PWM2A (external bridge PWM command for output 2A)
CLKOUT	PWM2B (external bridge PWM command for output 2B)
POWERFAULT	EADP (external audio power-down signal)

The driver configuration is selected with the two programmable registers, *PWMINT1* = 0x93 and *PWMINT2* = 0x81, *on page 51*.

8.1 I^2S bypass

A configuration is available which allows the passing of the I^2S input signal straight to the I^2S output signal.

This configuration is set using two programmable registers *PWMINT1* = 0x93 and *PWMINT2* = 0x80.

9 Serial audio interface

The serial-to-parallel interface and the parallel-to-serial interface can have different sampling rates.

The following terms are used in this section:

- **BICLK active edge:** Pins SDATAI, SDATAO, LRCLKI, LRCLKO always change synchronously with BITCLK active edges. The active edge can be configured as a rising or falling edge via register programming.
- **BICLK strobe edge:** Pins SDATAI, SDATAO, LRCLKI, LRCLKO should be stable near BICLK strobe edges, the slave device is able to use strobe edges to latch serial data internally.

9.1 Master mode

In this mode, pins BICLKI/BICLKO and pins LRCLKI/LRCLKO are configured as outputs.

Figure 8. Master mode

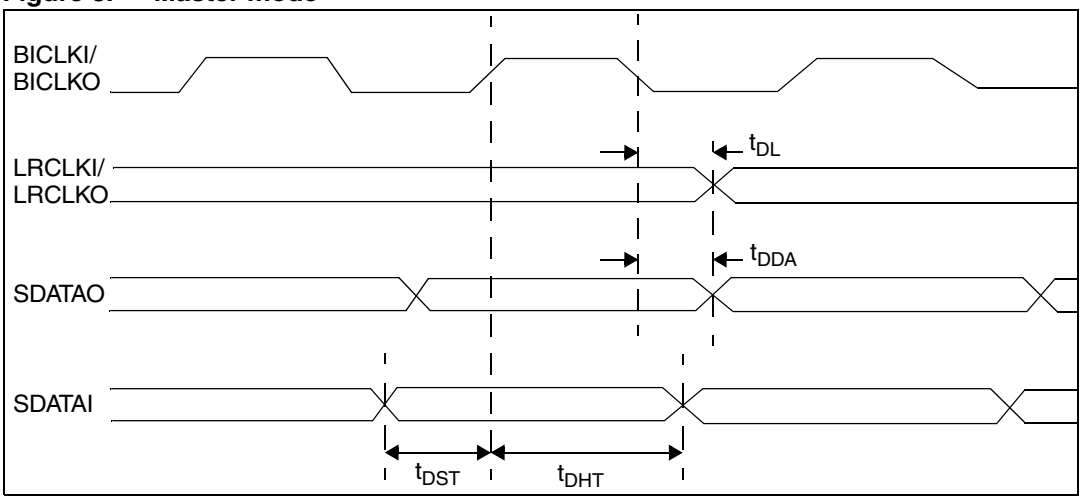


Table 20. Master mode

Symbol	Parameter	Min	Typ	Max	Unit
t_{DL}	LRCLKI/LRCLKO propagation delay from BICLK active edge	0		10	ns
t_{DDA}	SDATAO propagation delay from BICLKI/O active edge	0		15	ns
t_{DST}	SDATAI setup time to BICLKI/O strobing edge	10			ns
t_{DHT}	SDATAI hold time from BICLKI/O strobing edge	10			ns

9.2 Slave mode

In this mode, pins BICLKI/O and pins LRCLKI/O are configured as inputs.

Figure 9. Slave mode

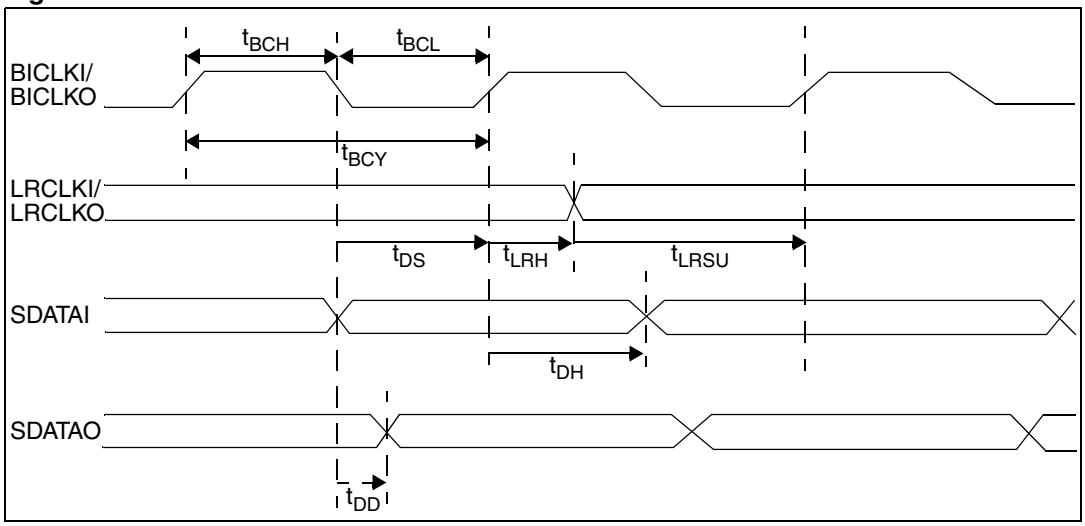


Table 21. Slave mode

Symbol	Parameter	Min	Typ	Max	Unit
t_{BCY}	BICLK cycle time	50			ns
t_{BCH}	BICLK pulse width high	20			ns
t_{BCL}	BICLK pulse width low	20			ns
t_{LRSU}	LRCLKI/LRCLKO setup time to BICLK strobing edge	10			ns
t_{LRH}	LRCLKI/LRCLKO hold time to BICLK strobing edge	10			ns
t_{DS}	SDATAO setup time to BICLK strobing edge	25			ns
t_{DH}	SDATAO hold time to BICLK strobing edge	25			ns
t_{DD}	SDATAI propagation delay from BICLK active edge	0		10	ns

9.3 Serial formats

Different audio formats are supported in both master and slave modes. Clock and data configurations can be customized to match most of the serial audio protocols available on the market.

Data length can be customized to 8, 16, 24 or 32 bits.

Figure 10. Right justified

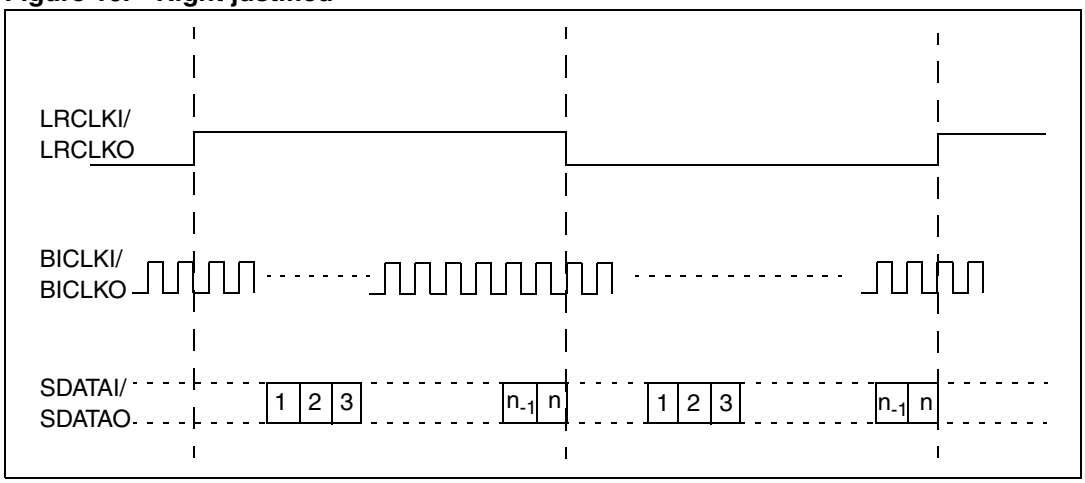
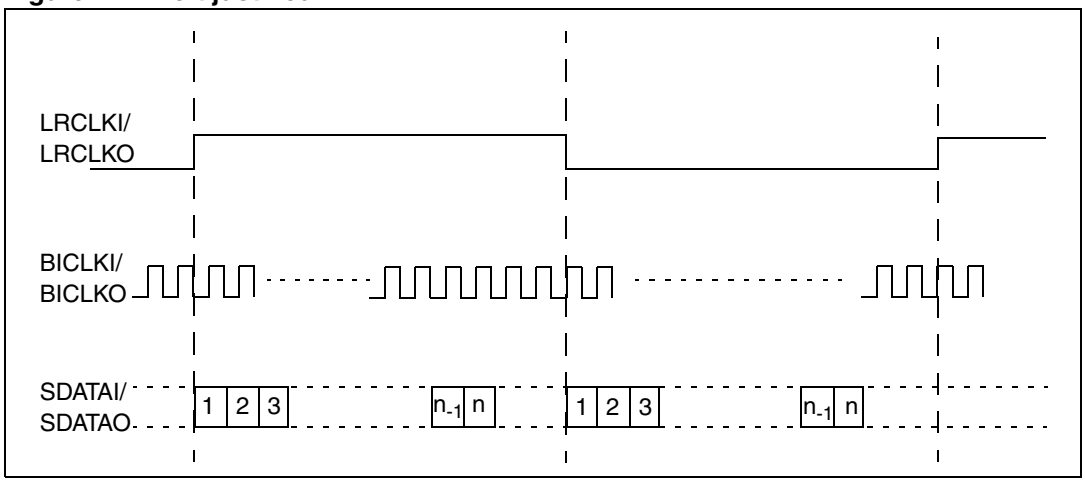
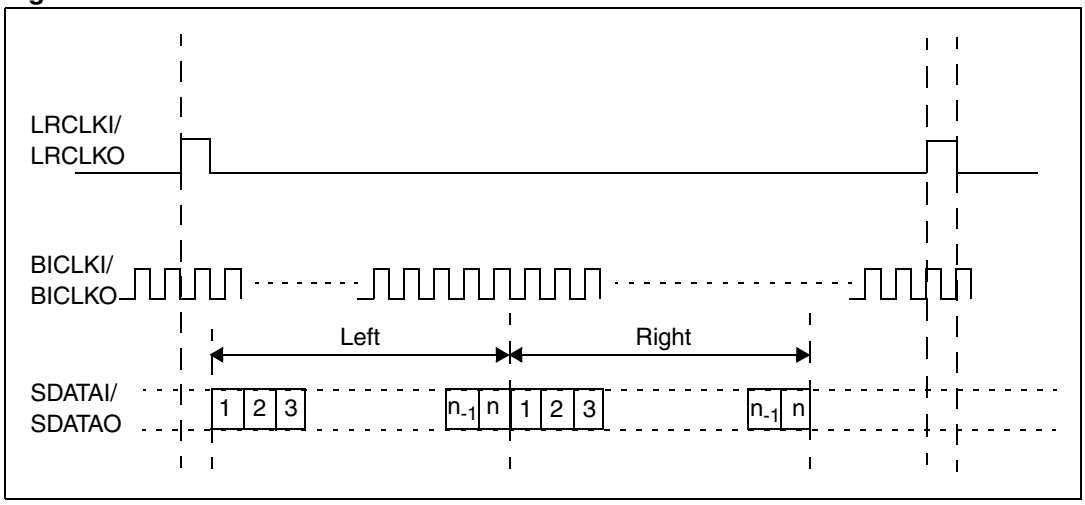


Figure 11. Left justified



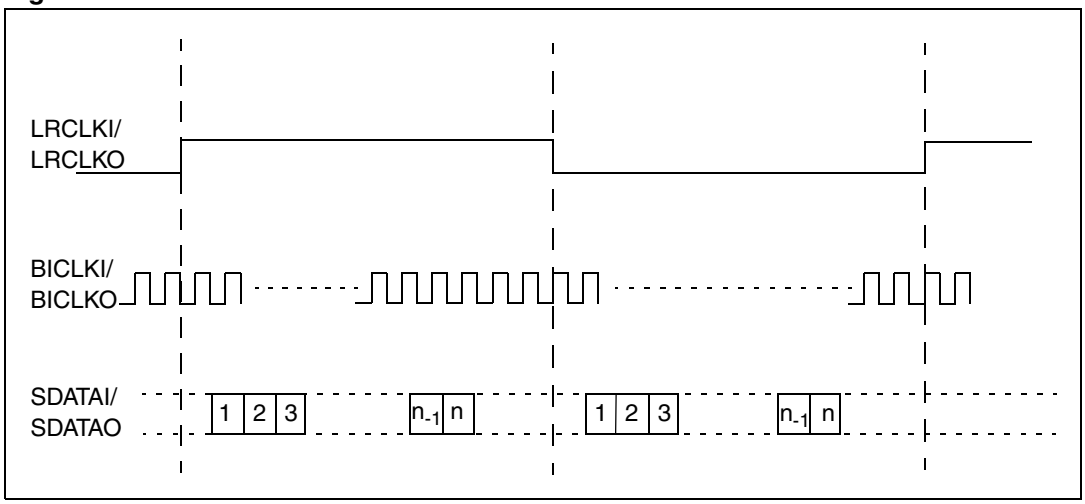
9.3.1 DSP

Figure 12. DSP



9.3.2 I²S

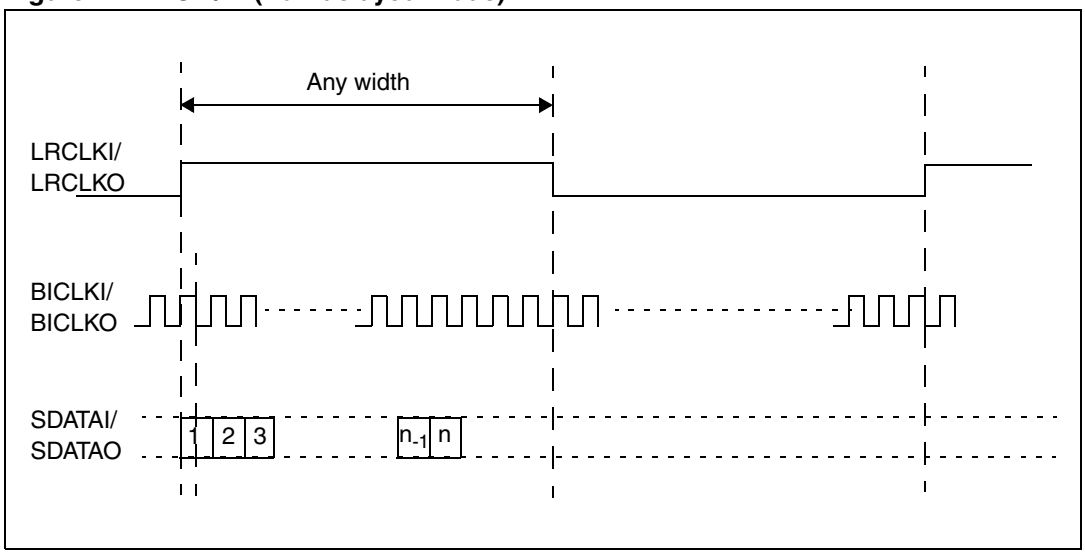
Figure 13. I²S



9.3.3 PCM/IF (non-delayed mode)

- MSB first
- 16-bit data

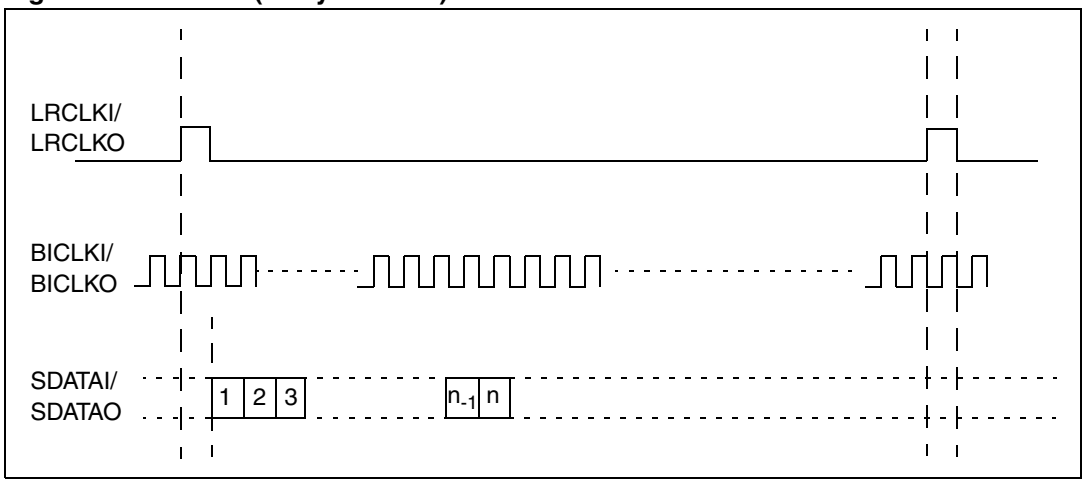
Figure 14. PCM/IF (non-delayed mode)



9.3.4 PCM/IF (delayed mode)

- MSB first
- 16-bit data

Figure 15. PCM/IF (delayed mode)



10 I²C interface

10.1 Data transition and change

Data changes on the SDA line must only occur when the SCL clock is low. SDA transition while the clock is high is used to identify a start or stop condition.

10.2 Start condition

A start condition is identified by a high to low transition of the data bus SDA signal while the clock signal SCL is stable in the high state. A start condition must precede any command for data transfer.

10.3 Stop condition

A stop condition is identified by low to high transition of the data bus SDA signal while the clock signal SCL is stable in the high state. A stop condition terminates communication between the STA529 and the master bus.

10.4 Data input

During data input, the STA529 samples the SDA signal on the rising edge of clock SCL. For correct device operation the SDA signal must be stable during the rising edge of the clock and the data can change only when the SCL line is low.

10.5 Device addressing

To start communication between the master and the STA529, the master must initiate with a start condition. Following this, the master sends 8 bits (MSB first) on the SDA line corresponding to the device select address and read or write mode.

The 7 most significant bits are the device address identifiers, corresponding to the I²C bus definition. In the STA529, the I²C interface has the device address 0x34.

The 8th bit (LSB) identifies the read or write operation (R/W). It is set to 1 in read mode and 0 in write mode.

After the start condition, the STA529 waits for its device address on SDA. When a match is found, it acknowledges the identification on SDA during the 9th bit time. The byte following the device identification byte is the internal space address.

10.6 Write operation

Following the start condition the master sends a device select code with the R/W bit set to 0. The STA529 acknowledges this and then writes to the byte of the internal address. After receiving the internal byte address, the STA529 responds with an acknowledgement.

10.6.1 Byte write

In the byte-write mode the master sends one data byte. This is acknowledged by the STA529. The master then terminates the transfer by generating a stop condition.

10.6.2 Multi-byte write

The multi-byte write modes can start from any internal address. The master generates a stop condition which terminates the transfer.

10.7 Read operation

10.7.1 Current address byte read

Following the start condition the master sends a device select code with bit R/W set to 1. The STA529 acknowledges this and then responds by sending one byte of data. The master then terminates the transfer by generating a stop condition.

10.7.2 Current address multi-byte read

The multi-byte read modes can start from any internal address. Sequential data bytes are read from sequential addresses within the STA529. The master acknowledges each data byte read and then generates a stop condition terminating the transfer.

10.7.3 Random address byte read

Following the start condition the master sends a device select code with bit R/W set to 0. The STA529 acknowledges this and then the master writes the internal address byte. After receiving the internal byte address, the STA529 again responds with an acknowledgement. The master then initiates another start condition and sends the device select code with bit R/W set to 1. The STA529 acknowledges this and then responds by sending one byte of data. The master then terminates the transfer by generating a stop condition.

10.7.4 Random address multi-byte read

The multi-byte read modes could start from any internal address. Sequential data bytes are read from sequential addresses within the STA529. The master acknowledges each data byte read and then generates a stop condition terminating the transfer.

Figure 16. I²C write operations

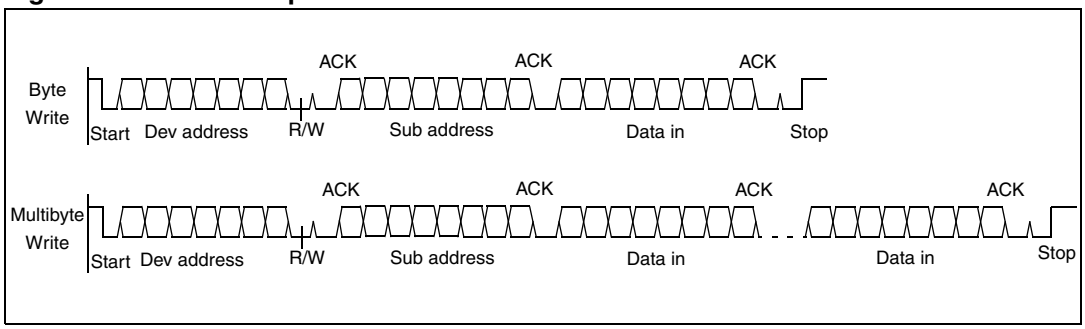
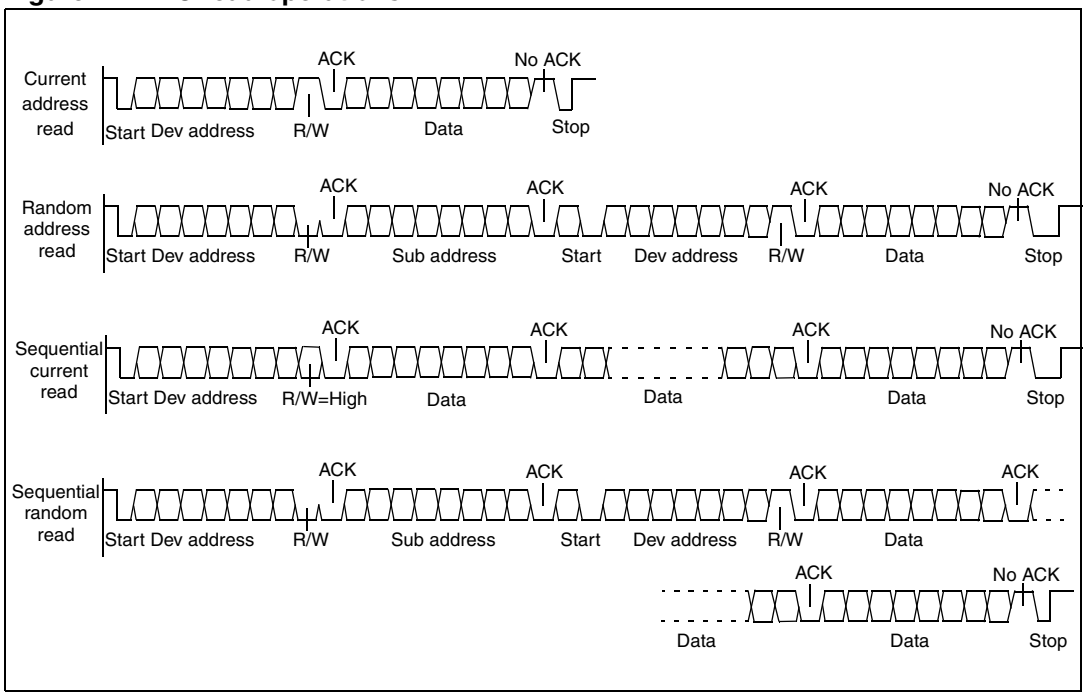


Figure 17. I²C read operations



11 Registers

This section describes the set-up register used in the device.

11.1 Summary

Table 22. Register summary

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x00	FFXCFG0	MUTE	POW_STBY	SOFT_ VOL_ON	BIN_SOFT START	TIM_SOFT_VOL[3:0]			
0x01	FFXCFG1	L1_R2	MUTE_ON_ INVALID	PWM_MODE[1:0]		PWM_SHIFT[1:0]		Reserved	
0x02	MVOL	SET_VOL_MASTER[7:0]							
0x03	LVOL	SET_VOL_LEFT[7:0]							
0x04	RVOL	SET_VOL_RIGHT[7:0]							
0x05	TTF0	TIM_TS_FAULT[15:8]							
0x06	TTF1	TIM_TS_FAULT[7:0]							
0x07	TTP0	TIM_TS_POWUP[15:8]							
0x08	TTP1	TIM_TS_POWUP[7:0]							
0x0A	S2PCFG0	BICLK_ STRB	LRCLK_ LEFT	SHARE_ BILR	MSB_FIRST	DATA_FORMAT[2:0]			MASTER_ MODE
0x0B	S2PCFG1	PDATA_LENGTH[1:0]		BICLK_OS[1:0]		MAP_L[1:0]		MAP_R[1:0]	
0x0C	P2SCFG0	BICLK_ STRB	LRCLK_ LEFT	SDATAO_ ACT	MSB_FIRST	DATA_FORMAT[2:0]			MASTER_ MODE
0x0D	P2SCFG1	PDATA_LENGTH[1:0]		BICLK_OS[1:0]		MAP_L[1:0]		MAP_R[1:0]	
0x14	PLLCFG0	PLL_DIREC T_PROG	FRAC_ CTRL	DITHER_DISABLE[1:0]		IDF[3:0]			
0x15	PLLCFG1	FRAC_INPUT[15:8]							
0x16	PLLCFG2	FRAC_INPUT[7:0]							
0x17	PLLCFG3	STRB	STRB_ BYPASS	NDIV[5:0]					
0x18	PLLPFE	PLL_ BYP_ UNL	BICLK2PLL	PLL_PWDN	PFE1A	PFE1B	PFE2A	PFE2B	RESET_ FAULT
0x19	PLLST	PLL_ UNLOCK	PLL_PWD_ STATE	PLL_BYP_ STATE	Reserved				
0x1E	ADCCFG	PGA[2:0]			INSEL	STBY	BYPASS_ CALIB	CLKENBL	Reserved
0x1F	CKOCFG	CLKOUT_ DIS	CLKOUT_SEL[1:0]		Reserved				
0x20	MISC	OSC_DIS	P2P_FS_RANGE[2:0]			ADC_FS_RANGE[1:0]		P2P_IN_ ADC	CORE_ CLKENBL
0x21	PADST0	Reserved							
0x22	PADST1	Reserved							

Table 22. Register summary (continued)

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0x23	FFXST	Reserved					INVALID_ INP_FBK	MUTE_ INT_FBK	Reserved
0x28	BISTRUN	Reserved							
0x29	BISTST0	Reserved							
0x2A	BISTST1	Reserved							
0x2B	BISTST2	Reserved							
0x2D	PWMINT1	PWM_INT[15:8]							
0x2E	PWMINT2	PWM_INT[7:0]							
0x32	POWST	POWER DOWN	POW_ TRISTATE	POW_ FAULT1A	POW_ FAULT1B	POW_ FAULT2A	POW_ FAULT2B	Reserved	

All other registers not mentioned here are reserved and must not be used.

11.2 General registers

FFXCFG0 FFX configuration

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
MUTE	POW_STBY	SOFT_VOL_ON	BIN_ SOFTSTART	TIM_SOFT_VOL[3:0]			

Address: 0x00

Type: R/W

Buffer: No

Reset: 0x75

Description:

7 MUTE:
0: standard operation (default)
1: FFX output is zero (muted condition)

6 POW_STBY:
0: FFX bridge is in power-up mode
1: FFX bridge is in standby mode (default)

5 SOFT_VOL_ON:
0: smooth transition not active
1: smooth transition when changing volume control (default)

4 BIN_SOFTSTART:
Reserved (1: default)

3:0 TIM_SOFT_VOL: volume control time step for any 0.5 dB volume change
Time is $(2^{TIM\_SOFT\_VOL}) * 20.83\ \mu s$
Default value: 0101. This value means 666.66 µs

FFXCFG1 Configuration

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
L1_R2	MUTE_ON_ INVALID	PWM_MODE[1:0]		PWM_SHIFT[1:0]		RES	RES

Address: 0x01

Type: R/W

Buffer: No

Reset: 0xF8

Description:

7 L1_R2: channel mapping:
0: right channel is mapped to output channel 1 and left channel is mapped to output channel 2
1: left channel is mapped to output channel 1 and right channel is mapped to output channel 2 (default)

6 MUTE_ON_ INVALID: mutes PWM outputs if invalid digital data is received:
0: outputs are not muted
1: outputs are muted (default)

5:4 PWM_MODE[1:0]:
00: binary (output B is opposite of output A)
01: binary headphones (output B is 50% duty cycle)
10: reserved, do not use
11: phase shift (default)

3:2 PWM_SHIFT[1:0]:
10: default
PWM period-shift between channels 1 and 2
Value is N * 90^{o}
Default is 180^{o}

1:0 Reserved (00: default)

MVOL Master volume control

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
SET_VOL_MASTER[7:0]							

Address: 0x02

Type: R/W

Buffer: No

Reset: 0x00

Description:

7:0 SET_VOL_MASTER[7:0]: master volume control:
From 0 dB to -127.5 dB in 0.5-dB steps
Default value (0x00) corresponds to 0 dB

LVOL Left channel volume control

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
SET_VOL_LEFT[7:0]							

Address: 0x03

Type: R/W

Buffer: No

Reset: 0x48

Description:

7:0 SET_VOL_LEFT[7:0]: left channel volume control:
Left channel volume control (from +36 dB to -91.5 dB in 0.5-dB steps)
Default value (0x48) corresponds to 0 dB

RVOL Right channel volume control

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
SET_VOL_RIGHT[7:0]							

Address: 0x04

Type: R/W

Buffer: No

Reset: 0x48

Description:

7:0 SET_VOL_RIGHT[7:0]: right channel volume control:
Right channel volume control (from +36 dB to -91.5 dB in 0.5-dB steps)
Default value (0x00) corresponds to 0 dB

TTF0 Tristate time after fault (MSBs)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TIM_TS_FAULT[15:8]							

Address: 0x05

Type: R/W

Buffer: No

Reset: 0x00

Description:

7:0 MSBs of TIM_TS_FAULT[15:0]:
See register *TTF1*.

TTF1 Tri-state time after fault (LSBs)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TIM_TS_FAULT[7:0]							

Address: 0x06

Type: R/W

Buffer: No

Reset: 0x02

Description:

7:0 LSBs of TIM_TS_FAULT[15:0]: time in which power is held in tristate mode after a fault signal:
Time is TIM_TS_FAULT * 83.33 µs.
Default value (0x0002) corresponds to 166.66 µs tristate time after fault

TTP0 Tri-state time after power-up (MSBs)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TIM_TS_POWUP[15:8]							

Address: 0x07

Type: R/W

Buffer: No

Reset: 0x00

Description:

7:0 MSBs of TIM_TS_POWUP[15:0]:
See register *TTP1* below.

TTP1 Tristate time after power-up (LSBs)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TIM_TS_POWUP[7:0]							

Address: 0x08

Type: R/W

Buffer: No

Reset: 0x02

Description:

7:0 LSBs of TIM_TS_POWUP[15:0]: time in which power is held in tri-state mode after a power-up signal:
Time is TIM_TS_POWUP * 83.33 µs
Default value (0x0002) corresponds to 166.66 µs tristate time after power-up

S2PCFG0 Serial to parallel audio interface configuration

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
BICLK_STRB	LRCLK_LEFT	SHARE_BILR	MSB_FIRST	DATA_FORMAT[2:0]			MASTER_ MODE

Address: 0x0A

Type: R/W

Buffer: No

Reset: 0xD2

Description:

7 BICLK_STRB:
0: bit clock strobe edge is falling edge, bit clock active edge is rising edge
1: bit clock strobe edge is rising edge, bit clock active edge is falling edge (default)

6 LRCLK_LEFT:
0: left/right clock is low for left channel, high for right channel
1: left/right clock is high for left channel, low for right channel (default)

5 SHARE_BILR:
0: default
1: left/right clock and bit clock are shared between serial to parallel interface and parallel to serial interface, BICLKI and LRCLKI are used

4 MSB_FIRST:
0: LSB first
1: MSB first (default)

3:1 DATA_FORMAT[2:0]: serial interface protocol format:
000: left Justified
001: I^2S (default)
010: right justified
100: PCM no delay
101: PCM delay
111: DSP

0 MASTER_MODE:
0: SAI OUTis in slave mode (default)
1: SAI OUTis in master mode

S2PCFG1 Serial-to-parallel audio interface configuration

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PDATA_LENGTH[1:0]		BICLK_OS[1:0]		MAP_L[1:0]		MAP_R[1:0]	

Address: 0x0B

Type: R/W

Buffer: No

Reset: 0x91

Description:

7:6 PDATA_LENGTH[1:0]: serial-to-parallel interface data length:
Length is (N+1) * 8 bit
Default (10) is 24 bit

5:4 BICLK_OS[1:0]: bit clock oversampling:
Value is (N+1) * 32 * fs (where fs = sampling frequency)
Default (01) is 64 fs

3:2 MAP_L[1:0]: left data-mapping slot:
Value is nth slot
Default (00) is slot 0

1:0 MAP_R[1:0]: right data-mapping slot:
Value is nth slot
Default (01) is slot 1

P2SCFG0 Parallel-to-serial audio interface configuration

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
BICLK_ STRB	LRCLK_LEFT	SDATAO_ACT	MSB_FIRST	DATA_FORMAT[2:0]			MASTER_ MODE

Address: 0x0C

Type: R/W

Buffer: No

Reset: 0xD3

Description:

7 BICLK_STRB: defines the bit clock edges:
0: strobe is falling edge, active edge is rising
1: strobe is rising edge, active edge is falling (default)

6 LRCLK_LEFT: defines the channel for the LR clock:
0: clock is low for left channel, high for right channel
1: clock is high for left channel, low for right channel (default)

5 SDATAO_ ACT: sets the behavior of pin SDATAO:
0: output is tristated when no data is sent (default)
1: output is never in tri-state (it is 0 when no data is sent)

4 MSB_FIRST: data alignment in the protocol for SDATAI and SDATAO:
0: LSB is the first bit
1: MSB is the first bit (default)

3:1 DATA_FORMAT[2:0]: serial interface protocol format:
000: left justified
001: I^2S (default)
010: right justified
100: PCM no delay
101: PCM delay
111: DSP

0 MASTER_ MODE: selects serial interface master/slave mode:
0: slave
1: master (default)

P2SCFG1 Parallel-to-serial audio interface configuration

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PDATA_LENGTH[1:0]		BICLK_OS[1:0]		MAP_L[1:0]		MAP_R[1:0]	

Address: 0x0D

Type: R/W

Buffer: No

Reset: 0x91

Description:

7:6 PDATA_LENGTH[1:0]: serial-to-parallel interface data length:
Length is (PDATA_LENGTH+1) * 8 bit
Default (10) is 24 bits

5:4 BICLK_OS[1:0]: bit clock oversampling:
Value is (BICLK_OS+1) * 32 * fs
Default (01) is 64 fs

3:2 MAP_L[1:0]: left data-mapping slot:
Value is nth slot
Default (00) is slot0

1:0 MAP_R[1:0]: right channel data-mapping slot:
Value is nth slot
Default (01) is slot1

PLLCFG0 PLL configuration

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PLL_DIRECT_PROG	FRAC_CTRL	DITHER_DISABLE[1:0]		IDF[3:0]			

Address: 0x14

Type: R/W

Buffer: No

Reset: 0x00

Description:

7 PLL_DIRECT_PROG: PLL programming:
0: default
1: PLL is programmed according to the PLLCFG register settings

6 FRAC_CTRL:
0: default
1: PLL fractional-frequency synthesis is enabled

5:4 DITHER_DISABLE[1:0]:
00: default
1x: disables rectangular phase frequency divider dither input to fractional control
x1: disables triangular Phase Frequency Divider dither input to Fractional Control
The mentioned blocks are shown in *Figure 5*.

3:0 IDF[3:0]: PLL input division factor:
0000: IDF = 1 (default)
0001: IDF = 1
0010: IDF = 2
…
1111: IDF = 15

PLLCFG1 PLL configuration (MSBs)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
FRAC_INPUT[15:8]							

Address: 0x15

Type: R/W

Buffer: No

Reset: 0x00

Description:

7:0 FRAC_INPUT[15:8]: MSBs of FRAC_INPUT[15:0] used to set the fractional part of PLL multiplication factor

PLLCFG2 PLL configuration (LSBs)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
FRAC_INPUT[7:0]							

Address: 0x16

Type: R/W

Buffer: No

Reset: 0x00

Description:

7:0 FRAC_INPUT[7:0]: LSBs of FRAC_INPUT[15:0] used to set the fractional part of PLL multiplication factor

PLLCFG3 PLL configuration

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
STRB	STRB_BYPASS	NDIV[5:0]					

Address: 0x17

Type: R/W

Buffer: No

Reset: 0x00

Description:

7 STRB: asynchronous strobe input to the fractional controller:
0: default

6 STRB_BYPASS: standby bypass:
0: STRB signal is not bypassed (default)
1: STRB signal is bypassed

5:0 NDIV[5:0]: PLL multiplication factor (integral part) named as loop division factor:
0000 XX: LDF = NA
0001 00: LDF = NA
0001 01: LDF = 5
...
1101 11: LDF = 55
111X XX: LDF = NA
0000 00: default

PLLPFE PLL/POP-free configuration

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PLL_BYP_UNL	BICLK2PLL	PLL_PWDN	PFE1A	PFE1B	PFE2A	PFE2B	RESET_FAULT

Address: 0x18

Type: R/W

Buffer: No

Reset: 0x00

Description:

7 PLL_BYP_UNL: PLL bypass:
0: PLL is not bypassed (default)
1: PLL is bypassed when not locked

6 BICLK2PLL:
0: default
1: BICLKI is input to PLL

5 PLL_PWDN:
0: default
1: PLL is in power-down mode

4 PFE1A:
0: default
1: POP-free resistances are connected to output 1A

3 PFE1B:
0: default
1: POP-free resistances are connected to output 1B

2 PFE2A:
0: default
1: POP-free resistances are connected to output 2A

1 PFE2B:
0: default
1: POP-free resistances are connected to output 2B

0 RESET_FAULT:
0: default
1: fault signal in the I^2C register POWST is reset

PLLST PLL status

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PLL_UNLOCK	PLL_PWD_ STATE	PLL_BYP_ STATE	Reserved				

Address: 0x19

Type: RO

Buffer: No

Reset: Undefined

Description:

7 PLL_UNLOCK: PLL unlock state:
0: PLL is not in unlock state
1: PLL is in unlock state

6 PLL_PWD_ STATE: PLL power-down state:
0: PLL is not in power-down state
1: PLL is in power-down state

5 PLL_BYP_STATE: PLL bypass state:
0: PLL is not in bypass state
1: PLL is in bypass state

4:0 Reserved

ADCCFG ADC configuration

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PGA[2:0]			INSEL	STBY	BYPASS_CALIB	CLKENBL	Reserved

Address: 0x1E

Type: RO

Buffer: No

Reset: Undefined

Description:

7:5 PGA[2:0]: gain selection bits for the ADC programmable gain amplifier:
000: default
Values are from 0 to 42 dB in 6 dB steps

4 INSEL:
0: line input selected (default)
1: microphone input selected (it must be applied to INL line)

3 STBY: ADC standby mode:
0: ADC in power-up mode (default)
1: ADC in standby mode

2 BYPASS_CALIB:
0: ADC DC-removal block not bypassed (default)
1: ADC DC-removal block bypassed

1 CLKENBL: Clock enable:
0: system clock not enabled
1: system clock available at ADC input (default)

0 Reserved

CKOCFG Output clock configuration

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
CLKOUT_DIS	CLKOUT_SEL[1:]]		Reserved				

Address: 0x1F

Type: R/W

Buffer: No

Reset: Undefined

Description:

7 CLKOUT_DIS: CLKOUT PAD disabled
0: default
1: enabled

6:5 CLKOUT_SEL[1:0]:
00: default
The CLKOUT output frequency is the PLL output frequency divided by 2^{CLKOUT_SEL}

4:0 Reserved

MISC Miscellaneous configuration

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
OSC_DIS	P2P_FS_RANGE[2:0]			ADC_FS_RANGE[1:0]		P2P_IN_ADC	CORE_ CLKENBL

Address: 0x20

Type: R/W

Buffer: No

Reset: 0x20

Description:

7 OSC_DIS: enable/disable crystal oscillator:
0: default
1: disabled

6:4 P2P_FS_RANGE[2:0]: FFX audio frequency range:
000: very low (fs = 8 to 12 kHz)
001: low (fs = 16 to 24 kHz)
010: normal (fs = 32 to 48 kHz) (default)
011: high (fs = 64 to 96 kHz)
1X: very high (fs = 128 to 192 kHz)

3:2 ADC_FS_RANGE[2:0]: ADC audio frequency range:
00: normal (fs = 32 to 48 kHz) (default)
01: low (fs = 16 to 24 kHz)
1X: very low (fs = 8 to 12 kHz)

1 P2P_IN_ADC: FFX input:
0: FFX input is from serial-to-parallel audio interface (default)
1: FFX input is from ADC

0 CORE_CLKENBL: availability of system clock:
0: FFX system clock disabled (default)
1: FFX system clock enabled

FFXST FFX status

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Reserved					INVALID_INP_ FBK	MUTE_INT_FBK	Reserved

Address: 0x23

Type: RO

Buffer: No

Reset: Undefined

Description:

7:3 Reserved

2 INVALID_INP_FBK: invalid input status:
1: invalid input sent to FFX

1 MUTE_INT_FBK: FFX mute status
1: FFX is in mute state

0 Reserved

PWMINT1 PWM driver configuration (MSBs)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PWM_INT[15:8]							

Address: 0x2D

Type: R/W

Buffer: No

Reset: 0x00

Description:

7:0 PWM_INT[15:8]: MSBs of PWM_INT[15:0], see *Chapter 8: Driver configuration on page 28*

PWMINT2 PWM driver configuration (LSBs)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PWM_INT[7:0]							

Address: 0x2E

Type: R/W

Buffer: No

Reset: 0x00

Description:

7:0 PWM_INT[7:0]: LSBs of PWM_INT[15:0], see *Chapter 8: Driver configuration on page 28*

POWST Power bridge status register

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
POW_ POWERDOWN	POW_ TRISTATE	POW_FAULT1A	POW_FAULT1B	POW_FAULT2A	POW_FAULT2B	Reserved	

Address: 0x32

Type: RO

Buffer: No

Reset: Undefined

Description:

7 POW_POWERDOWN: power-down bridge:
0: not in power-down state
1: power-down state

6 POW_TRISTATE:
1: power bridge is in tristate

5 POW_FAULT1A:
1: power bridge 1A is in fault state

4 POW_FAULT1B:
1: power bridge 1B is in fault state

3 POW_FAULT2A:
1: power bridge 2A is in fault state

2 POW_FAULT2B:
1: power bridge 2B is in fault state

1:0 Reserved

12 Package mechanical data

This section contains packaging information for the following packages:

- TFBGA48
- VFQFPN52

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK® is an ST trademark.

12.1 Package TFBGA48

Figure 18. Package outline (TFBGA48)

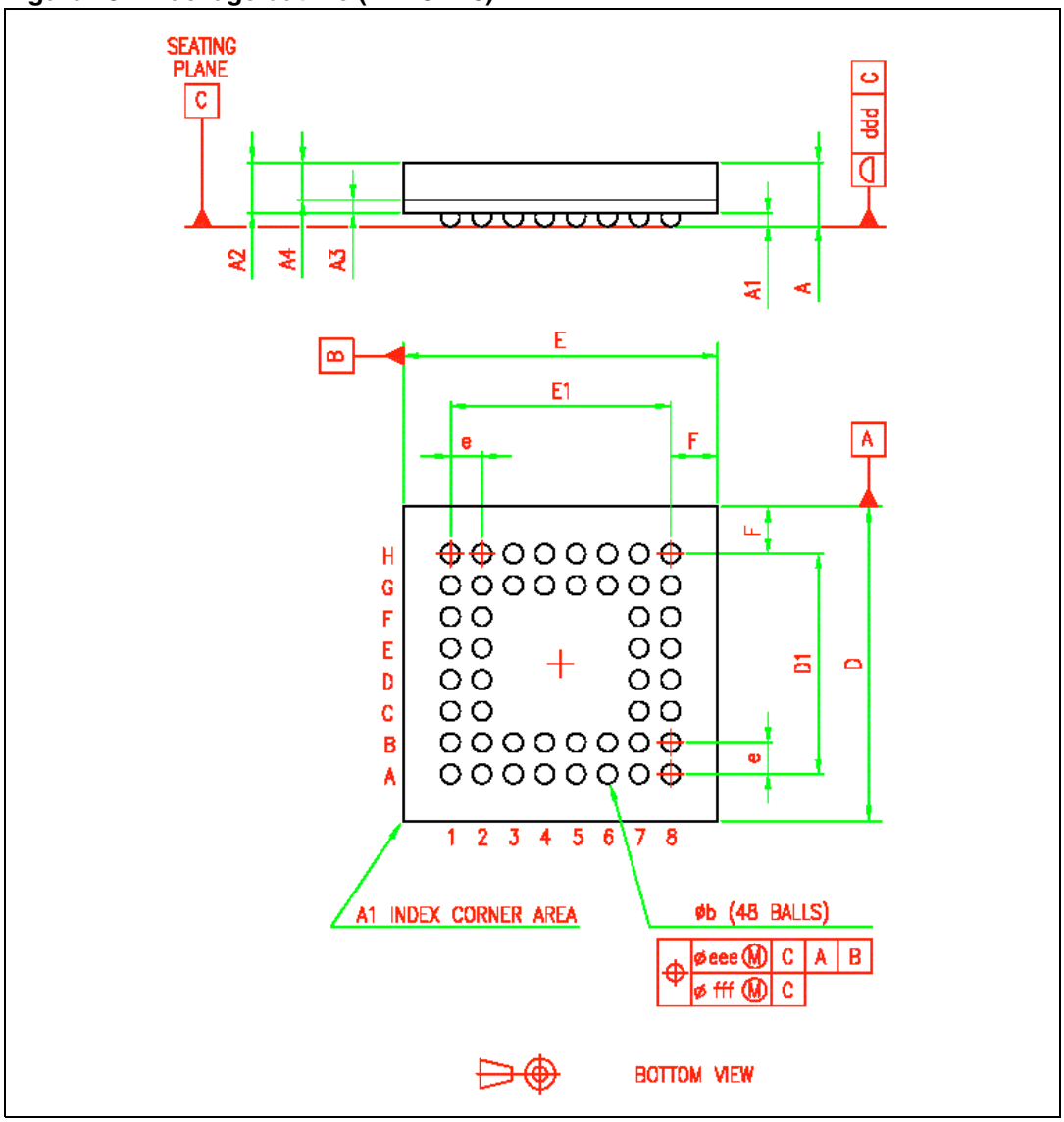


Table 23. Package dimensions (TFBGA48)

Reference	Dimensions in mm		
	Min	Typ	Max
A	-	-	1.20
A1	0.15	-	-
A2	-	0.785	-
A3	-	0.20	-
A4	-	-	0.60
b	0.25	0.30	0.35
D	4.85	5.00	5.15
D1	-	3.50	-
E	4.85	5.00	5.15
E1	-	3.50	-
e	-	0.50	-
F	-	0.75	-
ddd	-	-	0.08
eee	-	-	0.15
fff	-	-	0.05

12.2 Package VFQFPN52

Figure 19. Package outline (VFQFPN52)

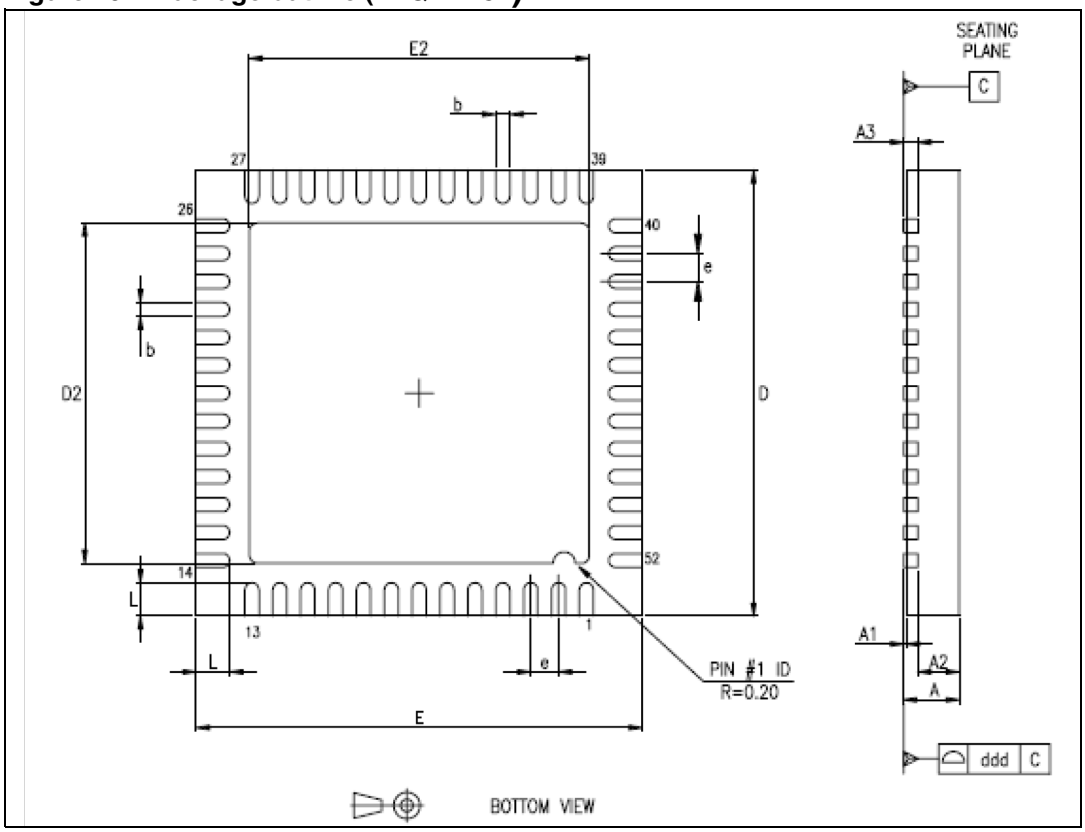


Table 24. Package dimensions (VFQFPN52)

Reference	Dimensions in mm		
	Min	Typ	Max
A	0.800	0.900	1.000
A1	-	0.020	0.050
A2	-	0.650	1.000
A3	-	0.250	-
b	0.180	0.230	0.300
D	7.875	8.000	8.125
D2	2.750	5.700	6.250
E	7.875	8.000	8.125
E2	2.750	5.700	6.250
e	0.450	0.500	0.550
L	0.350	0.550	0.750
ddd	-	-	0.080

13 Revision history

Table 25. Document revision history

Date	Revision	Changes
25-Jan-2007	1	Initial release.
09-Apr-2010	2	Complete update and change in presentation
30-Mar-2012	3	Updated *Features* Added *Section 6.3: Set fractional PLL* Updated *Section 7.2: Functional description* Minor textual updates

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