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1 Control Logic

1.1. General Description

The control logic of the ZSC31050 consists of the Calibration Microcontroller (CMC) and the modules control logic of the analog-to-digital converter (ADC), control logic of the digital ports, PWM and serial digital interface (SIF). The configuration of the various modes of the device is done by programming the EEPROM.

The CMC controls the measurement cycle and performs the calculations for sensor signal conditioning. This eliminates the gain deviation, the offset, the temperature deviation, and the non-linearity of the pre-amplified and A/D-converted sensor signal.

The communication of the ZSC31050 with an external microcontroller especially for calibration purposes is done via a serial digital interface. Communication protocols according to I²C™* and SPI standard are supported. Additionally a one-wire interface is implemented. These serial interfaces are used for the calibration of the sensor system consisting of a sensor transducer and ZSC31050.

Furthermore the serial interface makes available the read out of the results of sensor signal conditioning as digital values during the calibration or during the Normal Operation Mode (NOM) for processing by an external microcontroller. The internal processing of received interface commands is done by the CMC. As a result, the measurement cycle is interrupted if a command is received. Only the read out of data is controlled by the serial interface itself and does not interrupt the CMC.

The controller of the A/D-conversion is started by the CMC. It generates a clock for the ADC (switched capacitor technique) and the chopper clock for the analog front-end and executes a continuous measurement cycle. The result of the A/D-conversion is a counter value, which is read and processed after a synchronization signal that is generated after every measurement. The processing of the conditioning calculation by the CMC works in parallel to the A/D conversion.

The output of the conditioning result can be provided via various channels: analog voltage output, 4 to 20 mA current loop, or PWM. Additionally there are two digital output ports with programmable thresholds, hysteresis and delay.

* I²C™ is a trademark of NXP.

1.2. CMC Description

The Calibration Microcontroller (CMC) is especially adapted to the tasks connected with the signal conditioning. The main features are as follows:

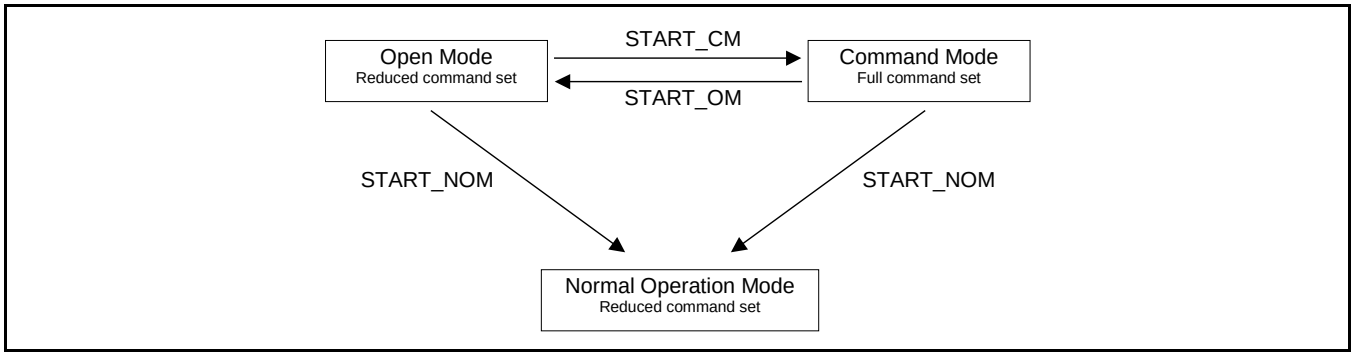
- Processing width: 16 bit
- Programmed via ROM
- Constants/coefficients for the conditioning calculation are stored in the EEPROM. After power-on or after re-initialization from EEPROM by sending a specific command to the serial interface, the EEPROM is mirrored to the RAM.
- Continuous parity-checking during every read from RAM. If incorrect data is detected, the diagnostic mode (DM) is activated (an error code is written to the serial digital output; the analog out is set to the diagnostic level).
- The conditioning calculation is done with 16-bit saturation arithmetic; i.e., if an overflow occurs in any calculation, the result is fixed to the maximum of the defined 16-bit range. The sign is preserved.

1.3. General Working Modes

ZSC31050 supports three different working modes:

- Normal Operation Mode (**NOM**)
- Command Mode (**CM**)
- Open Mode (**OM**)

Figure 1.1 Modes of Digital Serial Interface



1.3.1. Normal Operation Mode (NOM)

The Normal Operation Mode (NOM) is the working mode in which the signal conditioning operation is done. After power-on, the ZSC31050 starts with an initialization routine, which also can be started by sending a certain command via the serial digital interface at any time.

During the initialization routine, first the EEPROM is mirrored to the RAM, which checks the EEPROM content. If an error is detected, the DM is activated. The configuration of the ZSC31050, which is stored in the EEPROM, is consecutively set.

Next the continuous measurement cycle and the conditioning calculation start. The signal conditioning result is refreshed with each cycle time period. This generates the analog output at the OUT pin, and it can be read via the serial digital Interface (SIF) as a digital output.

Provided that the EEPROM is programmed correctly, the NOM operates without the microcontroller sending any command to the digital serial interface. Read-out of the conditioning result via the SIF is possible; this does not interrupt continuous processing of the signal conditioning routine.

1.3.2. Command Mode (CM)

The CM is the working mode that is used for calibration data acquisition and access to the internal RAM and EEPROM of the ZSC31050. The CM start command START_CM aborts the running NOM, so the measurement cycle is stopped. The ZSC31050 changes to CM only after receiving the START_CM command via the digital serial interface. This command generates an interrupt for the CMC, the measurement cycle is stopped, and the called command routine is processed. During processing, the serial interface is disabled; no further commands are recognized. After finishing the routine, the CMC waits for further commands. It is also possible to start the NOM by using the current contents of EEPROM or RAM.

1.3.3. Digital Serial Interface

For the digital serial interface, there are three modes: the Open Mode (OM), the Normal Operation Mode (NOM), and the Command Mode (CM). In OM and NOM, only a reduced set of commands is available. For all commands that change the configuration of the ZSC31050 (write to EEPROM/RAM, start different measurement cycle), the ZSC31050 must first be transferred to CM. This protects the ZSC31050 against unintentional configurations.

After power-on the ZSC31050 starts in Open Mode. Every command sent to the digital serial interface transfers the ZSC31050 to the Normal Operation Mode except the command START_CM, which starts the CM. The command START_CM is only processed if it is received as the first command after power-on via the digital serial interface. When the ZSC31050 enters NOM, this mode can only be reset by a new power-on. The ZSC31050 leaves the CM by receiving the command START_OM or START_NOM or by a reset due to power-on.

If the ZSC31050 receives a command in NOM that is not in the reduced command set, this command is ignored, no interrupt for the CMC is generated and the measurement cycle is continued. If the serial interface is operating in I²C™ mode, no acknowledges are generated after the command byte.

1.3.4. Error Codes

The ZSC31050 detects various possible errors. A detected error is signaled by changing in a diagnostic mode. In this case, the analog output is set to HIGH or LOW (maximum or minimum possible output value) and the output registers of the digital serial interface are set to a significant error code (see Table 1.1). Note that the error detection functionality must be individually enabled by configuration words (Sensor Connection; Common Mode Voltage out of limits).

Table 1.1 Error Codes

Detectable Error	Description	Enabled by [Register:Bit]	Sets SIF Output to	Sets Analog Out to Either	
				Voltage Out	Current Loop
EEPROM Sign	Signature check during read out of EEPROM after power-on or after SIF-Command COPY_EEP2RAM		$CAAA_{HEX}$	~VSS	<4mA
RAM Parity	Parity check at every RAM access	CFGAPP: SCCD	$CF0F_{HEX}$	~VSS	<4mA
Register Parity	Continuous parity check of configuration registers	CFGAPP: SCCD	$CE38_{HEX}$	~VSS	<4mA
ROM Check	Signature check of ROM after power-on	CFGCYC: ROMCHE	$CCCC_{HEX}$	~VSS	<4mA
Arithmetic Check	Arithmetic check during measurement cycle		$C1C7_{HEX}$	~VSS	<4mA
Watchdog	Watchdog check of start-routine and measurement-cycle		$C555_{HEX}$	~VSS	<4mA
Configuration	Programmed configuration is not allowed (conflict regarding A/D-conversion time and enabled functionality)		$C333_{HEX}$	~VSS	<4mA
Sensor Connection	Connection check of sensor bridge	CFGAPP: SCCD	$CFCF_{HEX}$	~VDDA	>20mA
				~VSS*	<4mA*
Common Mode Voltage Out of Limits	Check if bridge common mode voltage complies the programmed limits (CMV read command: DB_{HEX})	CGFCYC: ECMV	10_{BIN} + 14bits ADC result for $V_{IN\_CM}/2$	~VDDA	>20mA
			V_{IN_CM} = Measured Common Mode Voltage		
* ZSC31050 behavior after reset with the detectable error present.					

2 Signal Conditioning

2.1. AD Conversion

During Signal Conditioning Mode, the analog preconditioned sensor signal is continuously A/D converted. The A/D conversion is configurable regarding resolution r_{ADC} and the inherent range shift RS_{ADC} by the configuration words. Furthermore the one or two-step conversion mode is selectable (ADC order). The two-step conversion is faster, the one-step conversion is more accurate because of larger integration time. The selected configuration for the ADC is equal for all measurements (measurand (e.g., pressure), temperature 1 and 2, common mode voltage), thus the conversion time is constant during the whole measurement cycle. Only the inherent range shift is selectable individually for every single signal. Additionally for all measured signals auto-zero measurements are done during the measurement cycle. The resulting digital raw values for measurand (e.g. pressure) and temperature are defined by these equations:

⇒ Analog differential input voltage to A/D conversion

Measurand:

$$V_{ADC\_DIFF\_P} = a_{IN\_P} * V_{IN\_DIFF\_P} + V_{XZC}$$

Temperature:

$$V_{ADC\_DIFF\_T} = a_{IN\_T} * V_{IN\_DIFF\_T}$$

Residual Offset:

$$V_{ADC\_OFF} = a_{IN\_OFF} * V_{IN\_OFF}$$

⇒ Digital raw A/D-conversion result

$$Z_{ADC} = 2^{r_{ADC}} * \left(\frac{V_{ADC\_DIFF} + V_{ADC\_OFF}}{V_{ADC\_REF}} + 1 - RS_{ADC} \right)$$

Z_{ADC} will be returned by commands D1, D2 and D2 (refer to Table 4.6 for detailed command information)

V_{IN_DIFF}	Analog differential input voltage to analog front end
V_{IN_OFF}	Residual offset voltage of analog front end
V_{ADC_DIFF}	Analog differential input voltage to A/D converter
V_{ADC_OFF}	Residual offset voltage of analog front end to A/D converter
V_{ADC_REF}	ADC reference voltage (ratiometric reference for pressure measurement)
r_{ADC}	Resolution of A/D conversion
RS_{ADC}	Range shift of A/D conversion: Bridge sensor measurement: ½, ¾, $^{7}/_{8}$, $^{15}/_{16}$ Temperature measurement: ½
a_{IN_p}	Gain of analog front end for pressure signal
a_{IN_T}	Gain of analog front end for temperature signal
a_{IN_OFF}	Gain of analog front end for residual offset
V_{XZC}	Extended zero compensation voltage (refer to the *ZSC31050 Data Sheet* for details): $V_{XZC} = \frac{VDD_{BR} * k * Z_{XZC}}{20 * a_{IN}}$ (Z_{XZC} are bit fields in register CFGAFE and VDD_{BR} is the bridge voltage. Recommended Z_{XZC}= -20 to +20.)

⇒ **Auto-zero value**

$$Z_{AZ} = 2^{r_{ADC}} * \left(\frac{V_{ADC\_OFF}}{V_{ADC\_REF}} + 1 - RS_{ADC} \right)$$

⇒ Auto-zero corrected raw A/D-result

$$Z_{CORR} = Z_{ADC} - Z_{AZ} = 2^{r_{ADC}} * \frac{V_{ADC\_DIFF}}{V_{ADC\_REF}}$$

Z_{CORR} will be returned by commands D8, D9 and DA (refer to Table 4.6 for detailed command information)

2.2. Correction Formula for Measurand (e.g., Pressure Input Signal)

The digital raw value for the measurand is further processed with the correction formula to remove offset and temperature dependency and to compensate non-linearity up to the 3rd order. The signal conditioning equation is solved by the CMC and is defined as follows:

⇒ Range Definition of Inputs

$$Z_{CORR\_p} \in \left[-2^{r_{ADC}-1}; 2^{r_{ADC}-1} \right) \qquad (RS_{ADC} = ½)$$

$$Z_{CORR\_T1} \in \left[-2^{r_{ADC}-1}; 2^{r_{ADC}-1} \right) \qquad c_i \in \left[-2^{15}; 2^{15} \right)$$

⇒ Conditioning Equations

$$Y = \frac{Z_{CORR\_p} + c_0 + 2^{-(r_{ADC}-1)} * c_4 * Z_{CORR\_T1} + 2^{-2(r_{ADC}-1)} * c_5 * Z_{CORR\_T1}^2}{c_1 + 2^{-(r_{ADC}-1)} * c_6 * Z_{CORR\_T1} + 2^{-2(r_{ADC}-1)} * c_7 * Z_{CORR\_T1}^2}$$

$$Y \in [0; 1)$$

$$P = Y * \left(1 - 2^{-15} * c_2 - 2^{-15} * c_3\right) + 2^{-15} * c_2 * Y^2 + 2^{-15} * c_3 * Y^3$$

$$P \in [0; 1)$$

r_{ADC}	Resolution of A/D conversion
Z_{CORR_p}	Raw input main channel A/D result for measured value (auto-zero compensated)
Z_{CORR_T1}	Raw temperature input A/D result for measured value (auto-zero compensated)
Conditioning coefficients stored in EEPROM registers 0 to 7	
$c_i \in [-2^{15}; 2^{15})$, two's complement	
c_0 …	Bridge offset
c_1 …	Gain
c_2 …	Non-linearity 2nd order
c_3 …	Non-linearity 3rd order
c_4 …	Temperature coefficient Bridge offset 1st order
c_5 …	Temperature coefficient Bridge offset 2nd order
c_6 …	Temperature coefficient Gain 1st order
c_7 …	Temperature coefficient Gain 2nd order

The first equation compensates the offset and fits the gain including its temperature dependence. The non-linearity is then corrected regarding the intermediate result Y. The result of these equations is a non-negative 15-bit value P for the measurand (e.g., pressure) in the range [0; 1). This value P is continuously written to the output register of the digital serial interface during measurement cycle.

Note: The conditioning coefficients c_i are positive or negative values in two's complement.

2.3. Correction Formula for Temperature

There is also an option to condition the raw temperature value $Z_{CORR\_T1/2}$ regarding offset, gain and non-linearity. The result of this conditioning is a non-negative 15-bit value $T_{1/2}$ for temperature in the range [0; 1). This value $T_{1/2}$ is continuously written to the output register of the digital serial interface during the measurement cycle if the output is enabled. Note that the raw A/D result Z_{CORR_T1} for temperature is included in the conditioning of the measurand signal (section 2.2).

⇒ Range Definition of Inputs

$$Z_{CORR\_Ti} \in \left[-2^{r_{ADC}-1}; 2^{r_{ADC}-1} \right) \qquad t_i \in \left[-2^{15}; 2^{15} \right)$$

⇒ Conditioning Equations

$$Y_t = \frac{Z_{CORR\_Ti} + t_0}{t_1} \qquad Y_t \in [0;1)$$

$$T_i = Y_t * \left(1 - 2^{-15} * t_2\right) + 2^{-15} * t_2 * Y_t^2$$

$$T_i \in [0;1)$$

r_{ADC}	Resolution of A/D conversion
Z_{CORR_Ti}	Raw input main channel A/D result temperature T1/T2 (auto-zero compensated)
	Conditioning coefficients stored in EEPROM registers 10 to 15; $ti \in [-2^{15}; 2^{15})$ two's complement:
t_0 …	Temperature offset
t_1 …	Gain
t_2 …	Non-linearity 2nd order

The first equation compensates the offset and fits the gain. The nonlinearity is then corrected regarding the intermediate result Y_t.

Note: The conditioning coefficients t_i are positive or negative values in two's complement.

2.4. Limiting the Output

The conditioning results for measurand P and temperature $T_{1/2}$ can be output via different channels. For each channel, an individual set of minimum and maximum limits is defined in EEPROM in consideration of the resolution of the chosen output channel.

⇒ Limitation

$$P_{out}(P > I_{max}) = I_{max}$$
$$P_{out}(P < I_{min}) = I_{min} \qquad P_{out} \in [I_{min}; I_{max})$$

$$T_{out}(T > I_{max}) = I_{max}$$
$$T_{out}(T < I_{min}) = I_{min} \qquad T_{out} \in [I_{min}; I_{max})$$

Limits stored in EEPROM Register 8, 9 or 16, 17; $I_{min/max} \in [0; 2^{Output\text{-}Resolution})$:

I_{min} ... Lower output limit

I_{max} ... Upper output limit

Note: The limits Imin and Imax must match the resolution of the corresponding analog output. That means the limits for the analog voltage output (maximum resolution: 11-bit) must be defined in the range [0 ; 211), the limits for the PWM output (maximum resolution: 12-bit) must be defined in the range [0 ; 212).

3 Outputs

3.1. General Description

The ZSC31050 offers a variety of output modes via two output channels for the conditioning results of measurand (e.g., pressure) and temperature signals. The modes are Analog Voltage Output, 4 to 20 mA Current Loop, and two PWM outputs (PWM1 and PWM2). The three possible result values for the measurand and the two temperatures can be switched independently to these different outputs by EEPROM programming (CFGCYC:ACOS1, CFGCYC:ACOS2, see section 5.3). Furthermore, two ALARM output modes are available that apply only to the measurand value. Table 3.1 shows the options for outputting result values on the available outputs.

Table 3.1 Accessibility of Outputs

Output	Accessible with			Pin
	Measurand	Temperature 1	Temperature 2	
Analog voltage output	yes	yes	yes	OUT
4 to 20 mA current loop	yes	yes	yes	OUT
PWM1	yes	yes	yes	IO1
PWM2	yes	yes	yes	OUT
Alarm 1 *	yes	-	-	IO1
Alarm 2 *	yes	-	-	IO2 *

The possible combinations of the available outputs are limited by the pins used: OUT, IO1 and IO2. Consequently an output mode using the OUT pin can only be combined with an output mode using the pin IO1 or IO2 or both. The configuration is done by EEPROM programming (CFGOUT:COS1, CFGOUT:PMIO1, CFGOUT:PMIO2, see section 5). Table 3.2 shows all possible combinations of available outputs.

The associated result value (measurand or temperature) is always updated when a new value is calculated using the conditioning equations (see section 2). In addition the calculated values are also available as digital values at the digital serial interface.

* Application access to Port IO2 during the active ZACwire Mode (ZACwire Start Window or active “OWI Continuous Mode”) is not possible. The ALARM function is not applicable if an A/D resolution less than 13-bit and second order is set.

Table 3.2 Available Combinations of Outputs *(x = either 0 or 1)*

CFGOUT - EEPROM address 1B/27 (see section 5.3)			**Pin**		
COS1	PMIO1	PMIO2	OUT	IO1	IO2
00	0x	0	Analog voltage output	-	-
01	0x		(4 to 20) mA current loop	-	-
10	0x		PWM2	-	-
00	10		Analog voltage output	PWM1	-
01	10		(4 to 20) mA current loop	PWM1	-
10	10		PWM2	PWM1	-
00	11		Analog voltage output	Alarm 1	-
01	11		(4 to 20) mA current loop	Alarm 1	-
10	11		PWM2	Alarm 1	-
00	0x	1	Analog voltage output	-	Alarm 2
01	0x		(4 to 20) mA current loop	-	Alarm 2
10	0x		PWM2	-	Alarm 2
00	10		Analog voltage output	PWM1	Alarm 2
01	10		(4 to 20) mA current loop	PWM1	Alarm 2
10	10		PWM2	PWM1	Alarm 2
00	11		Analog voltage output	Alarm 1	Alarm 2
01	11		(4 to 20) mA current loop	Alarm 1	Alarm 2
10	11		PWM2	Alarm 1	Alarm 2

3.2. PWM Output

The ZSC31050 offers two PWM outputs at the OUT pin and at the IO1 pin.

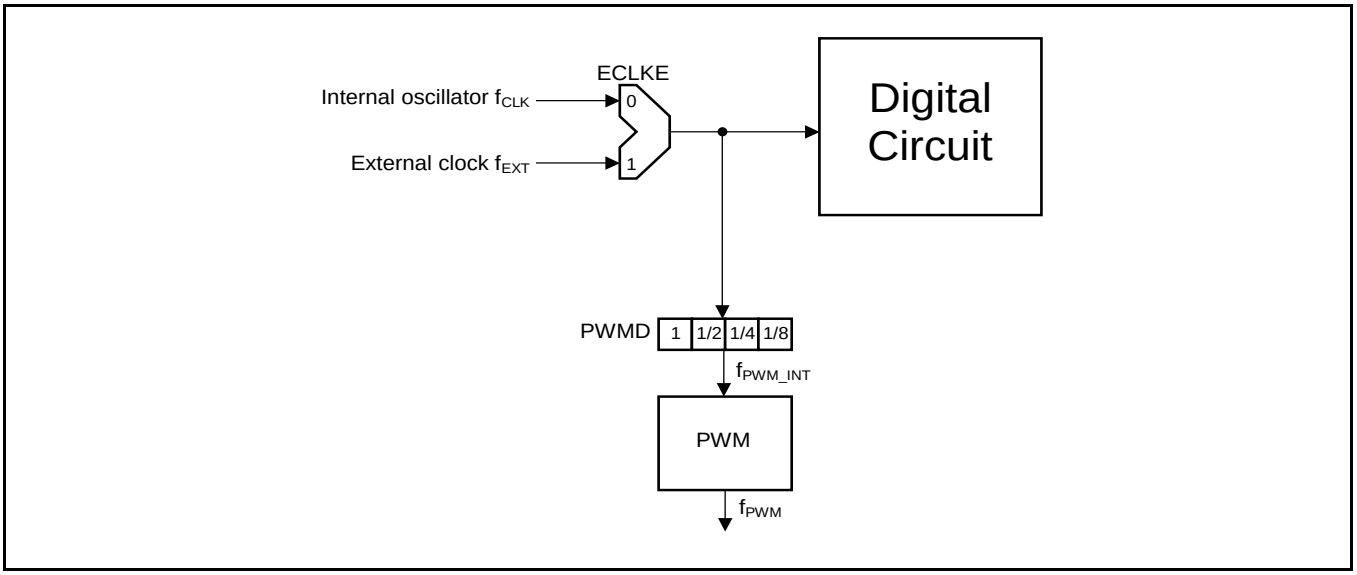
The PWM works synchronously

- To the internal oscillator frequency (f_{CLK} = 1 / 2 / 4 MHz, CFGAPP:OSCF) or
- To an external frequency (f_{EXT} = 2 to 4 MHz, CFGAPP:ECLKE = 1).

When an external frequency (f_{EXT}) is used, it must be supplied via the IN3 pin. Furthermore, it is possible to divide the frequency used by 2, 4, or 8 (CFGOUT:PWMD).

Figure 3.1 illustrates the influence of the EEPROM configuration on the internal frequencies used.

Figure 3.1 Possible Frequency Supply for PWM Output



The resolution r_{PWM} for PWM output (9 / 10 / 11 / 12 bit) must be defined again by EEPROM programming (CFGOUT:PWMRES). The resulting frequency of the PWM output depends on this resolution and on the internal frequency used.

$$f_{PWM} = f_{PWM\_INT} / 2^{r_{PWM}}$$

This results in frequencies for the PWM output as listed in Table 3.3. Note that the selected frequency of f_{CLK} or f_{EXT} will also influence the A/D conversion rate.

Table 3.3 Available Frequencies of PWM Output

f_{CLK} or f_{EXT}	d_{PWM} (CFGOUT:PWMD)	r_{PWM} (CFGOUT:PWMRES)			
		9 Bit	10 Bit	11 Bit	12 Bit
4 MHz	1	7.8 kHz	3.9 kHz	1.95 kHz	975 Hz
4 MHz	1/2	3.9 kHz	1.95 kHz	975 Hz	490 Hz
4 MHz	1/4	1.95 kHz	975 Hz	490 Hz	245 Hz
4 MHz	1/8	975 Hz	490 Hz	245 Hz	122 Hz
2 MHz	1	3.9 kHz	1.95 kHz	975 Hz	490 Hz
2 MHz	1/2	1.95 kHz	975 Hz	490 Hz	245 Hz
2 MHz	1/4	975 Hz	490 Hz	245 Hz	122 Hz
2 MHz	1/8	490 Hz	245 Hz	122 Hz	61 Hz
1 MHz	1	1.95 kHz	975 Hz	490 Hz	245 Hz
1 MHz	1/2	975 Hz	490 Hz	245 Hz	122 Hz
1 MHz	1/4	490 Hz	245 Hz	122 Hz	61 Hz
1 MHz	1/8	245 Hz	122 Hz	61 Hz	30 Hz

The result value for the PWM output is calculated by using the limiting equations (section 2.4) and is in the range of [l_{min}, l_{max}]. These limits l_{min} and l_{max} are defined in the EEPROM registers 8 and 9 for PWM2 (OUT pin) and 16 and 17 for PWM1 (Pin IO1), respectively. It must match the selected resolution r_{PWM} for the PWM output; i.e. the limits must be defined in the range [0, $2^{r_{PWM}}$).

The resulting PWM signal for an output value OUT for the measurand (e.g., pressure), temperature T1, or temperature T2 then has a duty cycle dc_{PWM} of

$$dc_{PWM} = \frac{(OUT + 1)}{2^{r_{PWM}}}$$

Furthermore, the polarity of the PWM output signal can be defined by EEPROM programming (CFGOUT:PWMPO); i.e., this defines whether a PWM clock cycle starts with a high or low level.

3.2.1. Alarm Tasks

The ZSC31050 offers two independently configurable alarm tasks (timer and comparator), which can be used as a programmable switch output. The IO1 and IO2 pins are used as the output for these ALARM tasks. The <OUT> output signal, defined by CFGCYC:ACOS1, is used as the input/source for both alarm tasks.

The behavior of the alarm output can be configured by four parameters for both alarms:

- Switch on threshold A_{ON}
- Hysteresis A_{HYST} is used for calculation of the switch off threshold $A_{OFF} = A_{ON} - A_{HYST}$
- Switch on delay A_td_{ON} and switch off delay A_td_{OFF}

Alarm tasks are realized completely in the firmware of the ZSC31050, so the NOM (running signal conditioning loop) is necessary for operation of the alarm outputs. The programmed switch on/off threshold is compared with the current-limited signal conditioning result for processing the alarm task.

3.2.2. Alarm Outputs and Processing Tasks

The activation of programmable IOs is scheduled in three tasks:

- Power-on and EEPROM-signature calculation: approx. 2ms
  => Alarm output IO1/IO2 is in the tristate.
- Processing of the start procedure
  => Alarm output IO1/IO2 is in programmed “inactive” state (CFGOUT:APO)
- Alarm operation depending on source and alarm configuration (registers: 16_{HEX} to 21_{HEX})
  => IOs are working like programmed

The start procedure consists of 4 to 7 measurement tasks (PAZ, P, T1, T1AZ, T2, T2AZ, CMV); also refer to the *ZSC31050 Data Sheet,* section 2.3.3. Each of these tasks requires a specific conversion time defined by the ADC adjustment (ADC-resolution, ADC-order, ADC-clock divider, clock frequency) in the range of 125µs to 100ms.*

Remark: ALARM tasks are not applicable if using an A/D resolution lower than 13-bit and second order is set; otherwise, a timing error is indicated.

3.2.3. Alarm Configuration

The alarm output is set HIGH if the programmed threshold A_{ON} is exceeded and reset if the value is less than the resulting threshold A_{OFF} (CFGOUT:APO=1). CFGOUT:APO=0 inverts this behavior.

Table 3.4 Alarm Parameter Calculation

Threshold	Calculation
Switch on threshold A_{ON}	AON [%] = ALARM_REG1 ∗100 / 65536 with ALARM_REG1 = Register 10_{HEX} or 13_{HEX} for Alarm1 or Alarm2 respectively (See Table 5.1.)
Switch off threshold A_{OFF}	AOFF [%] = AON [%] - ALARM_REG2 ∗100 / 65536 with ALARM_REG2 = Register 11_{HEX} or 14_{HEX} for Alarm1 or Alarm2 respectively
Switch on/off delay A_td_{ON} / A_td_{OFF}	A_tdON = ALARM_REG3[7:0] ∗ 4 ∗ AD_ConversionTime A_tdOFF = ALARM_REG3 [13:8] ∗ 64 ∗ AD_ConversionTime with ALARM_REG3 = Register 12_{HEX} or 15_{HEX} for Alarm1 or Alarm2 respectively

* Also refer to the spreadsheet *ZSC31050_Bandwidth_Calculation_Rev_X_xy.xls*.

3.2.4. Window Mode

If the Window Alarm Mode is active (CFGOUT:AWME=1) the thresholds for alarm1/2 define the limits of the window, hysteresis, and ON/OFF delays, which function the same as described above. The both ALARM outputs are inverted relative to each other. It is not important which limit is higher. When the input value is inside the window limits, the ALARM1 shows:

- HIGH if programmed for ALARM1=High active & ALARM2=High active
- LOW if programmed for ALARM1=High active & ALARM2=Low active
- HIGH if programmed for ALARM1=Low active & ALARM2=Low active
- LOW if programmed for ALARM1=Low active & ALARM2=High active

All these values must be programmed in the EEPROM.

When the ZSC31050 SSC Evaluation Kit software is used for programming the EEPROM, the configuration files “ALARM1.31050” and “ALARM2.31050” can demonstrate how this functions with a threshold of 2.5V (Alarm1, low active) and 3.7V (Alarm2, low active) and the file “ALARM_WINDOW.31050” shows how it works with these thresholds as window limits.

3.3. Digital Readout

The ZSC31050 also supports digital readout in NOM; three 16-bit SIF output registers can be read out (high byte and MSB first; also known as “Big Endian”). The count of registers to be read out is defined in configuration register CFGSIF and by the setting for bits SIFOUTP, SIFOUTT1 & SIFOUT2. The read output result is a non-limited 15-bit value; the MSB is always “0.” The MSB is the error identification bit; in the case of an error, this bit is set.

The output can be read out continuously (i.e., without a stop condition). Then the contents of registers such as the programmed (CFGSIF) are sent in a loop. The content of SIF readout registers is refreshed if a new conditioning result is valid. The SIF state machine ensures that a running readout operation is not disturbed by refreshing of the readout data. Refer to section 4 for a detailed description of SIF and the communication protocols used.

Important: Be carefully if clearing the EEPROM: do not power off/on or restart the ZSC31050 after this. Clearing the EEPROM resets all the communication flags (CFGSIF:SIFOUTT2/SIFOUTT1/SIFOUTP) of the interface. If this is activated, no communication is possible. Reactivation is possible by sending the following commands: “B70034”, “C9” and “01”.

4 Serial Digital Interface

4.1. General Description

The ZSC31050 includes a serial digital interface, which is able to communicate using three different communication protocols: I²C™, SPI and a ZACwire™ (one-wire, OWI) communication (see Figure 4.1). The serial digital interface allows the programming of the EEPROM to configure the application mode of the ZSC31050 and to calibrate the conditioning equation. Furthermore it provides the read out of the conditioning results of the measurand and both temperatures as digital 15-bit values.

The ZSC31050 always functions as a slave. The communication protocol used must be chosen by programming the EEPROM. There are also commands to change the valid communication mode. Only one communication protocol is valid at one time. The implemented commands are available in all communication modes but are divided into two sets with different validity (refer to sections 1.3.3 and 4.3.4). Commands that change the configuration of the device are suppressed in Normal Operation Mode (NOM) and are available only after changing to Command Mode (CM).

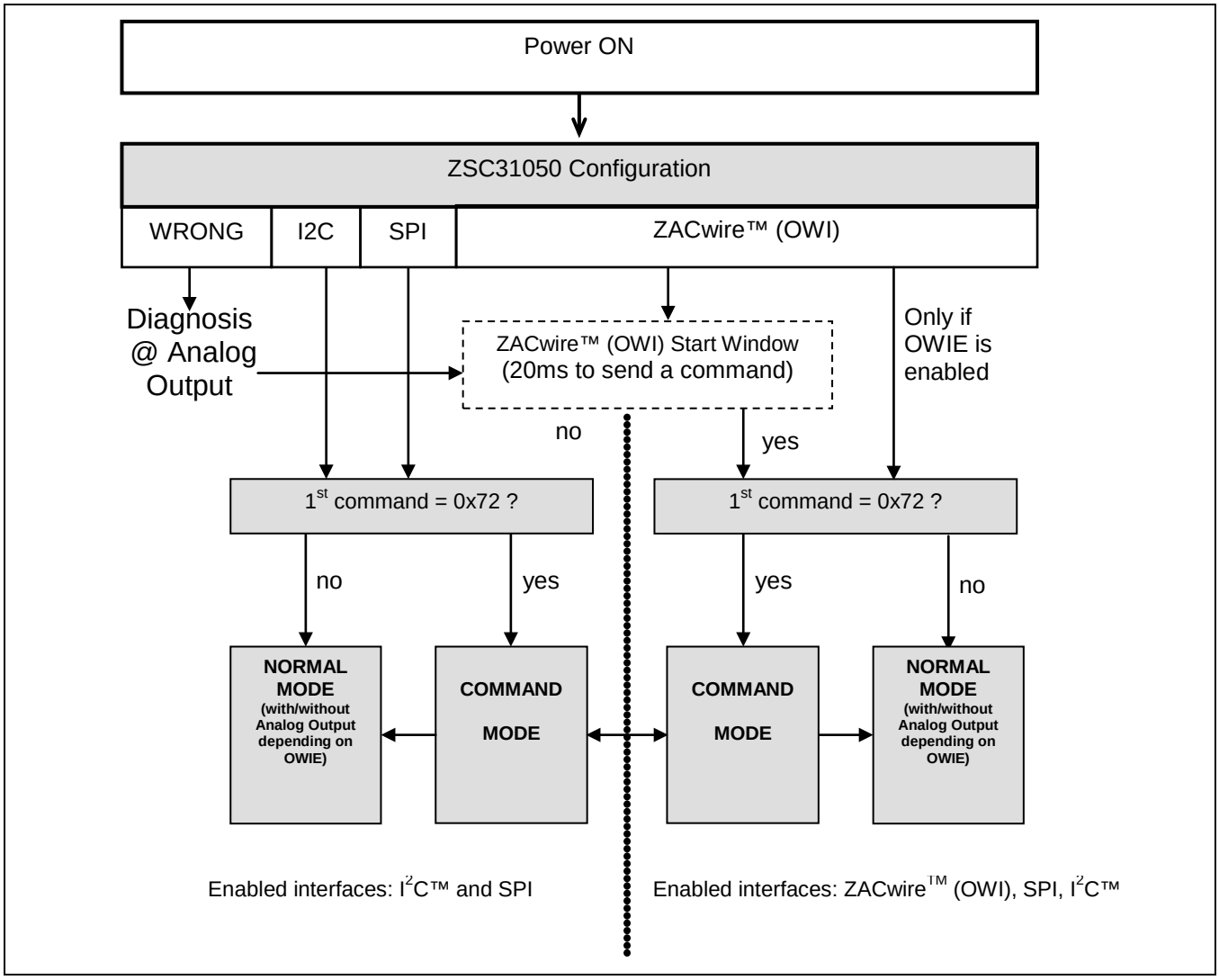
A non-configured device, identified by a CRC error for the EEPROM contents, starts up in a special mode so that communication by any of the available protocols is possible. After power-on, a 20ms time window is opened to start OWI communication (the OWI-start-window). If no OWI communication is detected, the serial digital interface changes to a mode in which it can receive commands in I²C™ Mode as well as in SPI Mode. If it is necessary to read out data from a non-configured device (transmission by slave), the communication protocol used must be explicitly defined by sending a specific command. Note that the ZSC31050 also does not send acknowledges in non-configured mode if I²C™ communication is used.

If the ZSC31050 receives a valid command at the serial digital interface, the measurement cycle is interrupted because the internal microcontroller must execute the requested command routine. An exception is a read-request. The ZSC31050 answers without interrupting the measurement cycle. This allows the read-out of the digital conditioning results during measurement cycle. A command consists of an address byte and a command byte. Additionally the commands for writing the EEPROM or its mirror in the RAM include two data bytes. This is independent from the communication protocol used. To read data from the ZSC31050 (e.g., EEPROM contents) usually a specific command must be sent to transfer this data into the output register of the serial interface. Thereafter the READ command, consisting of the address byte with the read bit set, is used to get this data. The data are transmitted continuously and repeated as long as the master send the clock and does not abort the command by generating a stop condition. Again this is independent from the communication protocol used. During the measurement cycle, the ZSC31050 transfers the conditioning results into the output registers of the serial digital interface. There are three registers for the measurand and both temperatures. The activation of these registers and consequently of the transmitted data must be set by EEPROM programming. If the master sends a read request, the results are sent in the sequence measurand, temperature 1, and temperature 2, according to the register activation.

The high byte and MSB must be sent first when sending 16-bit words ("Big Endian" notation).

Communication is controlled by the internal clock frequency. The internal clock frequency f_{CLK} must be a minimum of 5 times higher than communication clock frequency.

Figure 4.1 Possible Communication Configuration

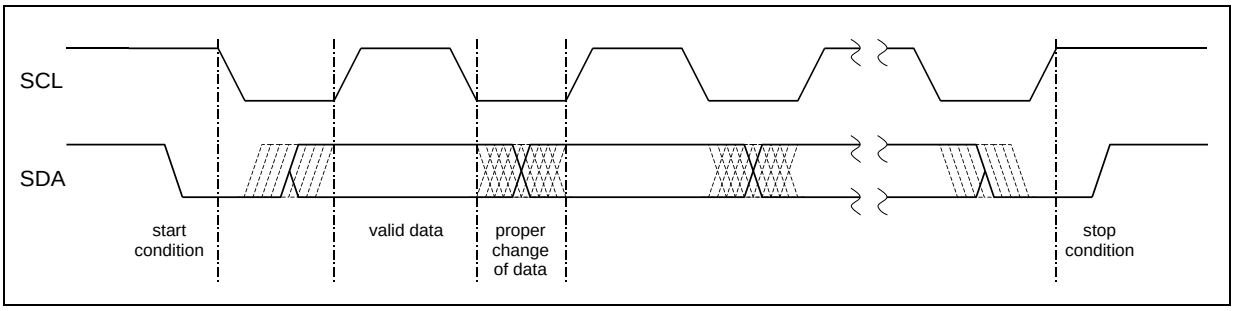


4.2. I²C™ Protocol

For I²C™ communication a data line (SDA) and a clock line (SCL) are required. The I²C™ protocol used is defined as follows:

- **Idle period**
  During inactivity of the bus, SDA and SCL are pulled-up to supply voltage VDDA.
- **Start condition**
  A high to low transition on SDA while SCL is at the high level indicates a start condition. Every command must be initiated by a start condition sent by a master. A master can always generate a start condition.
- **Stop condition**
  A low to high transition on SDA while SCL is at high level indicates a stop condition. A command must be closed by a stop condition to start processing the command routine inside the ZSC31050.

Figure 4.2 Principles of I²C™ Protocol Actions



- **Valid data**
  Data is transmitted in bytes (8 bits) starting with the most significant bit (MSB), 16 bit data words are transmitted beginning with high byte first (=“Big Endian”). Each byte transmitted is followed by an acknowledge bit. Transmitted bits are valid if after a start condition SDA remains at constant level during the high period of SCL. The SDA level has to change only when clock signal at SCL is low.
- **Acknowledge**
  An acknowledge after the transmitted byte is obligatory. The master must generate an acknowledge-related clock pulse. The receiver (slave or master) pulls-down the SDA line during the acknowledge clock pulse. If no acknowledge is generated by the receiver, a transmitting slave will become inactive. A transmitting master can abort the transmission by generating a stop condition and can repeat the command.

  A receiving master must signal the end of transfer to the transmitting slave by not generating an acknowledge-related clock pulse at SCL.

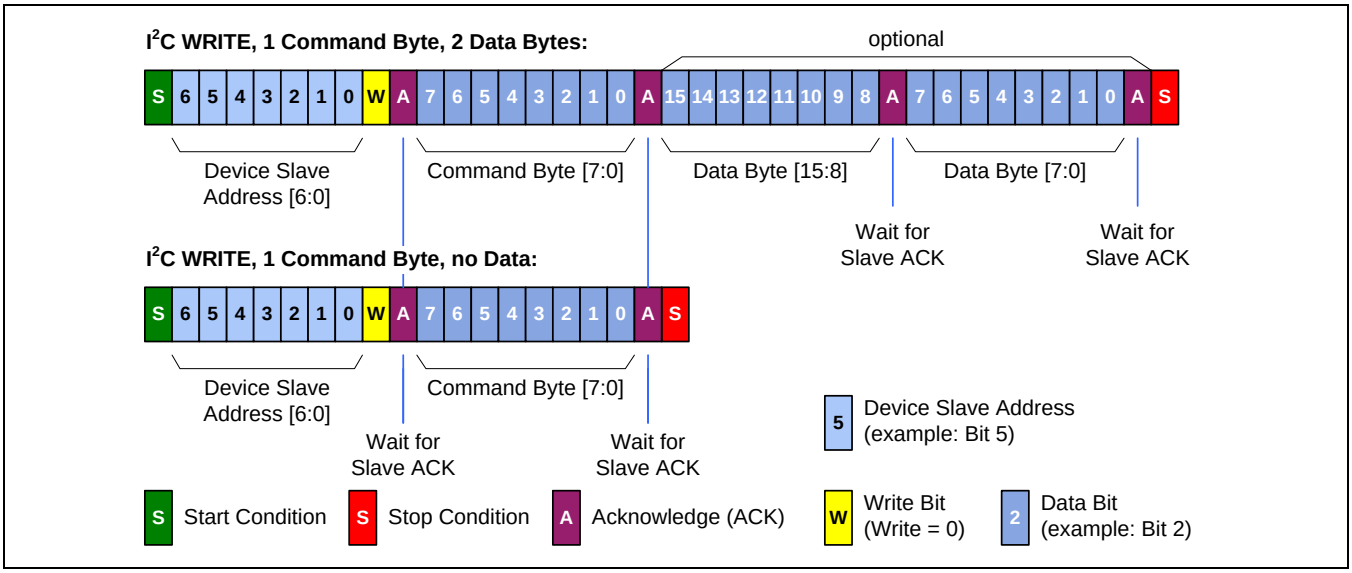
  The ZSC31050 as a slave changes to inactive interface mode during processing of internal command routines started by a previously sent command.
- **Addressing**
  Every slave connected to the I²C™-bus responds to a certain address. After generating the start condition, the master sends the address byte containing a 7-bit address followed by a data direction bit (R/W). A ‘0’ indicates a transmission from master to slave (WRITE); a ’1’ indicates a data request (READ).

  The addressed slave answers with an acknowledge; all other slaves connected with the I²C™ bus ignore this communication.

The general ZSC31050 slave address is 78_{HEX} (7-bit). By EEPROM programming, it is possible to allocate and activate an additional arbitrary slave address to every individual device. In this case, the device recognizes communication on both addresses: on the general one and on the activated one.

- **Write operation**
  During transmission from master to slave (WRITE), the address byte is followed by a command byte and depending on the transmitted command, an two optional data bytes. The internal microcontroller evaluates the received command and processes the related routine. A detailed description of the command set is given in section 4.5. The following figure illustrates the writing of a command with two data bytes and without data bytes.

Figure 4.3 I²C™ – Write Operation



- **Read Operation**
  After a data request from the master to the slave by sending an address byte including a set-data-direction bit, the slave answers by sending data from the activated interface output registers. The master must generate the transmission clock on SCL, the acknowledges after each data byte (except after the last one), and finally the stop condition.

  A data request is answered by the interface module itself and consequently does not interrupt the active process of the internal microcontroller. The data in the activated registers is sent continuously until a stop condition is detected; after transmitting all available data, the slave starts repeating the data.

  During the active measurement cycle, data is continuously updated with conditioning results. To get other data from the slave (e.g., EEPROM contents), usually a specific command must be sent before the data request to initiate the transfer of this data to the interface output registers. This command does interrupt the current process of the internal microprocessor and consequently also an active measurement cycle.

Figure 4.4 I²C™ – Read Operation – Data Request

Note: the n[th] data byte is the last required data byte; readout can be processed in a loop without the master resending initialization.

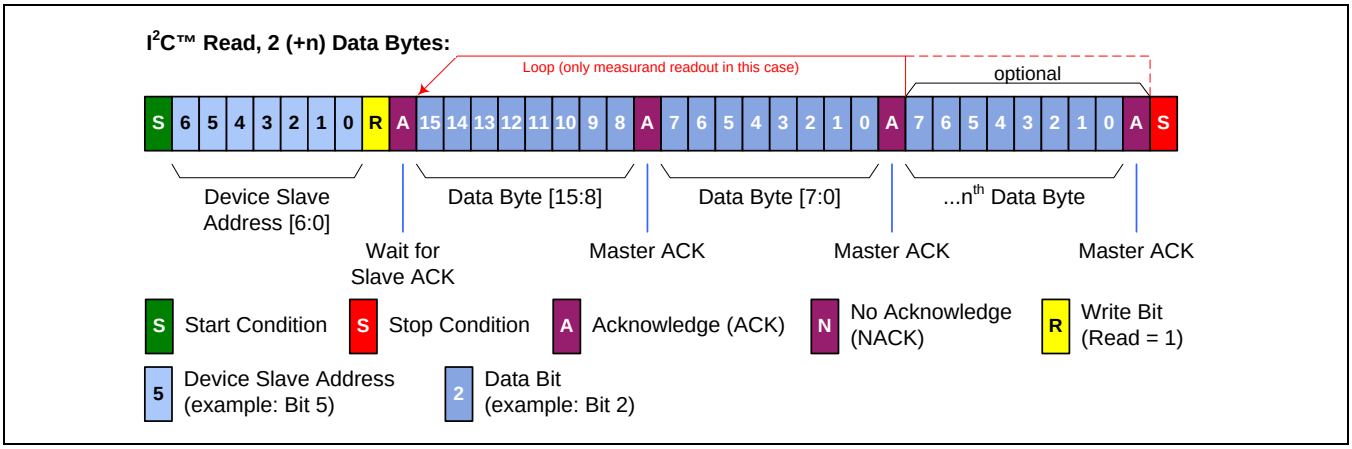


Figure 4.5 I²C™ – Timing Protocol

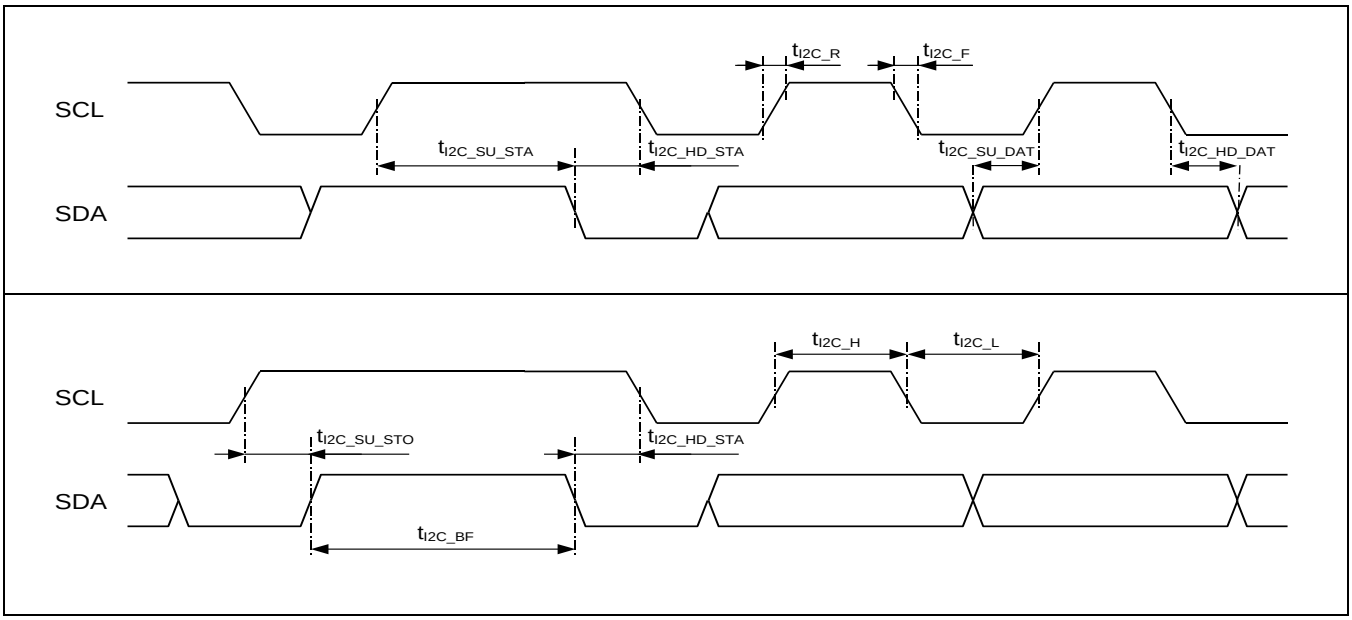


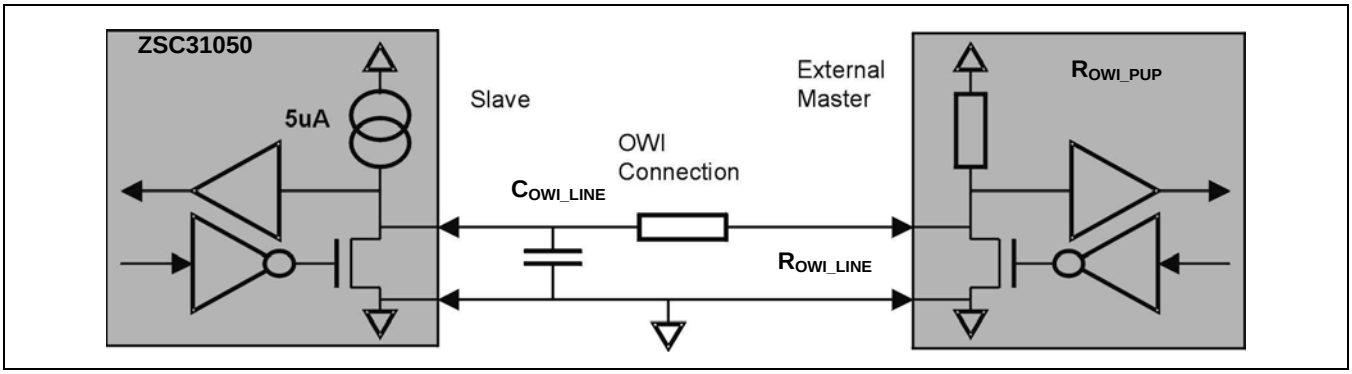
Table 4.1 Timing I²C™ Protocol

Nr.	Parameter	Symbol	min	typ	Max	Unit	Conditions
1	SCL clock frequency *	f_{SCL}			400	kHz	f_{OSC} ≥ 2MHz
2	Bus free time between start and stop condition	t_{I2C_BF}	1.3			µs	
3	Hold time start condition	$t_{I2C\_HD\_STA}$	0.6			µs	
4	Setup time repeated start condition	$t_{I2C\_SU\_STA}$	0.6			µs	
5	Low period SCL/SDA	t_{I2C_L}	1.3			µs	
6	High period SCL/SDA	t_{I2C_H}	0.6			µs	
7	Data hold time	$t_{I2C\_HD\_DAT}$	0			µs	
8	Data setup time	$t_{I2C\_SU\_DAT}$	0.1			µs	
9	Rise time SCL/SDA	t_{I2C_R}			0.3	µs	
10	Fall time SCL/SDA	t_{I2C_F}			0.3	µs	
11	Setup time stop condition	$t_{I2C\_SU\_STO}$	0.6			µs	
12	Noise interception SDA/SCL	t_{I2C_NI}			50	ns	Spike suppression

4.3. Digital One Wire Interface (OWI)

The ZSC31050 employs IDT's OWI one-wire digital interface. It combines a simple and easy protocol adaptation with a cost-saving pin sharing. Both the analog voltage output and this digital interface (calibration and/or digital output value) occur over the same pin. An advantage of IDT's OWI output signal capability is that it enables "end of line" calibration – no additional pins are required to digitally calibrate a finished assembly.

Figure 4.6 Block Schematic of the OWI connection



* Internal clock frequency f_{CLK} must be a minimum of 5 times higher than communication clock frequency.

Both devices are peers, however only the external device starts communication and requests data; in this sense it is referred to as master and the ZSC31050 as slave. The OWI interface is primarily intended for calibration use although the calibrated output signal is also available via this interface.

4.3.1. Properties and Parameters

Though OWI protocol is designed as bilateral protocol, it is necessary for reasons of compatibility to use an address in the communication. After the start condition, the master must send an address, consisting of a 7-bit slave address and a read/write–bit (0 = write, 1 = read). The slave address is part of the protocol and must be sent ***but will not be evaluated for communication at the ZSC31050***.

Table 4.2 OWI Interface Parameters – Worst Case Parameterization

Nr.	Parameter	Symbol		Unit	Conditions
1	Pull-up resistance master	R_{OWI_PU}	330	Ω	Refer to the *ZSC31050 Data Sheet,* section 1.5.2 for a detailed description of specifications.
2	OWI line resistance	R_{OWI_LINE}	20	Ω	
3	OWI load capacitance	C_{OWI_LOAD}	4.7	nF	

4.3.2. Initializing OWI Communication

There are two options for starting one-wire communication.

- The ZSC31050 opens a 20ms time window after power-on; i.e., the one-wire start window. If in this time window, one-wire communication is detected, the device stays in the one-wire mode until this is closed by sending a specific command. If no one-wire communication occurs in the start window, the interface leaves the one-wire mode and changes to the configured interface mode: I²C™ or SPI as programmed in EEPROM. The one-wire start window can be suppressed by configuration (CFGSIF:OWIWIND = 1) if no access via one-wire communication is desired.
- The ZSC31050 can be configured by EEPROM programming so that OWI is also enabled in NOM during the measurement cycle (CFGSIF:OWIWIND = 0 and CFGSIF:OWIE = 1). Then it is possible to read out the actual conditioning results for measurand and temperature via one-wire communication (OUT pin); the analog voltage output is disabled.

4.3.3. OWI Protocol

The OWI protocol used is defined as follows:

- **Idle period**
  During inactivity of the bus, the OWI line is pulled-up to supply voltage VDDA.
- **Start condition**
  When the OWI line is in idle mode, a low pulse (return to high) with a minimum width of 10µs indicates a start condition. Every command must be initiated by a start condition sent by a master. A master can generate a start condition only when the OWI line is in idle mode.
- **Stop condition**
  The master finishes a transmission by changing back to the high level (idle mode). Every command (referred to as a “write operation”) must be closed by a stop condition to start processing the command. The master can interrupt a sending slave after a data request (referred to as a “read operation”) by clamping the OWI line to the low level for generating a stop condition.

No transition from low-to-high or from high-to-low (constant level) at OWI line for at least twice the period of the last transmitted valid bit indicates a stop condition. A stop condition without considering the last bit-time (secure stop condition) is generated at a constant level at the OWI line for more than 510 clocks of the internal clock oscillator.

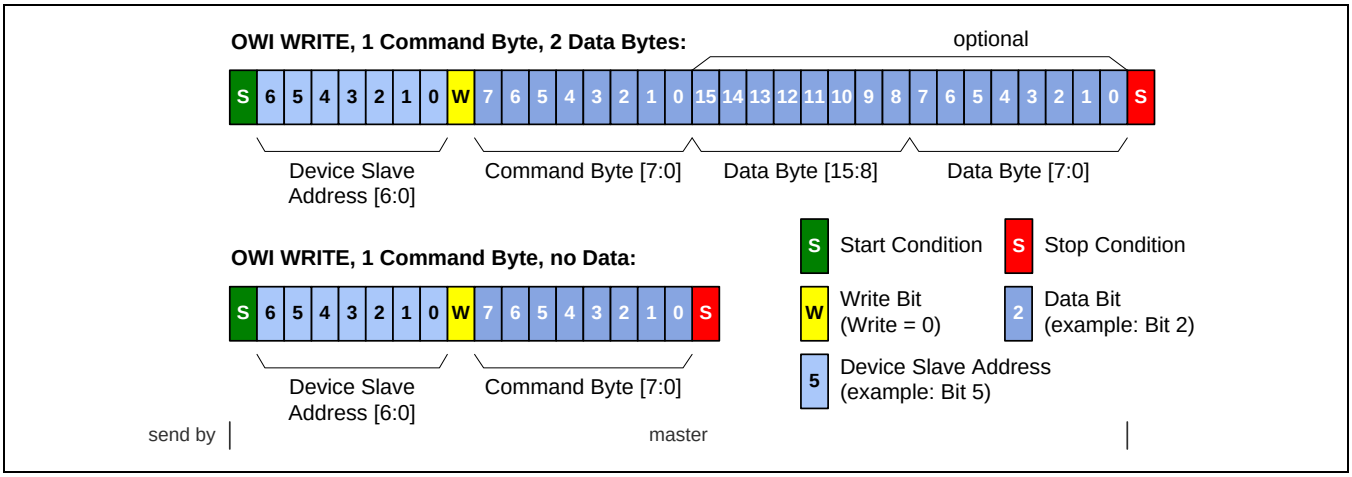
- **Valid data**
  Data is transmitted in bytes (8 bits) starting with the most significant bit (MSB); 16 bit data words are transmitted beginning with high byte first (i.e., “Big Endian”). Transmitted bits are recognized after a start condition at every transition from low-to-high at the OWI line. The value of the transmitted bit depends on the duty ratio between the high phase and high/low period (bit period, t_{OWI_BIT}). A duty ratio greater than 1/8 and less than 3/8 is detected as ‘0’; a duty ratio greater than 5/8 and less than 7/8 is detected as ‘1’.

  The bit period of consecutive bits must not change more than with a factor of 2 because the stop condition is detected in this case.

- **Addressing**
  Though the OWI protocol is designed as a bilateral protocol, it is necessary for reasons of compatibility to use an address in the communication. After the start condition, the master must send an address consisting of a 7-bit slave address and a read/write bit (0 = write, 1 = read). The slave address is part of the protocol and must be sent ***but will not be evaluated for communication at the ZSC31050***.

- **Write operation**
  During transmission from master to slave (WRITE), the address byte is followed by a command byte and, depending on the transmitted command, an optional two data bytes. The internal microprocessor evaluates the received command and processes the related routine. The following figure illustrates the write of a command with two data bytes and without data bytes. A detailed description of the command set is given in section 4.5.

Figure 4.7 OWI – Write Operation



- **Read operation**
  After a data request from the master to the slave by sending an address byte including a set-data-direction bit, the slave answers by sending data from the activated interface output registers. The slave generates the data bits with a bit period equal to the last received bit (R/W bit). The master must generate a stop condition after receiving the requested data.

  A data request is answered by the interface module itself and consequently does not interrupt the current process of the internal microprocessor.

The data in the activated registers is sent continuously until a stop condition is detected; after transmitting all available data the slave starts repeating the data.

During an active measurement cycle, data is continuously being updated with conditioning results. To get other data from the slave (e.g., EEPROM contents), usually a specific command must be sent before the data request to initiate the transfer of this data to the interface output registers. This command does interrupt the current process of the internal microcontroller and consequently also a running measurement cycle.

Figure 4.8 OWI – Read Operation - Data Request

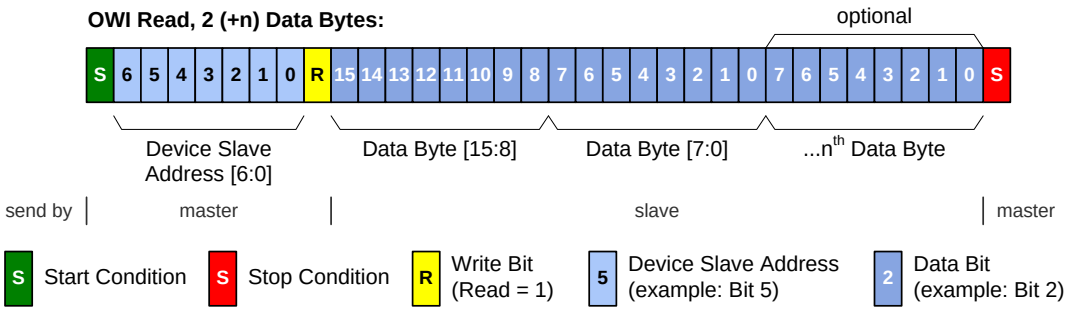


Figure 4.9 OWI – Timing Protocol

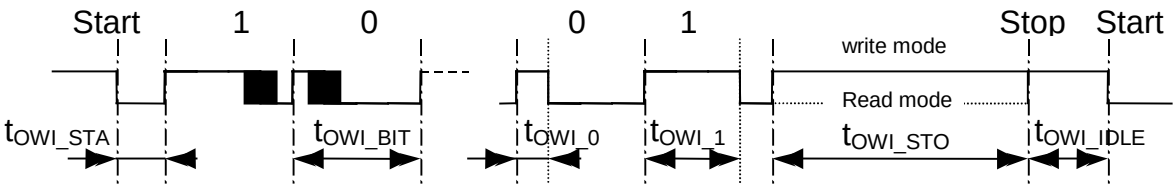


Table 4.3 OWI Timing Protocol

Nr.	Parameter	Symbol	min	typ	max	Unit	Conditions
1	Bus free time between start and stop condition	t_{OWI_IDLE}	10			µs	
2	Hold time start condition	t_{OWI_STA}	10			µs	
3	Bit period	t_{OWI_BIT}	20		100	µs	
4	Duty ratio bit ‘0’	t_{OWI_0}	0.125	0.25	0.375	t_{OWI_BIT}	
5	Duty ratio bit ‘1’	t_{OWI_1}	0.625	0.75	0.875	t_{OWI_BIT}	
6	Hold time stop condition	t_{OWI_STO}	2.0	250		$t_{OWI\_BIT\_L}$ µs	$t_{OWI\_BIT\_L}$ is the bit period of the last valid bit
7	Bit period deviation	$t_{OWI\_BIT\_DEV}$	0.75	1.0	1.25	t_{OWI_BIT}	

4.3.4. Using the OWI-Interface

For OWI communication, the analog output pin OUT is used; as a result, OWI enables end-of-line calibration, which offers an inexpensive and powerful overall sensor module calibration at the end of the manufacturing process. Although the OWI is designed primarily for calibration, it can also be used to digitally read out the calibrated sensor signal continuously.

These two communication tasks are supported in different configurations of the interface.

- **"OWI-start-window" for calibration only**
  In this mode, the ZSC31050 listens during the first 20ms after power-on for communication. To open the communication, the START_CM command including the slave address must be sent. After that, the output pin remains in the digital interface mode until the command START_CYCL_RAM / EEP or after power-on. The window can be suppressed by setting the lock bit "OWIWind" in EEPROM register $23/17_{HEX}$. But this should only be done as the last step of calibration (because reactivating of this window is then only possible via I²C™).
- **"OWI Continuous Mode" for calibration and for digital read out**
  Activate the OWI mode via the start window as described above and enable the "OWI for NOM" bit (OWIE-> "OWI Continuous Mode") with the write command to EEPROM register $23/17_{HEX}$. It is now possible to use the OWI interface for calibration and also for digital readout. The configuration for the read out is determined in the configuration word CFGSIF (EEPROM register $23/17_{HEX}$) with the SIFOUTP / SIFOUTT1 / SIFOUTT2 bits. The request for the desired output values (P, T1, T2) is a read command to the slave address (e.g., send $F1_{HEX}$ to the slave address 78_{HEX}). Depending on the configuration, the ZSC31050 sends the measurand value for the first request and for the next, the T1 value (if configured), followed by the T2 value (if configured), and then it starts again with the measurand. The master must generate a stop condition after receiving the requested data.

4.3.5. Using OWI with the ZSC31050 Evaluation Kit and its Software

The ZSC31050 Evaluation Kit and its software can be used to configure and activate one-wire communication via OWI. Refer to the *ZSC31050 Evaluation Kit Description* for more details and recommendations.

4.4. Synchronous Serial Peripheral Interface (SPI) Introduction

Using the SPI interface of the ZSC31050 requires a special configuration in EEPROM to activate this communication protocol, which is also different from the default configuration. It is necessary to have I²C™ or OWI communication access to the ZSC31050 to write the SPI configuration into EEPROM. There is no I²C™ or OWI communication possible if SPI configuration is written into EEPROM and activated.

During an SPI transfer, data is simultaneously transmitted (shifted out serially) and received (shifted in serially). A serial clock line synchronizes shifting and sampling of the information on the two serial data lines. A slave select line allows individual selection of a slave SPI device; slave devices that are not selected do not interfere with SPI bus activities. The ZSC31050's SPI slave interface supports all combinations of clock phase (CPHA) and polarity (CPOL). Slave CPOL and CPHA must be programmed to master adjustments before the beginning of transmission. RAM/EEPROM register 17_{HEX} (refer to Table 5.3) contains the initialization settings for the SPI interface:

SFGSIF: SIFMD = Interface mode SPI or I²C™

SFGSIF: SPICKP => Clock polarity CPOL

SFGSIF: SPICKE => Clock phase CPHA

Data is transmitted in bytes (8 bits) starting with the most significant bit (MSB), 16 bit data words are transmitted beginning with high byte first (i.e., "Big Endian").

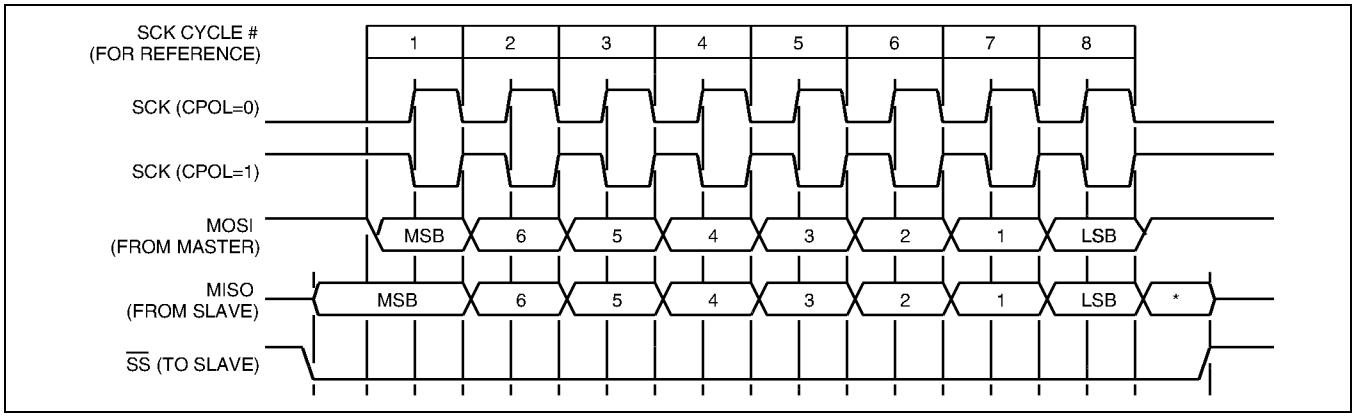
4.4.1. SPI Clock Phase and Polarity Controls

Software can select any of four combinations of the serial clock (SCK) phase and polarity using two bits in the SPI control register (SPCR). The clock polarity is specified by the CPOL control bit, which selects an active high or active low clock and has no significant effect on the transfer format. The clock phase (CPHA) control bit selects one of two fundamentally different transfer formats.

4.4.1.1. Transfer Format When CPHA Equals Zero

Figure 4.10 shows a timing diagram of an SPI transfer where CPHA is zero. Two waveforms are shown for SCK: one for CPOL equals zero and another for CPOL equals one. The diagram may be interpreted as a master or slave timing diagram since the SCK, master-in/slave-out (MISO), and master-out/slave-in (MOSI) pins are directly connected between the master and the slave. The MISO signal is the output from the slave, and the MOSI signals the output from the master. The /SS line is the slave select input to the slave.

Figure 4.10 SPI Transfer Format When CPHA Equals Zero – Principle Transfer Illustration

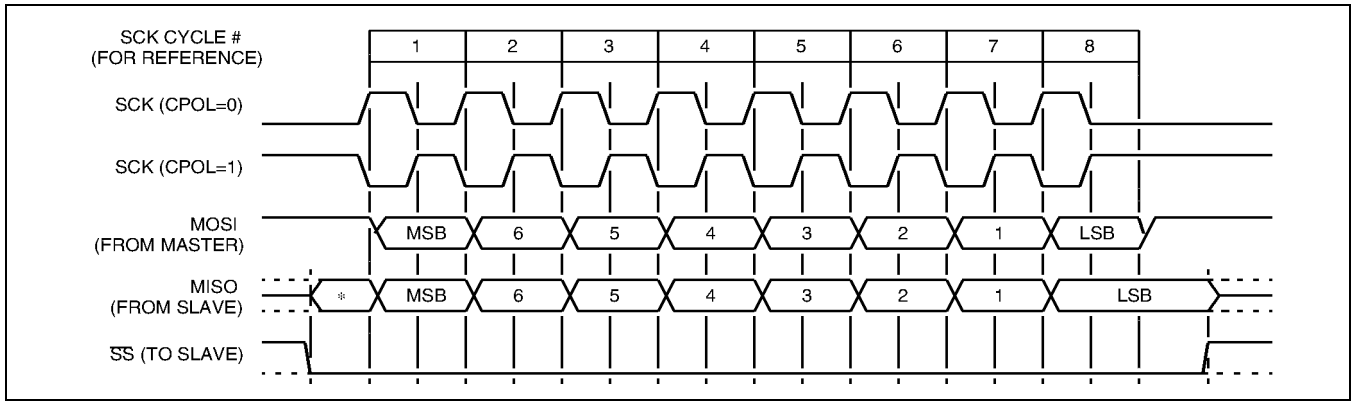


When CPHA equals one, the /SS line may remain active low between successive transfers (can be tied low at all times). This format is sometimes preferred in systems having a single fixed master and a single slave driving the MISO data line.

4.4.1.2. Transfer Format CPHA Equals One

Figure 4.11 shows a timing diagram of an SPI transfer where CPHA is one. Two waveforms are shown for SCK: one for CPOL equals zero and another for CPOL equals one. The diagram may be interpreted as a master or slave timing diagram since the SCK, MISO, and MOSI pins are directly connected between the master and the slave. The MISO signal is the output from the slave, and the MOSI signal is the output from the master. The /SS line is the slave select input to the slave.

Figure 4.11 SPI Transfer Format When CPHA Equals One – Principle Transfer Illustration



When CPHA equals zero, the /SS line must be negated and reasserted between each successive serial byte.

When CPHA equals one, the /SS line may remain active low between successive transfers (can be tied low at all times). This format is sometimes preferred in systems having a single fixed master and a single slave driving the MISO data line.

4.4.2. SPI Pin Signals

There are four I/O pin signals associated with SPI transfers: the SCK, the MISO data line, the MOSI data line, and the active low /SS pin. When the master initiates a transfer, eight clock cycles are automatically generated on the SCK pin. The SCK pin is an input and the clock signal from the master synchronizes the data transfer between the master and slave devices. Slave devices ignore the SCK signal unless the /SS pin is active low. In both the master and slave SPI devices, data is shifted on one edge of the SCK signal and is sampled on the opposite edge where data is stable. Edge polarity is determined by the SPI transfer protocol.

The MISO and MOSI data pins are used for transmitting and receiving serial data. At the slave, MOSI is the data input line and MISO is the data output line. As an option, one slave device selected by the master can drive data out its MISO pin to the MISO master pin. The automatic control of the direction of these pins makes reconfiguration through external logic unnecessary when a new device becomes the master.

The /SS pin behaves differently on master and slave devices. On a slave device, this pin is used to enable the SPI slave for a transfer. If the /SS pin of a slave is inactive (high), the device ignores SCK clocks and keeps the MISO output pin in the high-impedance state.

4.4.3. Beginning and Ending SPI Transfers

A transfer includes the eight SCK cycles plus an initiation period at the beginning and ending period of the transfer. The details of the beginning and ending periods depend on the CPHA format selected and whether the SPI is configured as a master or a slave. The initiation delay period is also affected by the SPI clock rate selection when the SPI is configured as a master.

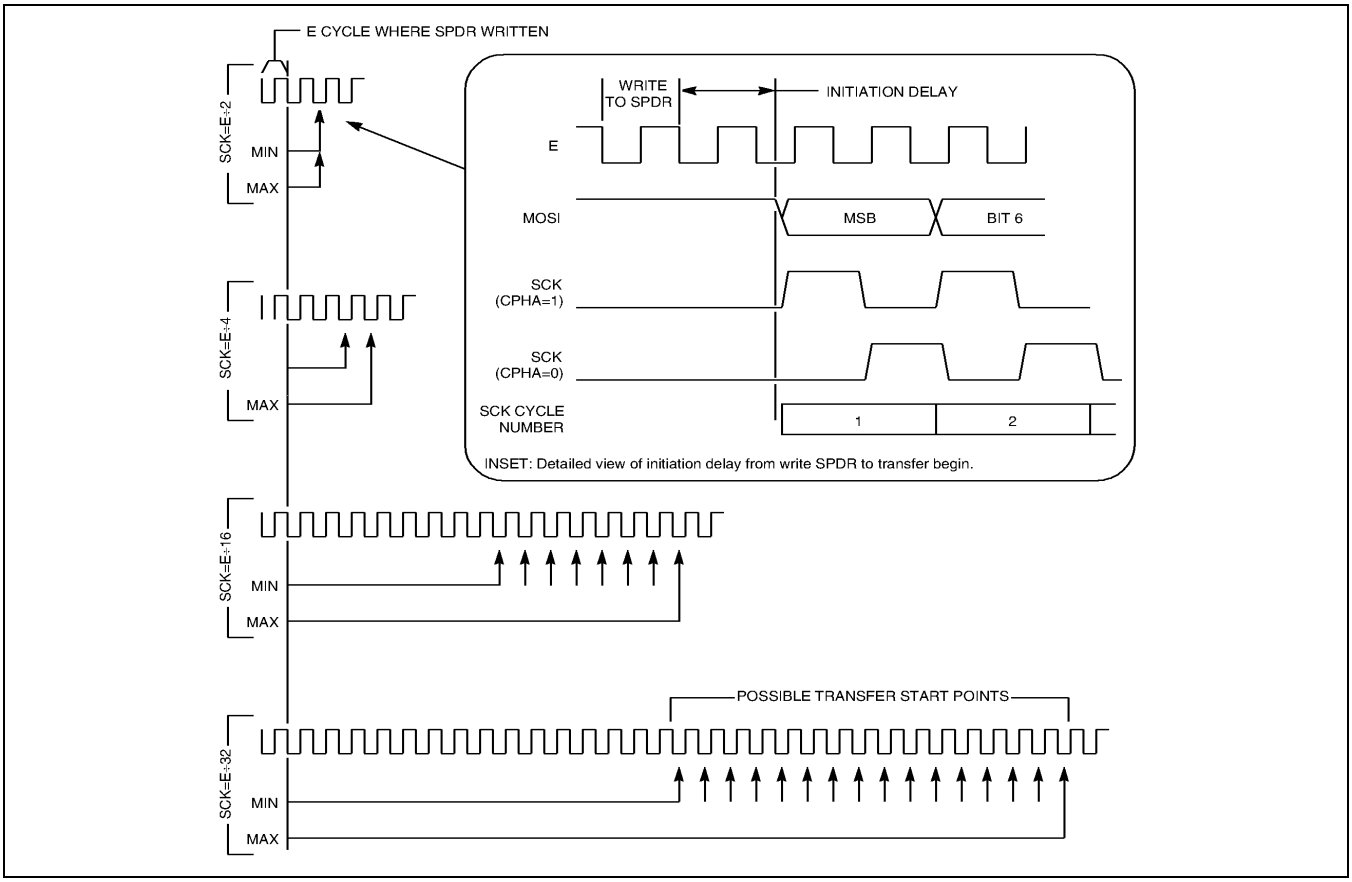
It might be useful to refer to the transfer format illustrated in Figure 4.10 and Figure 4.11 to understand how the beginning and ending details fit into a complete transfer operation.

4.4.4. Transfer Beginning Period (Initiation Delay)

All SPI transfers are started and controlled by a master SPI device. For a slave, the transfer begins with the first SCK edge or the falling edge of /SS, depending on the CPHA format selected. When CPHA equals zero, the falling edge of /SS indicates the beginning of a transfer. When CPHA equals one, the first edge on the SCK indicates the start of the transfer. In either CPHA format, a transfer can be aborted by taking the /SS line high, which causes the SPI slave logic and bit counters to be reset. The SCK rate selected has no effect on slave operations since the clock from the master is controlling transfers.

CPHA has no effect on the delay until the start of the transfer, but it does affect the initial state of the SCK signal. When CPHA equals zero, the SCK signal remains inactive for the first half of the first SCK cycle. When CPHA equals one, the first SCK cycle begins with an edge on the SCK line from its inactive to its active level. The SPI clock rate (selected by SPR[1:0]) affects the delay from the write to SPDR and the start of the SPI transfer (see Figure 4.12). The internal SPI clock in the master is a free-running derivative of the internal MCU clock. Since the SPI clock is free-running, there is an uncertainty about when the write-operation to the SPI data register (SPDR) will occur relative to the slower SCK. This uncertainty causes the variation in the initiation delay shown in Figure 4.12.

Figure 4.12 Delay from Write SPDR to Transfer Start (Master)

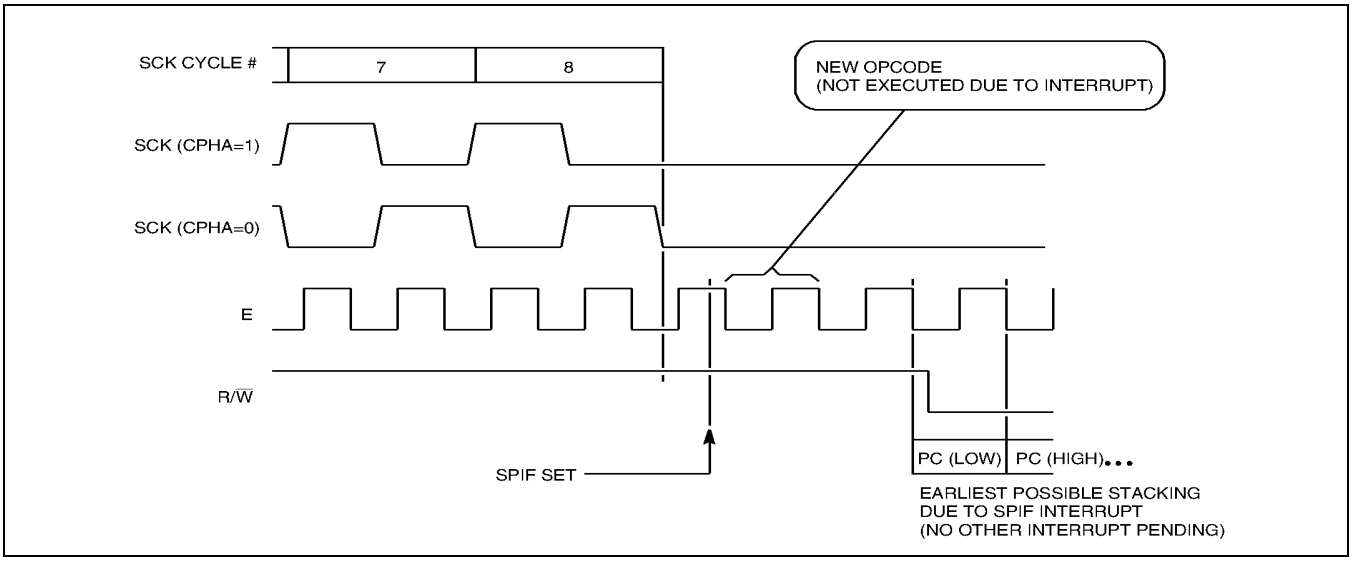


4.4.5. Transfer Ending Period

An SPI transfer is technically complete when the SPIF flag is set, but depending on the configuration of the SPI system, there may be additional tasks. Because the SPI bit rate does not affect timing of the ending period, only the fastest rate will be considered in discussions of the ending period.

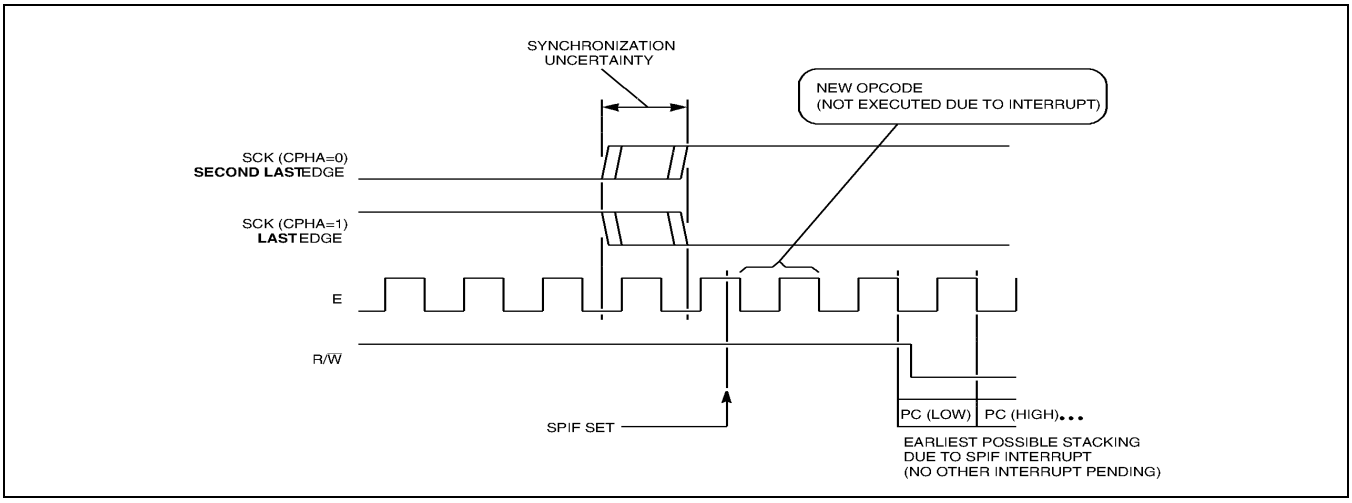
When the SPI is configured as a master, SPIF is set at the end of the eighth SCK cycle. When CPHA equals one, SCK is inactive for the last half of the eighth SCK cycle. Figure 4.13 shows the transfer-ending period for a master. The SCK waveforms in this figure show only the CPOL equals zero case, since clock polarity does not affect timing of the ending period.

Figure 4.13 Transfer Ending for an SPI Master



When the SPI is operating as a slave, the ending period is different because the SCK line can be asynchronous to the MCU clocks of the slave and because the slave does not have access to as much information about SCK cycles as the master. For example, when CPHA equals one, where the last SCK edge occurs in the middle of the eighth SCK cycle, the slave cannot know when the end of the last SCK cycle is. For these reasons, the slave considers the transfer complete after the last bit of serial data has been sampled, which corresponds to the middle of the eighth SCK cycle. A synchronization delay is required so the setting of the SPIF flag is properly positioned relative to the internal clock of the slave. Figure 4.14 shows the ending period for a slave. The SCK waveforms in this figure show only the CPOL equals zero case, since clock polarity does not affect timing of the ending period.

Figure 4.14 Transfer Ending for an SPI Slave



When CPHA equals zero, there is a potential problem that can be avoided by proper software, but it is sometimes overlooked. The SPIF flag is set at the end of a transfer, but the slave is not permitted to write new data to the SPDR while the /SS line is still low. If the master device is busy, the /SS line to the slave can remain low longer than the slave expects.

4.4.6. SPI Interface Parameters

Table 4.4 Timing SPI Protocol

Nr.	Parameter	Symbol	Min	Typ	Max	Unit	Conditions
1	SCK to internal clock frequency ratio	f_{SCK_CLK}			$f_{CLK}/5$		f_{SCK} must be 5 times smaller than f_{CLK}
2	MISO hold time after SCK sample slope	$t_{SPI\_HD\_MISO}$	200			ns	
3	MOSI setup time before SCK sample slope	$t_{SPI\_SU\_MISO}$	$2/f_{CLK}$				
4	/SS setup time before SCK sample slope	$t_{SPI\_SU\_SS}$	10			ns	
5	/SS hold time after SCK sample clk [1)]	$t_{SPI\_HD\_SS}$	$1/ f_{SCK\_CLK}$				

1) The minimum is required in order to guarantee that the CMC receives the data from the SPI interface.

4.5. Interface Commands

All implemented commands are available in all communication modes: I²C™, SPI and ZACwire™ (OWI). A received valid command interrupts the internal microcontroller and initiates the processing of a command routine.

During command processing time, the digital serial interface (SIF) is disabled and received commands are ignored. The processing time depends on the internal system clock frequency, which is usually 2MHz but is selectable by EEPROM programming. The commands are divided into two sets with different validity. Commands that change the configuration of the device are ignored in NOM and are available only after changing to CM.

***Table 4.5 Restricted Command Set for Serial Digital Interface** – Commands are always valid*

Command (HEX)	Data	Command	Notes	Processing Time System clock 2MHz
01		START_CYC_EEP	Start measurement cycle including initialization from EEPROM [1)]	350µs
02		START_CYC_RAM	Start measurement cycle including initialization from RAM [1)]	220µs
10 to 1F		READ_RAM0	Read data from RAM address 00 to 0F Writes data from RAM to SIF Output Registers Usually followed by Read operation	50µs
20 to 2F		READ_RAM1	Read data from RAM address 10 to 1F Writes data from RAM to SIF Output Register Usually followed by Read operation	50µs
30 to 3F		READ_EEP0	Read data from EEPROM address 00 to 0F Writes data from EEPROM to SIF Output Register Usually followed by Read operation	50µs
40 to 4F		READ_EEP1	Read data from EEPROM address 10 to 1F Writes data from EEPROM to SIF Output Register Usually followed by Read operation	50µs
Note: 5x commands do not change the EEPROM or RAM configuration. They are used for communication to devices with unknown configuration.				
50		CFG_SIF_TO_OWI	Configure SIF to Communication Mode OWI	50µs
51 55 59 5D		CFG_SIF_TO_SPI	Configure SIF to Communication Mode SPI 51: SET_SIF_2_SPI SPI (CKE = 0, CKP = 0) 55: SET_SIF_2_SPI SPI (CKE = 0, CKP = 1) 59: SET_SIF_2_SPI SPI (CKE = 1, CKP = 0) 5D: SET_SIF_2_SPI SPI (CKE = 1, CKP = 1)	50µs
52		CFG_SIF_TO_I2C	Configure SIF to Communication Mode I²C™	
60	2 Byte	SET_DAC	Set output DAC to value defined by data bytes [0 to $7FF_{HEX}$] The AOUT pin goes into tri-state for 40µs during processing. Note: Only applicable for SPI and I²C™ communication mode. In OWI mode, use the limit registers 8_{HEX} and 9_{HEX} followed by command 02_{HEX} for the same functionality.	100µs
70		START_OM	Start Open Mode **Note**: In Open Mode the command set is restricted! Change to Command Mode is possible	50µs
71		START_NOM	Start Normal Operation Mode (NOM) In Normal Operation Mode, the command set is restricted! Change to Command Mode or Open Mode is NOT possible	
72		START_CM	Start Command Mode (CM) Complete command set! Change to Open Mode or Normal Operation Mode is possible	

1) The measurement task starts after this time. For detailed information about output update rate and startup time, refer to section 1.3.1 and 1.4 of the *ZSC31050 Data Sheet* and to *ZSC31050_Bandwidth_Calculation_Rev_X_xy.xls*.

Table 4.6 Additional Command Set for Serial Digital Interface

Command (HEX)	Data	Command	Notes	Processing Time System clock 2MHz / EEPROM-Progr. Steps
80 to 8F	2 Byte	WRITE_RAM0	Write data to RAM address 00 to 0F	50µs
90 to 9F	2 Byte	WRITE_RAM1	Write data to RAM address 10 to 1F	50µs
A0 to AF	2 Byte	WRITE_EEP0	Write data to EEPROM address 00 to 0F	12.5ms / 1
B0 to BF	2 Byte	WRITE_EEP1	Write data to EEPROM address 10 to 1F	12.5ms / 1
C0		COPY_EEP2RAM	Copy contents of EEPROM to RAM Restores EEPROM Configuration in RAM	130µs
C3		COPY_RAM2EEP	Copy contents of RAM to EEPROM Stores RAM Configuration to EEPROM (signature is copied without checking!!!)	400ms / 32
C8		GET_EEP_SIGN	Calculates EEPROM signature and outputs it to SIF Out Register #1	150µs
C9		GEN_EEP_SIGN	GET_EEP_SIGN + write the signature to EEPROM address $1D_{HEX}$	12.6ms / 1
CA		GET_RAM_SIGN	Calculates RAM signature and outputs it to SIF Out Register #1	150µs
CB		GEN_RAM_SIGN	GET_RAM_SIGN + write the signature to RAM address $1D_{HEX}$	150µs
CC		CLEAR_EEP	Clear EEPROM Sets complete EEPROM to 0000_{HEX}	12.5ms / 1
CF		ROM_VERSION	Output Hardware & ROM version to SIF Out Register #1 • Design revision is defined by the high byte CF_{HEX} command answer • ROM version is defined by the low byte CF_{HEX} command answer Example: ZSC31050D=$0C02_{HEX}$	50µs
All “Dx” commands are used for the calibration process, write raw conversion results to SIF Output Registers, and do not affect the analog output				
D0		START_AD_P	“P”: Start cyclic A/D conversion at measurand channel (P)	50µs + A/D conversion time
D1		START_AD_T1	“T1”: Start cyclic A/D conversion at Temperature T1 channel	
D2		START_AD_T2	“T2”: Start cyclic A/D conversion at Temperature T2 channel	
D4		START_AD_PAZ	“PAZ”: Start cyclic A/D conversion at measurand auto-zero (PAZ) channel	
D5		START_AD_TAZ1	“T1AZ”: Start cyclic A/D conversion at Auto-Zero Temp (TAZ1) channel	
D6		START_AD_TAZ2	“T2AZ”: Start cyclic A/D conversion at Auto-Zero Temp (TAZ2) channel	
D8		START_AD_P_AZC	“P_AZC”: Start cyclic A/D conversion for measurand including Auto-Zero-Correction	
D9		START_AD_T1_AZC	“T1_AZC”: Start cyclic A/D conversion for Temperature T1 including Auto-Zero-Correction	
DA		START_AD_T2_AZC	“T2_AZC”: Start cyclic A/D conversion for Temperature T2 including Auto-Zero-Correction	
DB		START_AD_CMV_AZC	“CMV_AZC”: Start cyclic A/D conversion at Common Mode Voltage (CMV) channel including Auto-Zero-Correction (T1AZ)	

5 EEPROM and RAM

5.1. Programming the EEPROM

Programming the EEPROM is done using an internal charge pump to generate the required programming voltage. The timing of the programming pulses is controlled internally. The programming time for a write operation is 12.5ms on the condition that the system clock is adjusted. The programming time varies for each part due to the tolerances of the system clock frequency. Thus a programming time of 20 ms for a write operation is long enough to program all parts successfully.

The programming of the EEPROM is done via the serial digital interface by sending specific commands (refer to section 4.3.4). The commands WRITE_EEP0 / WRITE_EEP1 include the address of the EEPROM word and are followed by the two data bytes. There is also the command CLEAR_EEP that sets the whole EEPROM to zero. During programming, the EEPROM the serial digital interface is disabled so that no commands can be received. In I²C™ mode, no acknowledges would be generated from a slave ZSC31050.

The additional command COPY_RAM2EEP writes the contents of the RAM area where EEPROM contents are mirrored back to the EEPROM. This is to simplify the calibration process when the ZSC31050 is configured iteratively. This copy operation includes 32 write operations and requires therefore typically 400ms.

Because programming the EEPROM (write, clear, copy RAM to EEPROM) changes the configuration of the device, this action is only allowed in CM (start with START_CM as the first command after power on).

5.2. EEPROM and RAM Contents

The configuration of the ZSC31050 is determined by EEPROM programming. There are 22 calibration constants for conditioning the sensor signal via the conditioning calculation, 7 configuration words for setting the configuration regarding the application, 1 CRC for checking the validity of EEPROM contents, and 2 additional 16-bit words for arbitrary free user data.

After every power-on, the EEPROM contents are mirrored once to the RAM to avoid frequent access to EEPROM during normal operation. During this read-out and only at that point, the CRC is checked. If EEPROM contents are correct, the sum of all EEPROM words including the CRC and excluding the free user data is $FFFF_{HEX}$ (calculation with overflow). If a CRC error is detected, the ZSC31050 starts in its reset configuration, opens the time window for one-wire communication (ZACwire™ (OWI) mode) and then sets the digital serial interface open for I²C™ and SPI (Open Mode).

The configuration of the device is determined by values read from the configuration words stored in the mirrored memory area in RAM and then stored into internal registers. The calibration constants are used for the digital conditioning calculation and are also read from RAM, so every change to this RAM area effects the configuration and behavior of the device. After power-on, the contents of the RAM are determined by EEPROM contents and can then be changed by specific commands writing to RAM. This new configuration is activated by the command START_CYC_RAM.

Table 5.1 EEPROM & RAM Contents

Register#/ RAM-Addr (hex)	Write Command RAM/EEP (hex)	Default (hex)	Description
Conditioning coefficients - Correction formula for measurand (see section 2.3)			
0	80/A0	800	c_0 - Offset
1	81/A1	2000	c_1 - Gain
2	82/A2	0	c_2 - Non-linearity 2nd order
3	83/A3	0	c_3 - Non-linearity 3rd order
4	84/A4	0	c_4 - Temperature coefficient Bridge Offset 1st order
5	85/A5	0	c_5 - Temperature coefficient Bridge Offset 2nd order
6	86/A6	0	c_6 - Temperature coefficient Gain 1st order
7	87/A7	0	c_7 - Temperature coefficient Gain 2nd order
Conditioning coefficients – Limit the output at OUT pin (see section 2.4)			
8	88/A8	0	l_{min} - Lower Limit with reference to pin OUT for voltage, current or PWM output
9	89/A9	7FF	l_{max} - Upper Limit with reference to pin OUT for voltage, current or PWM output
Conditioning coefficients - Correction formula for temperature (see section 2.3)			
A	8A/AA	1000	t_{10} - Offset Temperature 1
B	8B/AB	2000	t_{11} - Gain Temperature 1
C	8C/AC	0	t_{12} - Non-linearity 2nd order Temperature 1
D	8D/AD	1000	t_{20} - Offset Temperature 2
E	8E/AE	2000	t_{21} - Gain Temperature 2
F	8F/AF	0	t_{22} - Non-linearity 2nd order Temperature 2
Conditioning coefficients – Limit the output at IO1 and IO2 pins (see section 2.4)			
10	90/B0	0	Alarm 1: Threshold PWM1 : Lower Limit
11	91/B1	1FF	Alarm 1: Hysteresis PWM1 : Upper Limit
12	92/B2	0	Alarm 1: On-/Off-delay (two 8 bit values)
13	93/B3	0	Alarm 2: Threshold Common-mode voltage : Lower Limit
14	94/B4	FFFF	Alarm 2: Hysteresis Common-mode voltage : Upper Limit
15	95/B5	0	Alarm 2: On-/Off-delay (two 8 bit values)

Register#/ RAM-Addr (hex)	Write Command RAM/EEP (hex)	Default (hex)	Description
Configuration words (see section 5.3)			
16	96/B6	48	CFGCYC: Configuration of measurement cycle
17	97/B7	34	CFGSIF: Configuration of digital serial interface
18	98/B8	7625	CFGAPP: Configuration of target application
19	99/B9	9800	CFGAFE: Configuration of analog front end
1A	9A/BA	0124	CFGTMP: Configuration of temperature measurement
1B	9B/BB	8060	CFGOUT: Configuration of signal outputs
1C	9C/BC	9248	ADJREF: Adjustment of internal references
CRC			
1D	9D/BD	15BD	Signature
User free memory			
1E 1F	9E/BE 9F/BF	- -	Free user memory, not included in Signature Free user memory, not included in Signature

5.3. EEPROM and RAM Configuration Words

The configuration words are stored in RAM and EEPROM at addresses 16_{HEX} to $1C_{HEX}$ and determine the various modes of the ZSC31050. The following tables explain these configuration words.

Table 5.2 Configuration Word CFGCYC

Bit	IC-default	CFGCYC - Configuration of measurement cycle	EEPROM/RAM address 16_{HEX}
15:10	0000 00	Not used	-
9:7	00 0	Count of bridge measurements per cycle Count npmc of bridge measurements between two special measurements (e.g., temperature, auto-zero measurement) npmc = 2^{PMC} = 1, 2, 4, 8, 16, 32, 64, 128	PMC
6:5	10	Access port IO1 (output 2) Output of result via port IO1 for 0x: Measurand 10: Temperature 1 11: Temperature 2 Active only if CFGOUT:PMIO1 = 10 (PWM output at port IO1).	ACOS2
4:3	01	Access port OUT (output 1) Output of result via port OUT for 0x: Measurand 10: Temperature 1 11: Temperature 2	ACOS1
2	0	Enable common-mode voltage measurement and check Measures common-mode voltage from bridge (VINP and VINN pins are shorted) and checks if the result is within the limits defined in EEPROM addresses 13_{HEX} and 14_{HEX}	CMVE
1	0	Enable temperature 2 measurement Includes the measurement of temperature 2 during measurement cycle. 0: disabled 1: enabled	T2E
0	0	Enable Start-up ROM check ROM check is done after power-on. Start-up time until first valid output increases by 10ms. 0: disable 1: enabled	ROMCHE

Table 5.3 Configuration Word CFGSIF

Bit	IC-default	CFGSIF - Configuration of digital serial interface (SIF)	EEPROM/RAM address 17_{HEX}
15:9	0000 000	Alternative I²C™ slave address Additional slave address for communication via digital serial interface if CFGSIF:SIFID2E = 1. The general slave address is 78_{HEX}. If enabled both addresses are valid.	SIFID2
8	0	Enable one-wire communication during measurement cycle Active only if CFGSIF:OWIWIND = 0 (enables start window for one wire communication). Allows the read-out of the conditioning results for pressure and temperature via one-wire communication.	OWIE
7	0	Disable start window for one-wire communication Suppresses the 20ms time window for starting one-wire communication after power-on and after restart the measurement cycle by sending the commands START_CYC_EEP or START_CYC_RAM	OWIWIND
6	0	Enable SIF output of conditioning result for temperature 2 Delivers a continuously updated 15-bit value of temperature 2 for read out during the measurement cycle via digital serial interface. 1)	SIFOUTT2
5	1	Enable SIF output of conditioning result for temperature 1 Delivers a continuously updated 15-bit value of temperature 1 for read out during the measurement cycle via digital serial interface. 1)	SIFOUTT1
4	1	Enable SIF output of conditioning result for measurand Delivers a continuously updated 15-bit value of measurand for read out during measurement cycle via digital serial interface. 1)	SIFOUTP
3	0	Enable alternative I²C™ slave address The alternative address CFGSIF:SIFID2 is only valid for I²C™!	SIFID2E
2	1	SPI clock edge select 0: sample leading edge 1: sample trailing edge	SPICKE
1	0	SPI clock polarity 0: SCK low, idle 1: SCK high, idle	SPICKP
0	0	SIF mode Chose active communication mode: 0: I²C™ communication 1: SPI communication	SIFMD

1) ***Important:*** Use caution if clearing the EEPROM – do not power off/on or restart the ZSC31050 after this. Clearing the EEPROM resets all the communication flags (CFGSIF:SIFOUTT2/SIFOUTT1/SIFOUTP) of the interface. If this is activated, no communication is possible. Reactivation is possible by sending the following commands 72_{HEX}, 52_{HEX}, $B70034_{HEX}$, $C9_{HEX}$, and 01_{HEX}.

Table 5.4 Configuration Word CFGAPP

Bit	IC-Default	CFGAPP - Configuration of target application EEPROM/RAM address 18_{HEX}	
15	0	Bridge Signal Polarity - Interchange of input signal (VINP and VINN pin) 0: positive ($V_{BR\_DIFF} = V_{BR\_P} – V_{BR\_N}$) 1: negative ($V_{BR\_DIFF} = V_{BR\_N} – V_{BR\_P}$)	BSP
14	1	*Not used – Set always to '1'*	
13:12	11	ADC Range Shift regarding signal from IN3 pin (temperature 2) Active only if CFGTMP:TAM2 = 11 (Measurement of T2 with a user-defined voltage via IN3 pin). 00: ADC Input Range = [(–1/16 V_{ADC_REF}) to (+15/16 V_{ADC_REF})] 01: ADC Input Range = [(–1/8 V_{ADC_REF}) to (+ 7/8 V_{ADC_REF})] 10: ADC Input Range = [(–1/4 V_{ADC_REF}) to (+ 3/4 V_{ADC_REF})] 11: ADC Input Range = [(–1/2 V_{ADC_REF}) to (+ 1/2 V_{ADC_REF})]	ADRAIN3
11:10	01	IN3 reference mode Active only if CFGTMP:TAM2 = 11 (Measurement of T2 with arbitrary voltage via pin IN3). Arbitrary voltage is measured referenced to: 00: Bandgap reference V_{BG} (approx. 1.23V) 01: Supply voltage VDDA / 2 1d: Supply voltage check (Measures VDDA / 2 referenced to V_{BG})	IN3M
9	1	Activate sensor connection and RAM (= configuration registers) parity check: 0: enabled 1: disabled	SCCD
8	0	Sensor bridge excitation mode: 0: Voltage supplied 1: Current supplied (constant current generated with internal regulator and external low-TC resistor) **Hint:** CFGAPP:XZCE=1 is required for CFGAPP:CSBE=1	CSBE
7	0	Enable e**X**tended **Z**ero **C**ompensation Offset compensation by analog front-end, also called AnalogZeroPointShift; value is defined with CFGAFE:XZC 0: disabled 1: enabled	XZCE
6:5	01	Raw oscillator frequency adjust Fine adjustment by ADJREF:OSCA 00: f_{CLK} = 1 MHz 10: f_{CLK} = 2 MHz 01: f_{CLK} = 2 MHz 11: f_{CLK} = 4 MHz	OSCF
4	0	Enable external clock 0: disabled 1: enabled	ECLKE
3	0	A/D converter reference voltage selection 0: ADC-Ref = VBR 1: ADC-ref = VDDA **Hint:** CFGAPP:XZCE=1 & CFGAFE:XZC=0 is required for CFGAPP:ADREF=1 & CFGAPP:CSBE=1	ADREF

Bit	IC-Default	CFGAPP - Configuration of target application EEPROM/RAM address 18_{HEX}	
2:1	10	Value of controlled analog supply voltage. 00: VDDA = 3.0 V 01: VDDA = 4.0 V 10: VDDA = 5.0 V 11: VDDA = 5.5 V	VDC
0	1	Enable analog supply voltage control. Uses internal controller with external transistor.	VDCE

Table 5.5 Configuration Word CFGAFE

Bit	IC-default	CFGAFE - Configuration of analog front end EEPROM/RAM address 19_{HEX}	
15:13	100	Resolution of A/D-conversion (r_{ADC}, see section 2.1) Valid for measurand as well as for temperature measurement. Influences conversion time and integration time of measurement. 000: 9 Bit 001: 10 Bit 010: 11 Bit 011: 12 Bit 100: 13 Bit 101: 14 Bit 11d: 15 Bit	RADC
12	1	Order of A/D-conversion Influences conversion time and integration time of measurement. 0: 1st order conversion 1: 2nd order conversion	OADC
11:10	10	ADC Range Shift regarding measurand signal (RS_{ADC}, see section 2.1) 00: ADC Input Range = [(–1/16 V_{ADC_REF}) to (+15/16 V_{ADC_REF})] 01: ADC Input Range = [(–1/8 V_{ADC_REF}) to (+ 7/8 V_{ADC_REF})] 10: ADC Input Range = [(–1/4 V_{ADC_REF}) to (+ 3/4 V_{ADC_REF})] 11: ADC Input Range = [(–1/2 V_{ADC_REF}) to (+ 1/2 V_{ADC_REF})]	ADRAPR
9 8:4	0 00000	e**X**tended**Z**ero**C**ompensation value (offset compensation by analog front end XZC_{IN}; refer to section 2.1 and to the *ZSC31050 Data Sheet,* section 2.3) CFGAFE<9>: “1” => positive, ”0” => negative; CFGAFE<8:4>: 0-31 Active only if CFGAPP:XZCE = 1. The width/value of an extended zero compensation step depends on the selected input span. Refer to section 2.1 for resulting value of offset cancellation.	XZC
3:0	0000	Gain analog front end measurand measurement (a_{IN_p}, refer to section 2.1) 0000: 420 0001: 280 0010: 210 0011: 140 0100: 105 0101: 70 0110: 52.5 0111: 35 1000: 26.25 1001: 14 1010: 9.3 1011: 7 11dd: 2.8	GAIN

Table 5.6 Configuration Word CFGTMP

Bit	IC-default	CFGTMP - Configuration of temperature measurement EEPROM/RAM address $1A_{HEX}$	
15:14	00	Gain analog front end temperature 2 meas. (a_{IN_T2}, see section 2.1) 00: GT4 (≈ 5.65) 10: GT2 (≈ 4.7) 01: GT3 (≈ 5.17) 11: GT1 (≈ 1.9) For details see section 6.	GAINT2
13:12	00	Gain analog front end temperature 1 meas. (a_{IN_T1}, see section 2.1) 00: GT4 (≈ 5.65) 10: GT2 (≈ 4.7) 01: GT3 (≈ 5.17) 11: GT1 (≈ 1.9) For details see section 6.	GAINT1
11	0	Polarity of external temperature sensor for temperature 2 measurement Active only if CFGAPP:TAD2 = 0 and CFGTMP:TAM2 ≠ 11 (enables temperature 2 measurement via TEMP pin). Switches polarity of supply current for temperature sensor. 0: Temperature sensor to VSS 1: Temperature sensor to VDDA	PETS2
10	0	Polarity of external temperature sensor for temperature 1 measurement Switches polarity of supply current for temperature sensor. 0: Temperature sensor to VSS 1: Temperature sensor to VDDA	PETS1
9:7	010	Temperature 2 (T2) zero-point adjust Allows shift of characteristics of temperature measurement. Refer to section 6 for details.	ZCT2
6:4	010	Temperature 1 (T1) zero-point adjust Allows shift of characteristics of temperature measurement. Refer to section 6 for details.	ZCT1
3:2	01	Temperature 2 (T2) acquisition mode Defines the used temperature sensor connected to pin IR_TEMP and implicit the input voltage range of temperature signal. 00: Internal diode 01: External diode 10: External resistor 11: External voltage Refer to section 6 for details.	TAM2
1:0	00	Temperature 1 (T1) acquisition mode Defines the used temperature sensor connected to pin IR_TEMP and implicit the input voltage range of temperature signal. 00: Internal diode 01: External diode 1d: External resistor Refer to section 6 for details.	TAM1

Table 5.7 Configuration Word CFGOUT

Bit	IC-default	CFGOUT - Configuration of signal outputs EEPROM/RAM address $1B_{HEX}$	
15:14	10	Resolution PWM output Active only if CFGOUT:PMIO1 = 10 or CFGOUT:COS1 = 10. Influences the PWM output frequency. 00: 9 Bit 10: 11 Bit 01: 10 Bit 11: 12 Bit	PWMRES
13:12	00	Clock divider PWM output regarding internal oscillator frequency Influences the PWM output frequency (see Table 3.3). 00: f_{CLK} / 1 10: f_{CLK} / 4 01: f_{CLK} / 2 11: f_{CLK} / 8	PWMD
11:10	00	Output polarity { PWM2 / PWM1 } at pin { OUT / IO1 } 0: PWM period starts with high level (high-active) 1: PWM period starts with low level (low active)	PWMPO
9	0	No access	
8	0	Clock divider for A/D converter Influences only the frequency for the A/D converter. Does not influence the internal working frequency. Set in connection with f_{CLK} = 4MHz (CFGAPP:OSCF = 11) to enlarge the processing time of the internal microcontroller when low resolution of less than or equal to 12-bit (CFGAFE:RADC = 0xx) is chosen. 0: f_{CLK} / 1 1: f_{CLK} / 2	VFCCLKD
7	0	Enable Alarm window mode Both thresholds and hysteresis (EEPROM addresses 10_{HEX}, 11_{HEX}, 13_{HEX}, and 14_{HEX}) are used to define a window for alarm output. Alarm 2 at pin IO2 is inverted to Alarm 1 at pin IO1. 0: disabled 1: enabled	AWME
6:5	11	Output polarity { Alarm 2 / Alarm 1 } at pin { IO2 / IO1 } 0: Alarm low-active 1: Alarm high-active	APO
4	0	Output mode port IO2 Threshold, hysteresis and delay of Alarm 2 output are defined in EEPROM addresses $19/13_{hex}$ to $21/15_{hex}$. 0: disabled 1: Alarm 2 output	PMIO2
3:2	00	Output mode port IO1 Threshold, hysteresis and delay of Alarm 1 output respectively the limits for PWM1 output are defined in EEPROM addresses $16/10_{hex}$ to $18/12_{hex}$. 0x: Disable 10: PWM1 output 11: Alarm 1 output	PMIO1
1:0	00	Output mode port OUT The limits for all outputs are defined in EEPROM addresses 8 to 9. 00: Voltage output 01: Current output 10: PWM2 output 11: Disable	COS1

Table 5.8 Configuration Word ADJREF

Bit	IC-default	ADJREF - Adjustment of internal references EEPROM/RAM address $1C_{HEX}$	
15:13	100	Adjust sensor bridge current Enabled if CFGAPP:CSBE = 1 (enables current supply for sensor bridge). Supply current depends on external zero-TC reference resistor R_{BR_REF} → I_{BR} = VDDA / (16· R_{BR_REF}). I_{BR} is finely adjustable in the range of 0.5 (000_{BIN}) to 1.375 (111_{BIN}) of I_{BR} in steps of approximately 0.125 units. Default setup is equivalent factor 1 (100_{BIN}).	CSB
12:10	100	Fine adjustment of controlled analog supply voltage Enabled with CFGAPP:VDCE and is raw adjusted with CFGAPP:VDC. Use this value to finely adjust the controlled analog supply voltage: from -1%VDDA (000_{BIN}) to +0.75%VDDA (111_{BIN}).	VDCA
9:7	100	Adjust oscillator frequency The internal oscillator frequency f_{CLK} is raw adjusted with CFGAPP:OSCF. Use this value to finely adjust the internal oscillator frequency in the range of 0.8 to 1.15 ∗ f_{CLK_NOM}	OSCA
6:4	xxx	Adjust bias current Internal bias current is adjustable to move the total current consumption into the required range. Current consumption can be decreased/increased by this value but may cause worse/better analog performance.	BCUR
3:0	1000	TC adjustment of internal bandgap voltage Used to adjust temperature behavior of the controlled analog supply voltage. **Hint:** The controlled analog supply voltage is enabled with CFGAPP:VDCE and is raw adjusted with CFGAPP:VDC.	VREF

5.4. EEPROM Signature

The EEPROM signature (address $29/1D_{hex}$) is used to check the validity of EEPROM contents. The signature is built using a polynomial arithmetic modulo 2. The following source code generates the signature if the field eepcont is allocated by the EEPROM contents (address 0 to 28) and N = 29 is the count of considered addresses.

Figure 5.1 Source-Code Signature Generation

```
#define POLYNOM 0xA005
unsigned short signature(eepcont, N)
   unsigned short eepcont[], N;
   {
      unsigned short sign, poly, p, x, i, j;
      sign = 0; poly = POLYNOM;
      for (i=0; i<N; i++) {
          sign^=eepcont[i];
          p=0; x=sign&poly;
          for (j=0; j<16; j++, p^=x, x>>=1);
          sign<<=1; sign+=(p&1);
      }
      return(~sign);
   }
```

6 Temperature Sensor Adaption and CMV Measurement

6.1. Sensor Bridge in Voltage Mode

Note that only T1 can be used for calibration. There are a few configurations for the temperature measurement that make sense for voltage-supplied bridges. Table 6.1 shows these configurations for different types of temperature sensors. Table 6.2 and following defines the resulting input range for the differential voltage V_{IN_T} at using an external temperature measuring diode for different supply voltages.

Table 6.1 Configuration of Temperature Measurement

Temperature sensor	Temp Gain a_{IN_T}	Zero point ZCT	Sensor referenced to	Remarks
Internal diode @ 5V	GT2	5	VSS	V_{VDDA} =4.5-5.5V, CFGAPP:VDC=5V
Internal diode @ 3V	GT2	7	VSS	V_{VDDA} =2.7-3.3V, CFGAPP:VDC=3V
Internal diode @ 3-5V	GT1	7	VSS	V_{VDDA} =2.7-5.5V, CFGAPP:VDC=3V
External diode External resistor	GT1 / GT2 / GT3 / GT4	0 to 7	VSS: $V_{IN\_DIFF\_T} = V_{IR\_TEMP}$ - VSS VDDA: $V_{IN\_DIFF\_T} = VDDA - V_{IR\_TEMP}$	V_{IR_TEMP} is voltage at pin IR_TEMP; $V_{IN\_DIFF\_T}$ is differential input voltage

Note: Internal diode adjustments are fitted to a typical V_F of 0.65V for the internal diode.

6.1.1. Internal and External Diode

Adaptation of an external diode is described in this section. Measure $V_{IN\_DIFF\_T}$ to determine an adjustment, normally 650mV is expected. Typically $V_{IN\_DIFF\_T}$ changes depending on the temperature with –2mV/K.

Hint: If using an internal or external diode for temperature measurement, it is necessary to adapt the supply voltage regulator at the external supply voltage (refer to register 18_{hex} CFGAPP:VDC). The voltage regulator must be tuned to the nearest value smaller than the VDDA potential. The input voltage ranges are valid for the described adjustments. When adapting an external temperature measuring diode, ensure that at the minimum and maximum temperature, the V_F of the diode including tolerances is inside the described voltage range.

Recommendation: If the sensor module is supplied in the supply voltage range of 2.7 to 5.5V, use an external resistor as the temperature sensor. If a diode temperature sensor should be used, use GT1 + ZCT7 for the internal diode and for the external diode GT1 with a V_T correlating to the ZCT adjustment.

The temperature sensor must be adjusted for gain and offset shift so that the measurement readout* (command: "D9" - START_AD_T1) *is within 12.5 to 87.5 % of ADC range (e.g. 13-bit, +/- 1/2: ADC-min/max = -3072/3072) for the full temperature range.

Table 6.2 Input Signal Range $V_{IN\_DIFF\_T}$ Using an External Diode (to VSS) and VDDA=5V

CFGAPP:VDDA=5V (V_{T_REF}=4V)		Tx ZeroPointShift ZCT; VDDA=5V							
Analog Gain a_{IN_T}	$V_{IN\_DIFF\_T}$	0	1	2	3	4	5	6	7
GT4	min [V]	0.12	0.24	0.35	0.46	0.97	1.01	1.12	1.15
	max [V]	0.60	0.71	0.82	0.90	1.56	1.64	1.74	1.77
GT3	min [V]				0.25	0.50			
	max [V]			0.60	1.00				
GT2	min [V]				0.05	0.30	0.35 *	0.39	
	max [V]				0.60	0.75	0.80 *	0.85	

Table 6.3 Input Signal Range $V_{IN\_DIFF\_T}$ Using an External Diode (to VSS) and VDDA=4V

CFGAPP:VDDA=4V (V_{T_REF}=3.25V)		Tx ZeroPointShift ZCT							
Analog Gain a_{IN_T}	$V_{IN\_DIFF\_T}$	0	1	2	3	4	5	6	7
GT4	min [V]			0.28	0.37 *				
	max [V]			0.54	0.63 *				
GT3	min [V]			0.02	0.08	0.37 *	0.43 *		
	max [V]			0.45	0.51	0.80 *	0.90 *		

Table 6.4 Input Signal Range $V_{IN\_DIFF\_T}$ Using an External Diode (to VSS) and VDDA=3V

CFGAPP:VDDA=3V (V_{T_REF}=2.5V)		Tx ZeroPointShift ZCT							
Analog Gain a_{IN_T}	$V_{IN\_DIFF\_T}$	0	1	2	3	4	5	6	7
GT4	min [V]				0.28	0.62			
	max [V]				0.53	0.87			
GT3	min [V]				0.06	0.30	0.35 *	0.40 *	0.44 *
	max [V]				0.43	0.64	0.70 *	0.75 *	0.80 *

Hint: The input signal ranges $V_{IN\_DIFF\_T}$ are roughly estimated and must be verified in application.

6.1.2. External Resistor

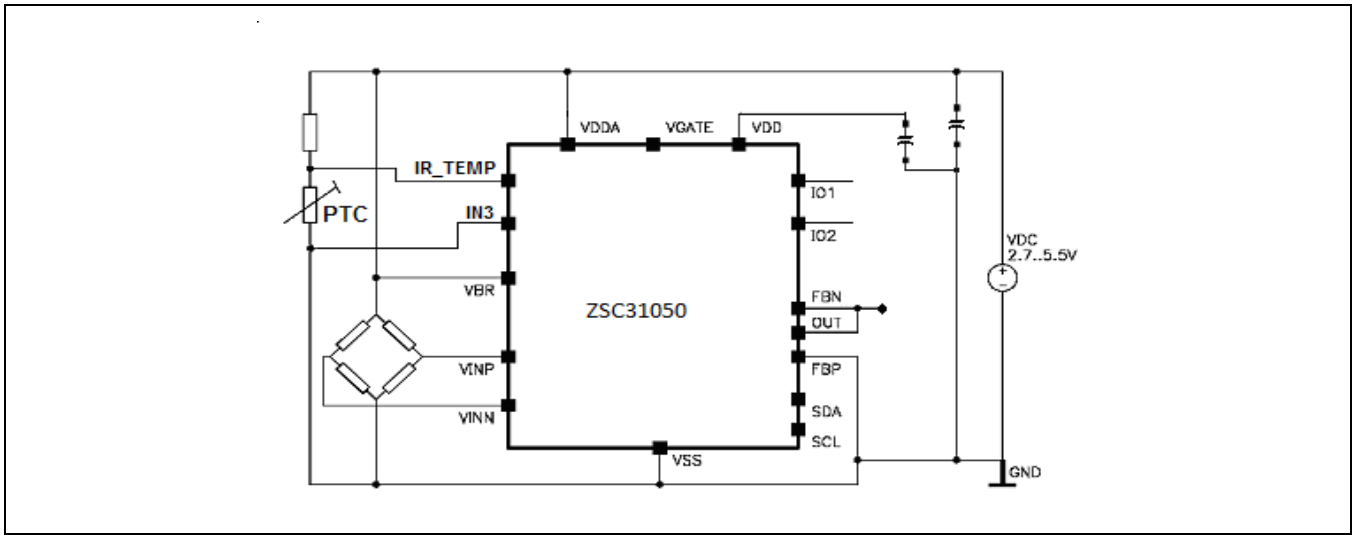
The external resistor mode supports using an external half bridge for the temperature measurement, which is connected between VDDA and VSS. The input signal range is asymmetric and has a maximum of approximately 30%∗VDDA less than VDDA or 30%∗VDDA more than VSS (programmable reference to VDDA or VSS).

Note: The input range is asymmetric from 0 to 30% of VDDA, beginning from VSS.

* This setting is recommended for external diodes.

Table 6.5 explains resulting input range for using an external resistor for temperature measurement in detail. The voltage $V_{IN\_DIFF\_T}$ is displayed as a ratio to VDDA because temperature measurement via an external resistor delivers a ratiometric result.

Figure 6.1 Temperature Measurement with External Resistor (PTC)



Note: The input range is asymmetric from 0 to 30% of VDDA, beginning from VSS.

Table 6.5 Valid Input Signal Range (VIN_DIFF_T / VDDA) using External Resistor Mode

		Tx ZeroPointShift ZCT; VDDA = 3 to 5V							
Analog Gain a_{IN_T}	$V_{IN\_DIFF\_T}$ / VDDA	0	1	2	3	4	5	6	7
GT4	min	3.7%	6.4%	9.1%	11.8%				
	max	18.0%	20.7%	23.4%	26.1%				
GT3	min	0.0%	1.2%	3.0%	4.8%	13.9%	15.6%	17.4%	19.2%
	max	15.1%	16.9%	18.7%	20.5%	29.4%	31.2%	33.0%	34.8%
GT2	min			0.0%	0.9%	7.6%	9.0%	10.3%	11.6%
	max			16.6%	18.1%	24.7%	26.0%	27.4%	28.7%

Hint: The input signal ranges ($V_{IN\_DIFF\_T}$ / VDDA) are roughly estimated and have to verify in application. Gain GT1 is not applicable in this configuration.

6.1.3. Conversion Result and Sensitivity Calculation

Table 6.6 Gain Calculation Parameter

Gain Identifier	a_{IN_T}	G_{FB2}	G_{XZC}	Gain Identifier in previous software
GT4	5.65	6	3	14
GT3	5.17	5.5	1.833	9
GT2	4.7	5	1.25	7
GT1	1.88	2	0.2	2.8

The gain (= a_{IN_T}) and offset (= ZCT) adjustments for the temperature measurement are programmable. The gain factor a_{IN_T} is a calculated value for an estimated calculation of sensitivity. The temperature measurement result is referenced to V_{T_REF} (depending on input mode) and can be calculated and verified by using the following formulas (voltages referenced to VSS, V_{IR_TEMP} = potential at pin IR_TEMP referenced to VDDA or VSSA depending on adjustment):

$$T1 = \left[2 * \left(G_{XZC} * \frac{Z_{XZC}}{40} - \frac{V_{IR\_TEMP}}{V_{T\_REF}} * \frac{G_{FB2}}{2.125} \right) + \frac{1}{2} \right] * 2^{ADCRES}$$ => command $D1_{HEX}$

$$T1\_AZ = \frac{1}{2} * 2^{ADCRES}$$ => command $D5_{HEX}$

$$T1\_AZC = T1 - T1AZ = \left(G_{XZC} * \frac{Z_{XZC}}{40} - \frac{V_{IR\_TEMP}}{V_{T\_REF}} * \frac{G_{FB2}}{2.125} \right) * 2^{ADCRES+1}$$ => command $D9_{HEX}$

G_{XCZ}: Refer to Table 6.6 for details

G_{FB2}: Refer to Table 6.6 for details

Z_{XZC} = {4,5,6,7,12,13,14,15} for software adjustment ZeroPointShift ZCT = {0,…,7}

V_{T_REF} = 4/3.25/2.5 for diode or VDDA for external resistor

ADCRES = ADC resolution in bits

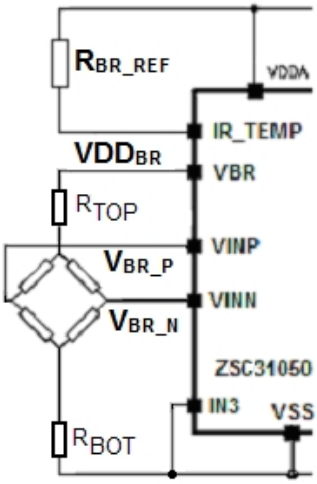
The resolution of temperature measurement can be calculated and verified by using following formula:

ST_{TS_E} = ABS { [T1_AZC ($V_{IR\_TEMP\_X}$) - T1_AZC($V_{IR\_TEMP\_Y}$)] / [$V_{IR\_TEMP\_X}$ - $V_{IR\_TEMP\_Y}$] } [counts/V]

$ST_{TS\_E} = 2^{ADCRES} * (a_{IN\_T} / V_{T\_REF})$ [counts/V]

6.2. Sensor Bridge in Current Mode

Figure 6.2 Bridge Current Mode Application



Bridge current excitation enables temperature measurement using temperature coefficient of bridge resistors, so no additional temperature sensor is needed. For temperature data acquiring the common mode voltage of the bridge inputs (VINN and VINP) is measured.

The bridge current must be adjusted with the restriction that the voltage drop across bridge VDD_{BR} and the input signals V_{BR_P} and V_{BR_N} are in the allowed range. The bridge current can be coarsely tuned by changing the external resistor R_{BR_REF} and finely adjusted by changing configuration register ADJREF:CSB.

The reference resistor R_{BR_REF} can be calculated as follows:

$$R_{BR\_REF} = R_{BR}(T) * VDDA / (16 * 2 * V_{IN\_CM})$$

The subjection of I_{BR} from R_{BR_REF} can be explained as follows:

$$I_{BR} = VDDA / (16 * R_{BR\_REF})$$

This can be used to calculate the current:

$$I_{BR} = 2 * V_{IN\_CM} / R_{BR} \text{ (with } I_{BR} < 1.5mA)$$

V_{IN_CM} in bridge excitation mode depends on a set of parameters. Recommendation: The spreadsheet *ZSC31050_Bridge_Current_Excitation_Rev_X_xy.xls* (available on request: see page **Error! Bookmark not defined.**) can be used for a detailed calculation of R_{BR_REF}, R_{TOP} and R_{BOT} in this mode to ensure that the common mode range is not degraded due to full temperature operation, tolerances of external elements, and measured rejection limits.

Bridge Current Excitation Mode offers two options for the A/D converter reference voltage, which is adjusted with the CFGAPP:ADREF configuration bit. In “VREF=VBR” Mode the potential of the VBR pin is used as the A/D converter reference voltage and it is recommended for ratiometric bridges. Extended zero compensation (XZC) can be used to compensate large offset values. In “VREF=VDDA” mode, VDDA is used as the A/D converter reference voltage. “VREF=VDDA” must be used for sensor bridges with non-ratiometric behavior in the temperature range, such as a temperature pre-compensated sensor.

In the case of activated bridge current excitation applications, XZCE must be always enabled if “VREF=VDDA” is also active, XZC must be set to “0”; otherwise, an error will be generated due to the fact that the XZC signal is generated based on the bridge voltage.

The following rules describe this behavior:

CFGAPP:CSBE=1 => CFGAPP:XZCE=1

CFGAPP:ADREF=1 & CFGAPP:CSBE=1 => CFGAPP:XZCE=1 & CFGAFE:XZC=0

6.2.1. Bridge Signal Measurements

Calculation options provided in *ZSC31050_Bridge_Current_Excitation_Rev_X_xy.xls* (available on request; see page **Error! Bookmark not defined.**) can be used to verify that the input signal is within the signal common mode range depending on the gain. The input / common mode voltage ranges depend on the adjusted gain a_{IN_2} of the second PGA stage (refer to “Gain Amp2” in the *ZSC31050 Data Sheet*, section 2.3.1).

For current-supplied bridges, the temperature measurement T1 is always done by evaluating the common mode voltage of the sensor bridge. This mode is enabled by CFGAPP:CSBE = 1. The necessary analog gain a_{IN_T} is 2.8, and this must be set with configuration parameter CFGTMP:GAINT1. The parameters CFGTMP:TAM1 and CFGTMP:ZCT1 are not applicable.

It is possible to verify the input signal common mode level/potential at calibration using the commands “D9” or “DB”. Calculation options are also available in *ZSC31050_Bridge_Current_Excitation_Rev_X_xy.xls* for representing an ideal A/D conversion result /data readout for commands “D9” and “DB”. IDT recommends using this function to verify the existing common mode range in the application and to interpolate to determine the real common mode potential if the measurement/calibration in the temperature range is located at the edges of the temperature of the application.

6.2.2. Temperature Measurement

Temperature measurement is completely configured by activating the Bridge Current Mode – nothing needs to be adjusted. The temperature measurement result can be calculated and verified by using the following formulas (voltages referenced to VSS; r_{ADC} = ADC resolution in bits):

$$V_{IN\_CM} = (V_{BR\_P} + V_{BR\_N}) / 2$$

$$T1 = 2^{r_{ADC}} * \{2.8 * [V_{IN\_CM} / VDDA - 1/3] + 0.5 \} \quad \Rightarrow \text{command “D1”}$$

$$T1\_AZ = 2^{r_{ADC}} * 0.5 \quad \Rightarrow \text{command “D5”}$$

$$T1\_AZC = T1 - T1AZ = 2^{r_{ADC}} * 2.8 * [V_{IN\_CM} / VDDA - 1/3] \quad \Rightarrow \text{command “D9”}$$

Gain and offset in Bridge Current Mode are not programmable for acquiring temperature. The resolution of the temperature measurement can be calculated and verified by using the following formula:

$$ST_{TS\_BCM} = ABS \{ [T1\_AZC(V_{IN\_CM\_X}) - T1\_AZC(V_{IN\_CM\_Y})] / [V_{IN\_CM\_X} - V_{IN\_CM\_Y}] \} \quad [counts/V]$$

$$ST_{TS\_BCM} = 2^{r_{ADC}} * (2.8 / VDDA) \quad [counts/V]$$

6.3. TEMP2 Measurements

The TEMP2 path is an additional path, which can be calibrated independent from the main path up to second order in the temperature and the signal (offset, gain and nonlinearity). **TEMP2 measurements cannot be used for bridge signal temperature calibration.**

ZSC31050 offers 4 modes for the TEMP2 measurements:

- Internal diode mode (CFGTMP:TAM2=00)
- External diode using pin IR_TEMP (CFGTMP:TAM2=01)
- Resistor mode using pin IR_TEMP (CFGTMP:TAM2=10)
- External voltage mode using **IN3** pin (CFGTMP:TAM2=11)

6.3.1. Internal, External Diode and Resistor Mode

Refer to section 6.1 for adapting input constraints and the adjustments for internal/external diode and resistor.

6.3.2. External Voltage Mode (also called IN3-Measurement)

The external Voltage Mode realizes ratiometric signal measurement of an external half bridge (connected via **IN3** pin) or a voltage source referenced to an internal voltage divider or source.

Adjustable Parameters/Configurations

The **IN3 Mode** (CFGAPP:IN3M) defines the internal half bridge connection: as a reference potential or measurement mode for using IN3 as an input:

- "V->VDDA/2" VDDA/2 is used as reference potential (ratiometric measurement)
- "V->V_{BG}" Bandgap voltage (approx. 1.23V) is used as a reference potential (non-ratiometric)
- "VDDA/2->V_{BG}" Supply voltage measurement mode – divided supply voltage (VDDA) is measured referenced to bandgap voltage

Additional adjustment parameters:

- **ADC-Range Shift IN3** (CFGAPP:ADRAIN3) defines the common mode range of the input signal and is used to adjust the AD converter range to the actual input signal range.
- **T2 Analog Gain** (CFGTMP:GAINT2) defines the gain for the differential signal between IN3 and the internal reference potential.

Table 6.7 IN3 Input Signal Range Depending on Mode and Gain

Mode		GT1	GT2	GT3	GT4
V->VDDA/2	min [%VDDA]	1.80/5	2.20/5	2.30/5	2.40/5
	max [%VDDA]	3.30/5	2.80/5	2.70/5	2.70/5
V->V_{BG}	min [V] @VDDA=5V	0.75	-	-	-
	max [V] @VDDA=5V	2.05	-	-	-

Hint: The IN3 input signal ranges are roughly estimated and must be verified in detail in the application.

6.4. CMV Measurement

ZSC31050 offers a special method for sensor aging detection. The common mode voltage (CMV) of the sensor bridge is measured and compared with defined limits for this function. Limits are stored in registers 13_{HEX} (lower) and 14_{HEX} (upper). A CMV error is indicated if the CMV measurement result is lower than the value stored in register 13_{HEX} or higher than the value stored in register 14_{HEX}.

Limits can be expressed as a percentage of the CMV measurement result (command: “DB”) or calculated directly with the CMV_AZC formula. When defining CMV limits, note that the CMV measurement result can drift in the temperature range depending on the temperature behavior of the sensor bridge.

The CMV measurement acquires the common mode voltage of the bridge (VINcm) and can be approximately calculated using following formula:

CMV_AZC = 2^RES ∗ (2.8 ∗ (VINcm/VDDA - 1/3) + 1/16) - T1AZ + 2^RES/2

with:

RES = Resolution in bits (RES =[9-15])

T1AZ = AZ readout of T1 Measurement (“D5” command)

VINcm = common mode voltage at input (shorted VINP and VINN)

VDDA = VDDA (supply) voltage

In the ideal case, T1AZ = RES/2:

CMV_AZC = 2^RES ∗ (2.8 ∗ (VINcm/VDDA - 1/3) + 1/16)

7 Additional Built-In Features

7.1. Internal Supply Regulator using an external FET

In non-ratiometric mode, the internal supply regulator can be used for controlling the VDDA supply voltage. The selection of the external regulation FET must be made by checking the droop and the regulation range under temperature conditions; parameter deviation of the external FET; and power consumption of the bridge and the ZSC31050.

Recommended FET types (JFET or N-Depletion) are

- DN3545: Recommended; used on the ZSC31050 Evaluation Kit Board
- BSS169: only 100V V_{DS}
- BSS149: a larger package
- BSP149: SOT-223-package

Note: Refer to the *ZSC31050 Data Sheet* for voltage regulator application circuit recommendations.

7.2. External Clock Input Option

Basically the ZSC31050 is clocked by an internally generated digital clock. Its frequency can be adjusted by EEPROM settings within a range of 1 to 4MHz. External clock frequency is specified in the same range.

The ZSC31050 also supports external clocking via the IN3 pin. For example, the external clocking can be used to enable a synchronized mode of working or a precise PWM frequency.

This mode must be enabled by EEPROM setting.

Table 7.1 External Clock Specification

Nr.	Parameter	Symbol	Min	Typ	Max	Unit	Conditions
1	External clock frequency	f_{clkext}	0.1		4	MHz	<800kHz accuracy derated
2	Clock LOW/HIGH time	$t_{clkext\_LOW/HIGH}$	125			µs	
3	Clock fall/rise time	$t_{clkext\_R/F}$			1	µs	
4	Input-High-Level	V_{clkext_HIGH}	0.7		1	VDDA	
5	Input-Low-Level	V_{clkext_LOW}	0		0.3	VDDA	

7.3. Clock Frequency Measurement and Adjust

Following principle can be used for measurement of the internal clock frequency:

- Configure an output (OUT pin or IO1 pin) as a PWM output and adjust the PWM correlating to external measurement constraints, possibilities, and required accuracy.
- Measure the PWM period.
- Calculate internal clock frequency using the following clock frequency formula.

$$f_{CLK} = \frac{2^{r_{PWM}} * PWM_{CLK\_DIV}}{t_{PWM\_PERIOD}}$$

r_{PWM} …	PWM resolution (CFGOUT:PWMRES)
$PWM_{CLK\_DIV} \in [1;4]$ …	PWM clock divider (CFGOUT:PWMD)
t_{PWM_PERIOD} …	Measured PWM period time

8 Related Documents

Document
ZSC31050 Feature Sheet
ZSC31050 Data Sheet
ZSC31050 Evaluation Kit Description
ZSC31050 Application Note—Current Loop *
ZSC31050 Application Note—Temperature Sensing with Thermocouples *
ZSC31050 Application Note—0-10V Output
ZSC31050 Application Note—RTD *
ZSC31xxx Application Note—External Protection Circuitry
SSC Application Note—Single Ended Input *
ZSC31050 Bandwidth Calculation Spread Sheet

Visit the product page for the ZSC31050 (www.IDT.com/ZSC31050) or contact your nearest sales office for the latest version of these documents.

* Note: Documents marked with an asterisk (*) require a free customer login account.

9 Glossary

Term	Description
ADC	Analog-to-Digital Converter
CM	Command Mode
CMC	Calibration Microcontroller
CMV	Common Mode Voltage
DAC	Digital-to-Analog Converter
DM	Diagnostic Mode
EEPROM	Electrically Erasable Programmable Read Only Memory
MSB	Most Significant Bit
NOM	Normal Operation Mode
OWI	One Wire Interface
OUT	Analog Output Pin
P	Pressure or Bridge Sensor Measurand (in equations)
PWM	Pulse Wide Modulation
RAM	Random-Access Memory
ROM	Read Only Memory
SCC	Sensor Connection Check
SIF	Serial Interface
TS	Temperature Sensor
XZC	eXtended Zero Compensation

10 Document Revision History

Revision	Date	Description
…	-	Former document versions.
1.03	September 2009	Adjustment to new ZMDI template.
1.04	October 2009	Update for “Related Documents” and “Document Revision History” so that information is included in table. Change to ZMDI denotation.
1.05	November 2009	Changed default EEPROM settings since modified test program is used formatting and linking issues solved. Bit 3 of EEPROM/RAM address 24 restored. Content of Table 6.4: ZSC31050D VDDA=3V: Input signal range VIN_DIFF_T at using an external diode (to VSS) corrected. Content of Table 1.1: Error Codes corrected.
1.06	May 2010	Inserted new drawings for Figure 4.3, Figure 4.4, Figure 4.7, Figure 4.8, Figure 4.7. Exchanged ZACwireTM to OWI (section 4.3.4). Section 9: Extended glossary. Added parameter tSPI_HD_SS in Table 4.4. Adjusted to new ZMDI template.
1.07	May 06, 2010	Wrong title in header corrected
1.08	July 01, 2010	Updated imagery on cover page. Corrected “AZC” for command in Table 4.6. Renamed ZMD31050 to ZSC31050. Added information about Dx commands in section 4.5. Minor edits for cross-references.
1.09	June 5, 2012	CFGCYC:OWIWIND modified to CFGSIF:OWIWIND
1.10	October 14, 2013	VDDA coding for fine adjustment updated. XZC function updated. ADC calculation formula corrected according to the Range Shift definition.
1.11	November 4, 2013	Update to Table 4.5 for notes for the SET_DAC command (60_{HEX}). Updates to Table 1.1 for the AOUT behavior for Sensor Connection error after reset.
1.12	June 23, 2015	Edits for section 3.2.3 and correction for “Switch off threshold A_{OFF}” formula in Table 3.4. Update for EEPROM defaults in Table 5.1. Update for contact information. Minor edits for consistency.
	April 26, 2016	Changed to IDT branding.

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