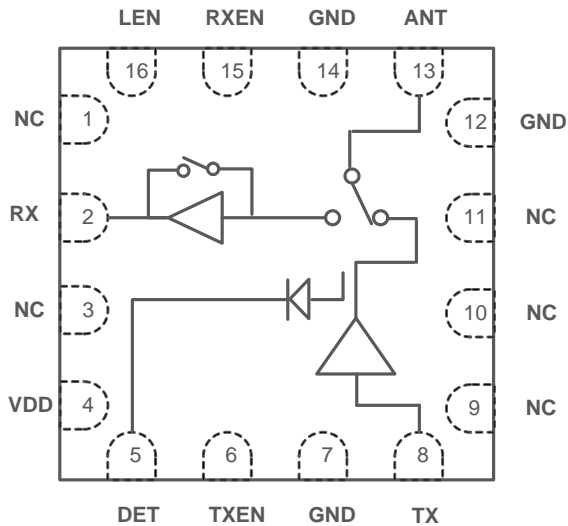# CMOS 5GHz WLAN 802.11ac RFeIC WITH PA, LNA AND SPDT

Description

RFX8050W is a highly integrated, single-chip, single-die RFeIC (RF Front-end Integrated Circuit) which incorporates key RF functionality needed for IEEE 802.11a/n/ac WLAN system operating in the 5.15-5.85GHz range. The RFX8050W architecture integrates a high-efficiency high-linearity power amplifier (PA), low noise amplifier (LNA) with bypass, the associated matching network, LO rejection, and harmonic filters all in a CMOS single-chip device.

RFX8050W has simple and low-voltage CMOS control logic, and requires minimal external components. A directional coupler based power detect circuit is also integrated for accurate monitoring of output power from the PA.

RFX8050W is assembled in an ultra-compact, ultra-thin 2.5x2.5x0.4mm 16-lead QFN package. With support to direct battery operation, the RFX8050W is ideal RF front-end solution for implementing 5GHz WLAN in smartphones and many other mobile platforms.

Applications

- ▶ 802.11n/ac Wi-Fi Devices
- ▶ Smartphones
- ▶ Tablets/MIDs
- ▶ Gaming
- ▶ Notebook/Netbook/Ultrabooks
- ▶ Mobile/Portable Devices
- ▶ Consumer Electronics
- ▶ Other 5GHz ISM Platforms

FEATURES

- 5GHz WLAN Single Chip, Single-Die RF Front-End IC
- High Transmit Signal Linearity Meeting Standards for 802.11ac OFDM /MCS9 Modulation
- Separate TX, RX Transceiver Ports, Single Antenna Port
- 5GHz Power Amplifier with Low-Pass Harmonic Filter
- Low Noise Amplifier with Bypass Mode
- Transmit/Receive Switch Circuitry
- Integrated Power Detector for Transmit Power Monitor and Control
- Low Voltage (1.2V) CMOS Control Logic
- Low-Current Mode in TX for Battery Current Savings

- ESD Protection Circuitry on All Pins DC Decoupled RF Ports
- Internal RF Decoupling on All VDD Bias Pins
- Low Noise Figure for the Receive Chain
- High Power Capability for Received Signals in Bypass Mode
- Very Low DC Power Consumption
- Full On-chip Matching Circuitry
- Minimal External Components Required
- 50-Ohm Input / Output Matching
- Market Proven CMOS Technology
- 2.5mm x 2.5mm x 0.4mm Small Outline 16L QFN Package with Exposed Ground Pad
- RoHS and REACH Compliant

Rev 1.5
Aug '14

PIN ASSIGNMENTS:

Pin Number	Pin Name	Description
1, 3, 9, 10, 11	NC	Internally Not Connected
2	RX	RF Output Port from LNA or Bypass – DC Shorted to GND
4	VDD	DC Supply Voltage
5	DET	Analog Voltage Proportional to the PA Power Output
6	TXEN	CMOS Input to Control TX Enable
8	TX	RF Input Port from the Transceiver – DC Shorted to GND
13	ANT	Antenna Port RF Signal from the PA or RF Signal Applied to the LNA-DC Shorted to GND
15	RXEN	CMOS Input to Control RX Enable
16	LEN	CMOS Input to Control LNA Enable or Bypass Mode
7, 12, 14	GND	Ground – Must Be Connected to GND in the Application Circuit

PIN-OUT DIAGRAM:
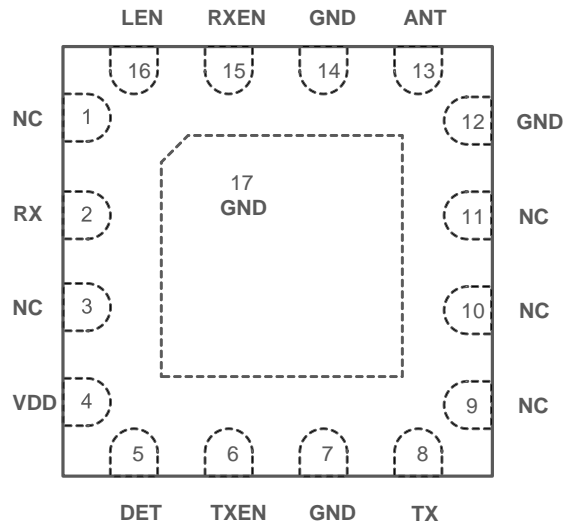
(Top "See-Through" View)

ABSOLUTE MAXIMUM RATINGS:

Parameters	Units	Min	Max	Conditions
DC VDD Voltage Supply	V	0	5.0	All VDD Pins
DC Control Pin Voltage	V	0	3.6	All Control Pins
DC VDD Current Consumption	mA		400	Through VDD Pins when TX is "ON"
TX RF Input Power	dBm		+7	
ANT RF Input Power	dBm		+10	Bypass Mode
Junction Temperature	^{o}C		150	
Storage Ambient Temperature	^{o}C	-40	+150	Appropriate care required according to JEDEC Standards
Operating Ambient Temperature	^{o}C	-40	+85	
Moisture Sensitivity				MSL1

Note: Sustained operation at or above the Absolute Maximum Ratings for any one or combinations of the above parameters may result in permanent damage to the device and is not recommended.

All Maximum RF Input Power Ratings assume 50-Ohm terminal impedance.

NOMINAL OPERATING CONDITIONS:

Parameters	Units	Min	Typ	Max	Conditions
DC VDD Voltage Supply	V	3.0	3.6	4.8	
Control Voltage "High" *(Note 1)*	V	1.2		*	* 3.6V or VDD Whichever is Lower
Control Voltage "Low"	V	0		0.3	
DC Control Pin Current Consumption	µA		1		
DC Shutdown Current	µA		1		
PA Turn On/Off Time	µsec		0.5		
LNA Turn On/Off Time	µsec		0.5		
Shut-Down and "ON" State Switching Time	µsec		0.5		

Note 1: If control voltage can exceed 1.8V, a 1KΩ – 10KΩ series resistor is recommended for the application circuit on each control line.

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TRANSMIT MODE CHARACTERISTICS (VDD=3.6V; T=+25 ^{o}C)

Parameters	Units	Min	Typ	Max	Conditions
Operating Frequency Band	GHz	5.15		5.85	
Linear Output Power for 802.11ac	dBm		+15.5		EVM<1.8%, MCS9 VHT80 256 QAM
Linear Output Power for 802.11a	dBm		+17		EVM<3%, 64QAM 54Mbps 20MHz BW
Small-Signal Power Gain	dB		28		Between TX and ANT pins
TX Quiescent Current	mA		130		Pout< 0dBm
TX Linear Current	mA		175		P_{OUT} = +17dBm
Power Detector Voltage Output	mV	200		1000	P_{OUT} = +5 to +18dBm, 10kΩ Load
Modulated Second Harmonic	dBm/MHz		-36		P_{OUT}=+18dBm, 802.11n HT40
Modulated Third Harmonic	dBm/MHz		-34		P_{OUT}=+18dBm, 802.11n HT40
Second Harmonic	dBc		-40		P_{OUT}=+18dBm, CW
Third Harmonic	dBc		-40		P_{OUT}=+18dBm, CW
Input Return Loss	dB		-10		At TX Port
Output Return Loss	dB		-8		At ANT Port
Load VSWR for Stability (CW, Fix Pin for Pout=+20dBm with 50Ω load)	N/A	4:1	6:1		All non-harmonically related spurs less than -43dBm/MHz
Load VSWR for Ruggedness (CW, Fix Pin for Pout=+20dBm with 50 Ohm Load)	N/A	8:1	10:1		No Damage

RECEIVE MODE CHARACTERISTICS (VDD=3.6V; T=+25 °C)

Parameters	Units	Min	Typ	Max	Conditions
Operating Frequency Band	GHz	5.15		5.85	All RF Pins are Loaded by 50-Ohm
Gain – Low NF Mode	dB		12		Between ANT and RX pins; RXEN=LEN="High"
Noise Figure – Low NF Mode	dB		3.3		At ANT Pin
Insertion Loss for LNA Bypass Mode	dB		5		Between ANT and RX Pins; RXEN="High", LEN="Low"
Input Return Loss	dB		-10		At ANT Port
			-10		Bypass Mode
Output Return Loss	dB		-10		At RX Port
			-10		Bypass Mode
RF Port Impedance	Ohm		50		Operating Frequency Band
DC Quiescent Current	mA		12		No RF Applied, Through VDD, Low NF Mode
			1.2		No RF Applied, Through VDD, Bypass Mode
Input P_{1dB}	dBm		-5		At ANT Pin, Low NF Mode
			+10		At ANT Pin, Bypass Mode

CONTROL LOGIC TRUTH TABLE

TXEN	LEN	RXEN	Mode Of Operation
0	0	0	Shutdown Mode
1	X	X	Transmit Mode
0	1	1	Receive Mode, Low NF Mode
0	0	1	Receive Mode, LNA Bypass Mode
All Others			Unsupported (No Damage)

Note: "1" denotes high voltage state (> 1.2V)
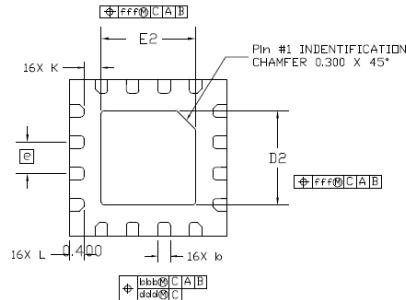"0" denotes low voltage state (<0.3V) at Control Pins

"X" denotes the don't care state
1KΩ – 10KΩ series resistor may be required for each control line
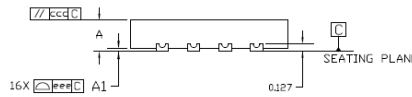
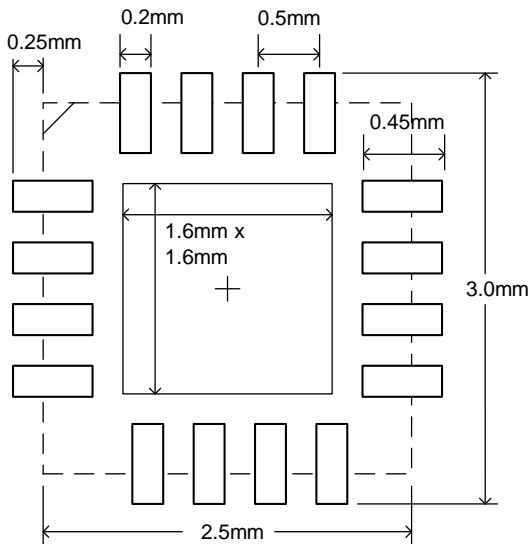## PACKAGE DIMENSIONS (All Dimensions in mm):

TOP VIEW

BOTTOM VIEW

SIDE VIEW

Notes
1. Dimensioning and Tolerancing per ASME Y14.5M-1994.
2. Dimension "A" exclude burr.
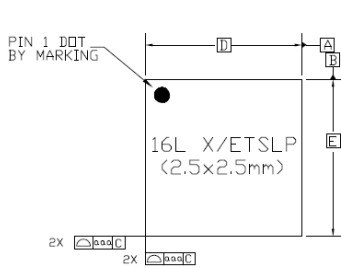
REF.	Min.	Nom	Max.
A	—	—	0.400
	—	—	0.400
	—	—	0.400
A1	0.000	—	0.050
A1	0.127 BSC		
D	2.500 BSC		
E	2.500 BSC		
D2	1.450	1.500	1.550
E2	1.450	1.500	1.550
b	0.150	0.200	0.250
e	0.500 BSC		
K	0.200	—	—
L	0.175	0.225	0.275
Dimensional Tol.			
aaa	0.050		
bbb	0.100		
ccc	0.050		
ddd	0.050		
eee	0.080		
fff	0.050		

PCB LAND PATTERN

PACKAGE MARKING

Pin 1 Mark

First Line Part Number

Second Line Lot Number

Third Line Date Code

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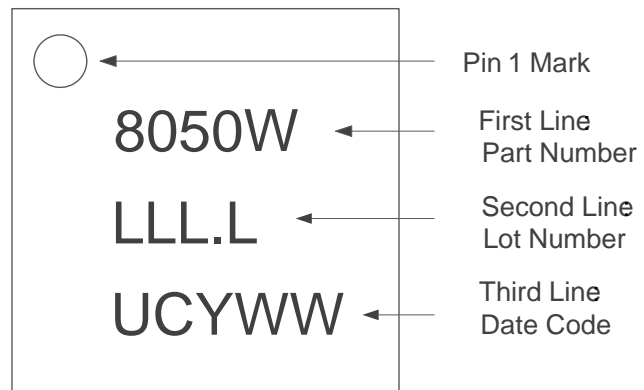
TAPE SPECIFICATION (All Dimensions in mm):

Ao	2.73	+/- 0.05
Bo	2.73	+/- 0.05
Ko	0.65	+/- 0.05
F	3.50	+/- 0.05
P1	4.00	+/- 0.10
W	8.20	+0.10/-0.05

(I) Measured from centreline of sprocket hole to centreline of pocket.
(II) Cumulative tolerance of 10 sprocket holes is ± 0.20 .
(III) Measured from centreline of sprocket hole to centreline of pocket.
(IV) Other material available.

ALL DIMENSIONS IN MILLIMETRES UNLESS OTHERWISE STATED.