AT91SAM7SE-EK Evaluation Board

User Guide

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Section 1
Overview

1.1 Scope

The AT91SAM7SE-EK evaluation board enables the evaluation of and code development for applications running on an AT91SAM7SE device.

This guide focuses on the AT91SAM7SE-EK board as an evaluation platform.

1.2 Deliverables

1.2.1 Standard Version AT91SAM7S-EK VAR

The AT91SAM7SE-EK package contains the following items:

- An AT91SAM7SE-EK board
- One Universal input AC/DC power supply with US and Europe plug adapter
- One A/B-type USB cable
- One serial RS232 cable
- One CD-ROM containing summary and full datasheets, datasheets with electrical and mechanical characteristics, application notes and getting started documents for all development boards and AT91 microcontrollers. An AT91 software package with C and assembly listings is also provided. This allows the user to begin evaluating the AT91 ARM® Thumb® 32-bit microcontroller quickly.

1.3 AT91SAM7SE-EK Evaluation Board

The board is equipped with an AT91SAM7SE512 (128-pin LQFP package) together with the following:

- 32 Mbytes of SDRAM memory
- 256 Mbytes of NAND Flash memory
- One USB device port interface
- One DBGU serial communication port
- One additional serial communication port with RTS/CTS handshake control
- One JTAG/ICE debug interface
- One Atmel AT73C213 Stereo Audio DAC

- One power LED and two general-purpose LEDs
- One joystick and two user input pushbuttons
- One Reset pushbutton
- Three expansion connectors (PIO A, PIO B, PIO C)
- One EBI expansion BGA-like footprint connector

Section 2

Setting Up the AT91SAM7SE-EK Board

2.1 Electrostatic Warning

The AT91SAM7SE-EK evaluation board is shipped in protective anti-static packaging. The board must not be subjected to high electrostatic potentials. A grounding strap or similar protective device should be worn when handling the board. Avoid touching the component pins or any other metallic element.

2.2 Requirements

In order to set up the AT91SAM7SE-EK evaluation board, the following items are needed:

- The AT91SAM7SE-EK evaluation board itself.
- AC/DC power adapter (5V at 2A), 2.1 mm x 5.5 mm

2.3 Layout

Figure 2-1. AT91SAM7SE-EK Layout - Top View

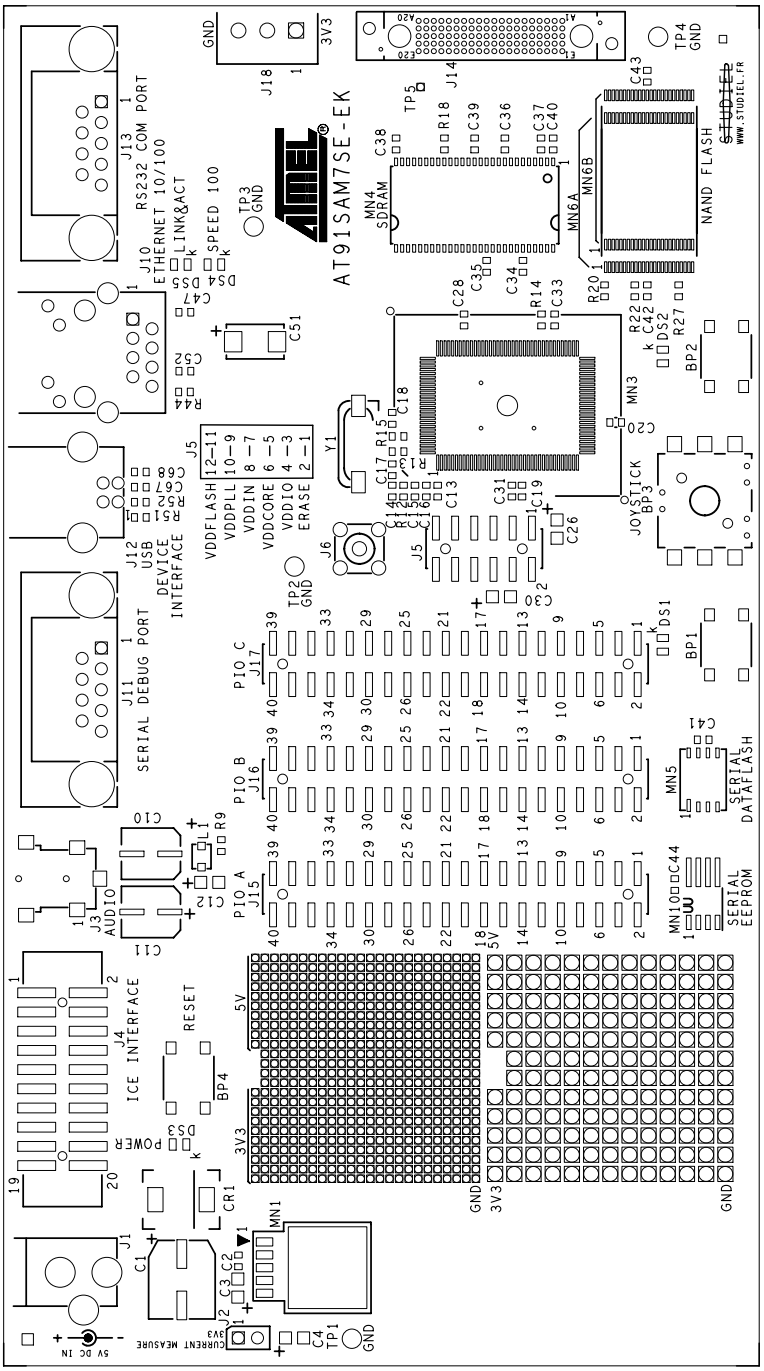
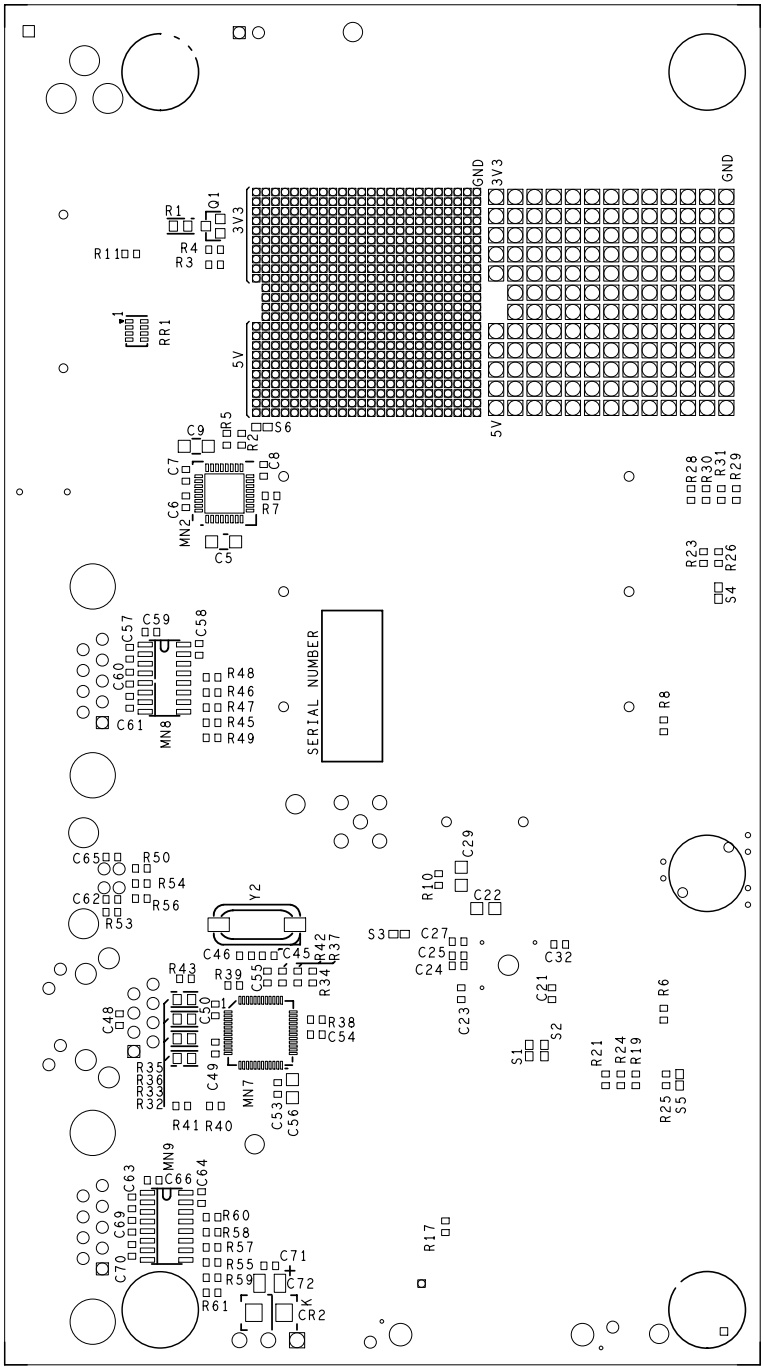


Figure 2-2. AT91SAM7SE-EK Layout - Bottom View



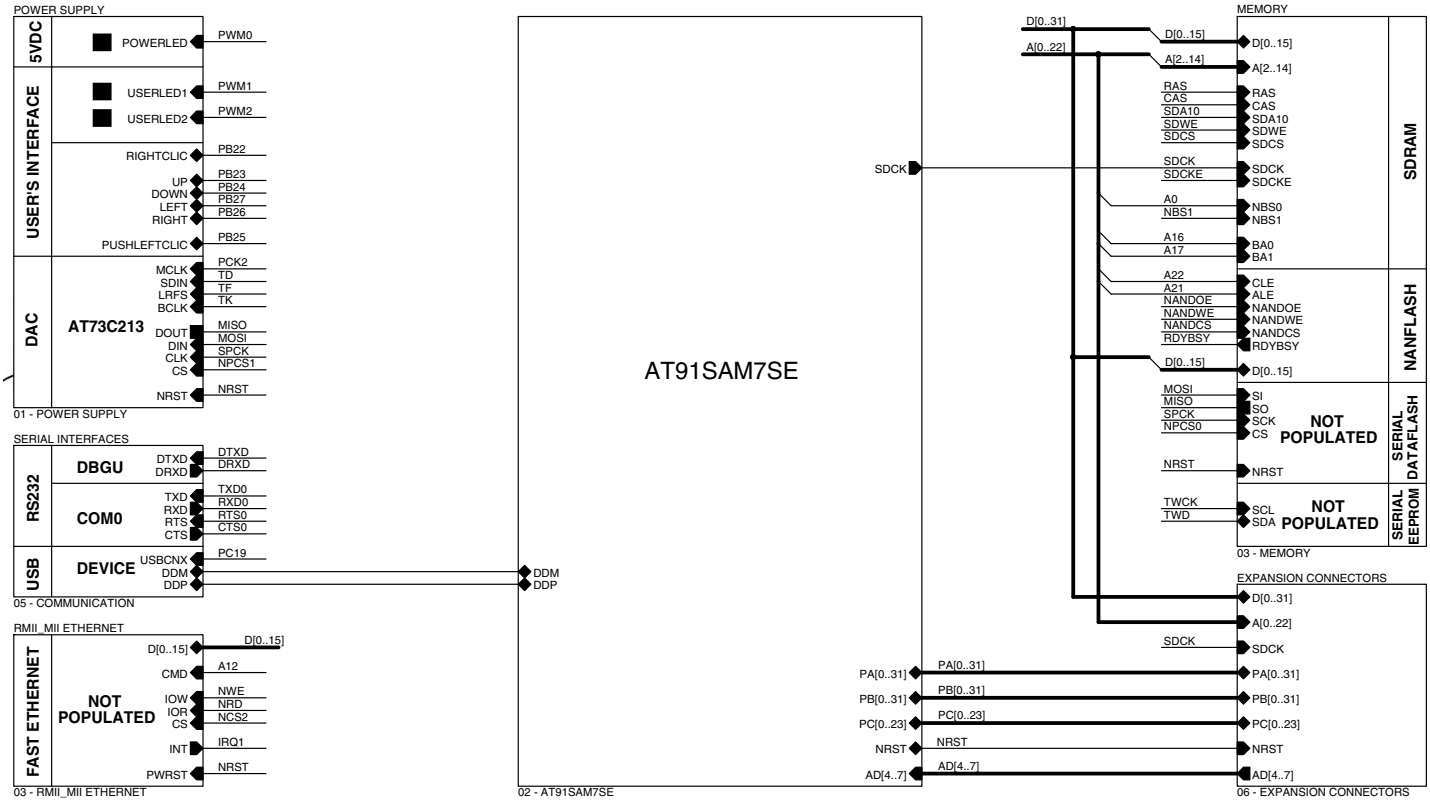
2.4 Powering Up the Board

The AT91SAM7SE-EK requires 5V DC (±5%). DC power is supplied to the board via the 2.1 mm x 5.5 mm socket J1. Coaxial plug center positive standard.

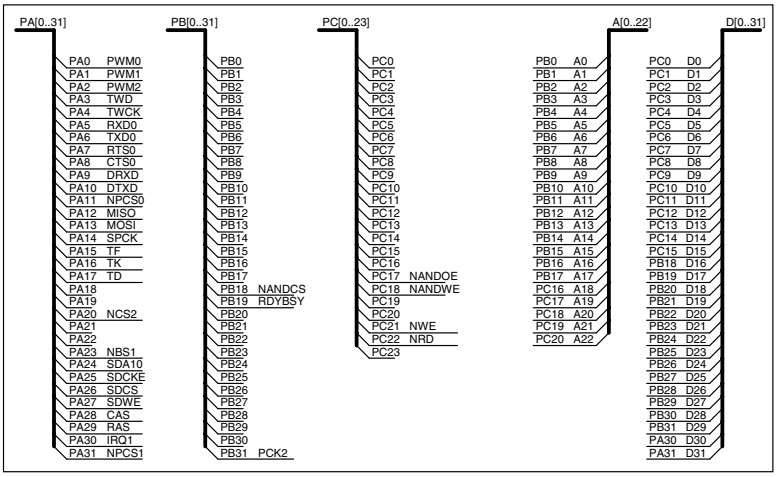
2.5 Getting Started

The AT91SAM7SE-EK evaluation board is delivered with a CD-ROM containing all necessary information and step-by-step procedures for working with the most common development toolchains. Please refer to this CD-ROM, or to the AT91 web site, http://www.atmel.com/products/AT91/, for the most up-to-date information on getting started with the AT91SAM7SE-EK.

2.6 AT91SAM7SE-EK Block Diagram



PIO USAGE



Section 3

Board Description

3.1 AT91SAM7SE Microcontroller

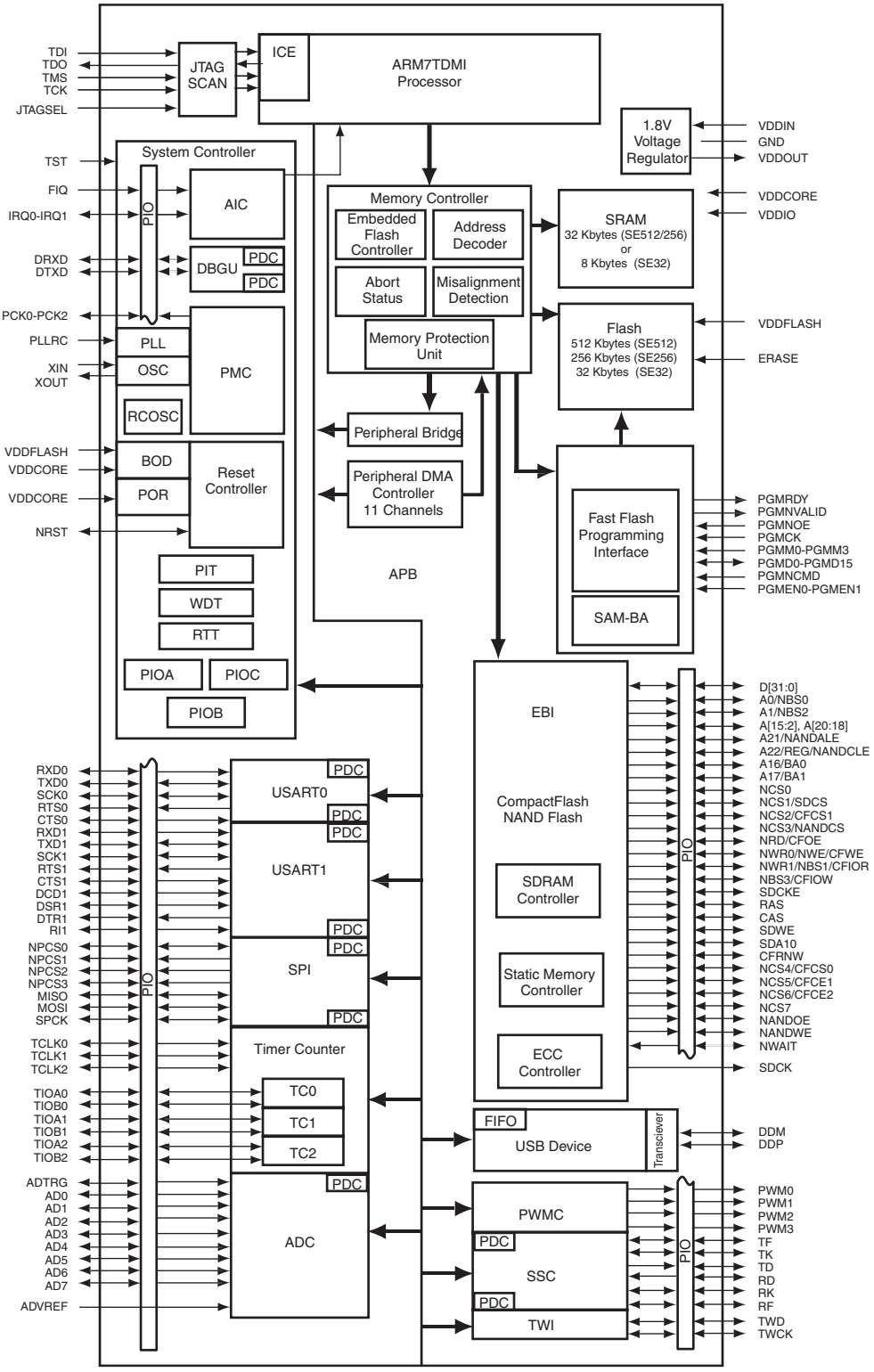
- Incorporates the ARM7TDMI® ARM® Thumb® Processor
  - High-performance 32-bit RISC Architecture
  - High-density 16-bit Instruction Set
  - Leader in MIPS/Watt
  - EmbeddedICE™ In-circuit Emulation, Debug Communication Channel Support
- Internal High-speed Flash
  - 512 Kbytes, Organized in Two Contiguous Banks of 1024 Pages of 256 Bytes Dual Plane (AT91SAM7SE512)
  - 256 Kbytes (AT91SAM7SE256) Organized in One Bank of 1024 Pages of 256 Bytes Single Plane (AT91SAM7SE256)
  - 32 Kbytes (AT91SAM7SE32) Organized in One Bank of 256 Pages of 128 Bytes Single Plane (AT91SAM7SE32)
  - Single Cycle Access at Up to 30 MHz in Worst Case Conditions
  - Prefetch Buffer Optimizing Thumb Instruction Execution at Maximum Speed
  - Page Programming Time: 6 ms, Including Page Auto-erase, Full Erase Time: 15 ms
  - 10,000 Erase Cycles, 10-year Data Retention Capability, Sector Lock Capabilities, Flash Security Bit
  - Fast Flash Programming Interface for High Volume Production
- 32 Kbytes (AT91SAM7SE512/256) or 8 Kbytes (AT91SAM7SE32) of Internal High-speed SRAM, Single-cycle Access at Maximum Speed
- One External Bus Interface (EBI)
  - Supports SDRAM, Static Memory, Glueless Connection to CompactFlash® and ECC-enabled NANDFlash
- Memory Controller (MC)
  - Embedded Flash Controller
  - Memory Protection Unit
  - Abort Status and Misalignment Detection
- Reset Controller (RSTC)
  - Based on Power-on Reset Cells and Low-power Factory-calibrated Brownout Detector
  - Provides External Reset Signal Shaping and Reset Source Status
- Clock Generator (CKGR)
  - Low-power RC Oscillator, 3 to 20 MHz On-chip Oscillator and One PLL
- Power Management Controller (PMC)

  - Power Optimization Capabilities, Including Slow Clock Mode (Down to 500 Hz) and Idle Mode
  - Three Programmable External Clock Signals
- Advanced Interrupt Controller (AIC)
  - Individually Maskable, Eight-level Priority, Vectored Interrupt Sources
  - Two External Interrupt Sources and One Fast Interrupt Source, Spurious Interrupt Protected
- Debug Unit (DBGU)
  - Two-wire UART and Support for Debug Communication Channel interrupt, Programmable ICE Access Prevention
- Periodic Interval Timer (PIT)
  - 20-bit Programmable Counter plus 12-bit Interval Counter
- Windowed Watchdog (WDT)
  - 12-bit key-protected Programmable Counter
  - Provides Reset or Interrupt Signals to the System
  - Counter May Be Stopped While the Processor is in Debug State or in Idle Mode
- Real-time Timer (RTT)
  - 32-bit Free-running Counter with Alarm
  - Runs Off the Internal RC Oscillator
- Three Parallel Input/Output Controllers (PIO)
  - Eighty-eight Programmable I/O Lines Multiplexed with up to Two Peripheral I/Os
  - Input Change Interrupt Capability on Each I/O Line
  - Individually Programmable Open-drain, Pull-up Resistor and Synchronous Output
  - Schmitt Trigger on All inputs
- Eleven Peripheral DMA Controller (PDC) Channels
- One USB 2.0 Full Speed (12 Mbits per second) Device Port
  - On-chip Transceiver, Eight Endpoints, 2688-byte Configurable Integrated FIFOs
- One Synchronous Serial Controller (SSC)
  - Independent Clock and Frame Sync Signals for Each Receiver and Transmitter
  - I²S Analog Interface Support, Time Division Multiplex Support
  - High-speed Continuous Data Stream Capabilities with 32-bit Data Transfer
- Two Universal Synchronous/Asynchronous Receiver Transmitters (USART)
  - Individual Baud Rate Generator, IrDA® Infrared Modulation/Demodulation
  - Support for ISO7816 T0/T1 Smart Card, Hardware Handshaking, RS485 Support
  - Full Modem Line Support on USART1
- One Master/Slave Serial Peripheral Interfaces (SPI)
  - 8- to 16-bit Programmable Data Length, Four External Peripheral Chip Selects
- One Three-channel 16-bit Timer/Counter (TC)
  - Three External Clock Inputs, Two Multi-purpose I/O Pins per Channel
  - Double PWM Generation, Capture/Waveform Mode, Up/Down Capability
- One Four-channel 16-bit PWM Controller (PWMC)
- One Two-wire Interface (TWI)
  - Master, Multi-Master and Slave Mode Support, All Two-wire Atmel EEPROMs Supported
  - General Call Supported in Slave Mode
- One 8-channel 10-bit Analog-to-Digital Converter, Four Channels Multiplexed with Digital I/Os
- SAM-BA™
  - Default Boot program
  - Interface with SAM-BA Graphic User Interface

- IEEE® 1149.1 JTAG Boundary Scan on All Digital Pins
- Four High-current Drive I/O lines, Up to 16 mA Each
- Power Supplies
  - Embedded 1.8V Regulator, Drawing up to 100 mA for the Core and External Components
  - 1.8V or 3,3V VDDIO I/O Lines Power Supply, Independent 3.3V VDDFLASH Flash Power Supply
  - 1.8V VDDCORE Core Power Supply with Brownout Detector
- Fully Static Operation: Up to 48 MHz at 1.65V and 85° C Worst Case Conditions
- Available in a 128-lead LQFP Green Package, or a 144-ball LFBGA RoHS-compliant Package

3.2 AT91SAM7SE Block Diagram

Figure 3-1. AT91SAM7SE Block Diagram



3.3 Memory

- 512 Kbytes of Internal Flash
- 32 KBytes of Internal High Speed SRAM
- 32 Mbytes of SDRAM memory (16-bit bus width)
- 256 Mbytes of NANDFlash memory (8-bit bus width)

3.4 Clock Circuitry

- 18.432 MHz 20 pF miniature AT cut strip crystal
- Internal RC Oscillator

3.5 Reset Circuitry

- Internal reset controller with a bi-directional reset pin
- External reset push button

3.6 Power Supply Circuitry

- Embedded 1.8V regulator (drawing up to 100 mA for the core and external components)
- On board 3.3V linear regulator

3.7 Remote Communication

- One Serial interface (DBGU COM Port) via RS-232 DB9 male connectors
- One additional serial interface (COM Port 0) with RTS/CTS handshake control via RS-232 DB9 male connectors
- USB V2.0 Full-speed compliant, 12 Mbits per Second (UDP)

3.8 Audio Stereo Interface

- One Atmel stereo audio DAC (AT73C213)
- One 32 Ohm/20 mW Stereo Headset output (J3) with master volume and mute controls

3.9 User Interface

- One 5-way joystick (4 directions and push for confirmation)
- Two user input pushbuttons
- Two user green LEDs
- One yellow power LED (can be also software controlled)

3.10 Debug Interface

- 20-pin JTAG/ICE interface connector
- DBGU COM Port

3.11 Expansion Slot

- All I/Os of the AT91SAM7SE are routed to peripheral extension connectors

- All EBI Signals of the AT91SAM7SE are routed to extension footprint connectors (J14)

This allows the developer to check the integrity of the components and to extend the features of the board by adding external hardware components or boards.

3.12 PIO Usage

Table 3-1. PIO Controller A

I/O Line	Peripheral A	Peripheral B	Comments	Function
PA0	PWM0	A0_NBS0	High-Drive	Power LED
PA1	PWM1	A1_NBS2	High-Drive	User LED 1
PA2	PWM2	A2	High-Drive	User LED 2
PA3	TWD	A3	High-Drive	EEPROM AT24C256 (SDA)
PA4	TWCK	A4		EEPROM AT24C256 (SCL)
PA5	RXD0	A5		RS232 COM PORT (RXD)
PA6	TXD0	A6		RS232 COM PORT (TXD)
PA7	RTS0	A7		RS232 COM PORT (RTS)
PA8	CTS0	A8		RS232 COM PORT (CTS)
PA9	DRXD	A9		SERIAL DEBUG PORT(RXD)
PA10	DTXD	A10		SERIAL DEBUG PORT(TXD)
PA11	NPCS0	A11		SPI DATAFLASH memory (Chip Select)
PA12	MISO	A12		SPI DATAFLASH & Audio DAC (MISO)
PA13	MOSI	A13		SPI DATAFLASH & Audio DAC (MOSI)
PA14	SPCK	A14		SPI DATAFLASH & Audio DAC (SPCK)
PA15	TF	A15		Audio DAC AT73C213 (LRFS)
PA16	TK	A16_BA0		Audio DAC AT73C213 (BCLK)
PA17	TD	A17_BA1	AD0	Audio DAC AT73C213 (SDIN)
PA18	RD	NBS3_CFIOW	AD1	
PA19	RK	NCS4_CFCS0	AD2	
PA20	RF	NCS2_CFCS2	AD3	ETHERNET DM9000A (Chip Select)
PA21	RXD1	NCS6_CFCE2		
PA22	TXD1	NCS5_CFCE1		
PA23	SCK1	NWR1_NBS1_CFIOR		SDRAM DEVICE (NBS1)
PA24	RTS1	SDA10		SDRAM DEVICE (SDA10)
PA25	CTS1	SDCKE		SDRAM DEVICE (SDCKE)
PA26	DCD1	NCS1_SDCS		SDRAM DEVICE (Chip Select)
PA27	DTR1	SDWE		SDRAM DEVICE (SDWE)
PA28	DSR1	CAS		SDRAM DEVICE (CAS)

Table 3-1. PIO Controller A (Continued)

I/O Line	Peripheral A	Peripheral B	Comments	Function
PA29	RI1	RAS		SDRAM DEVICE (RAS)
PA30	IRQ1	D30		ETHERNET DM9000A (IRQ)
PA31	NPCS1	D31		SPI Audio DAC AT73C213 (Chip Select)

Table 3-2. PIO Controller B

I/O Line	Peripheral A	Peripheral B	Comments	Function
PB0	TIOA0	A0_NBS0		ADDRES BUS (PB0..PB17)
PB1	TIOB0	A1_NBS2		
PB2	SCK0	A2		
PB3	NPCS3	A3		
PB4	TCLK0	A4		
PB5	NPCS3	A5		
PB6	PCK0	A6		
PB7	PWM3	A7		
PB8	ADTRG	A8		
PB9	NPCS1	A9		
PB10	NPCS2	A10		
PB11	PWM0	A11		
PB12	PWM1	A12		
PB13	PWM2	A13		
PB14	PWM3	A14		
PB15	TIOA1	A15		
PB16	TIOB1	A16_BA0		
PB17	PCK1	A17_BA1		
PB18	PCK2	D16		NandFlash (NANDCS)
PB19	FIQ	D17		NandFlash (RDYBSY)
PB20	IRQ0	D18		
PB21	PCK1	D19		
PB22	NPCS3	D20		RIGHT clic push button
PB23	PWM0	D21		Joystick UP
PB24	PWM1	D22		Joystick DOWN
PB25	PWM2	D23		Joystick LEFT
PB26	TIOA2	D24		Joystick RIGHT
PB27	TIOB2	D25		Joystick PUSH and LEFT clic push button
PB28	TCLK1	D26		

Table 3-2. PIO Controller B (Continued)

I/O Line	Peripheral A	Peripheral B	Comments	Function
PB29	TCLK2	D27		
PB30	NPCS2	D28		
PB31	PCK2	D29		Audio DAC AT73C213 (MCLK)

Table 3-3. PIO Controller C

I/O Line	Peripheral A	Peripheral B	Comments	Function
PC0	D0			DATA BUS (PC0..PC15)
PC1	D1			
PC2	D2			
PC3	D3			
PC4	D4			
PC5	D5			
PC6	D6			
PC7	D7			
PC8	D8	RTS1		
PC9	D9	DTR1		
PC10	D10	PCK0		
PC11	D11	PCK1		
PC12	D12	PCK2		
PC13	D13			
PC14	D14	NPCS1		
PC15	D15	NCS3_NANDCS		
PC16	A18	NWAIT		
PC17	A19	NANDOE		NandFlash (NANDOE)
PC18	A20	NANDWE		NandFlash (NANDWE)
PC19	A21			USB_CNX (VBUS DETECT) and NandFlash (ALE). See errata section
PC20	A22	NCS7		NandFlash (CLE)
PC21		NWR0_NWE_CFWE		
PC22		NRD_CFOE		
PC23	CFRNW	NCS0		

Section 4

Configuration

4.1 Jumpers

Table 4-1. Jumpers

Designation	Default Setting	Feature
J2	Closed	3.3V Jumper (1)
J5-1	Opened	Erases all internal Flash memory when the board is powered. To do so, the user will have to close this jumper for at least 10 ms.
J5-2	Closed	VDDIO Jumper(1)
J5-3	Closed	VDDCORE Jumper (1)
J5-4	Closed	VDDIN Jumper (1)
J5-5	Closed	VDDPLL Jumper (1)
J5-6	Closed	VDDFLASH Jumper (1)

Note: 1. These jumpers are provided for power consumption measurement use. By default, they are closed. To use this feature, the user has to open the strap and insert an anmeter.

4.2 Audio Configuration

Table 4-2. Audio Configuration

Designation	Default Setting	Feature
R5	Soldered	Enables the use of the audio stereo DAC AT73C213

4.3 JTAG/ICE

Table 4-3. JTAG/ICE Configuration

Designation	Default Setting	Feature
S1	Opened	Selects ICE mode or JTAG mode (Closed)
R11	Soldered	Enables the ICE NRST input

4.4 Microcontroller Clock

Table 4-4. Microcontroller Clock Configuration

Designation	Default Setting	Feature
R13/R15	Soldered	Enables the use of 18.432MHz crystal. If external clock used, R13/R15 must be unsoldered and S3 closed.
S3	Opened	

4.5 Memory

Table 4-5. Memory Configuration

Designation	Default Setting	Feature
SDRAM		
R18	Soldered	Enables MN4 Chip select access
NAND FLASH (MN6x)		
R22	Soldered	Enables the use of NANDFlash (MN6x)
R20	Soldered	Enables the use of Ready Busy signal
S5	Opened	Disables write protect
SERIAL DATAFLASH (MN5) (NOT POPULATED)		
R26	Soldered	Enables the use of the Serial DataFlash
S4	Opened	Disables the write protect.
TWI SERIAL EEPROM (MN10) (NOT POPULATED)		
R30	Soldered	Enables SCL access
R31	Soldered	Enables SDA access

4.6 Ethernet

NOT POPULATED

Table 4-6. Ethernet Configuration

Designation	Default Setting	Feature
R37	Soldered	Enables the use of the Ethernet controller DM9000A
R11	Soldered	Enables the use of the IRQ Ethernet controller

4.7 Miscellaneous

Refer to Section 3.12 and top level schematic for details on PIO usage.

Table 4-7.

Designation	Default Setting	Feature
R4	Soldered	Enables the software control of the POWER_LED
R51	Soldered	USB DEVICE: Enables the use of the USBCNX signal
R47 R48	Soldered Soldered	DBGU COM Port: Enables the use of DTXD output signal Enables the use of DRXD input
		RS232 COM Port 0: Enables the use of output signals
R58 R59	Soldered	TXD0 RTS0
		RS232 COM Port 0: Enable the use of input signals
R60 R61	Soldered	RXD0 CTS0
TP1	N.A	GND Test point
TP2	N.A	GND Test point.
TP3	N.A	GND Test point.
TP4	N.A	GND Test point.

Refer to Section 2.6, “AT91SAM7SE-EK Block Diagram”.

Section 5

Schematics

5.1 Schematics

This section contains the following schematics:

- Board Layout And Silkscreen Printing - Top View
- Power & Audio & User Interface
- AT91SAM7SE512-LQFP128
- Memory
- Ethernet
- Serial Interface
- Expansion

POWER SUPPLY

- 5VDC: POWERLED — PWM0
- USER'S INTERFACE: USERLED1 — PWM1; USERLED2 — PWM2; RIGHTCLIC — PB22; UP — PB23; DOWN — PB24; LEFT — PB27; RIGHT — PB26; PUSHLEFTCLIC — PB25
- DAC: AT73C213: MCLK — PCK2; SDIN — TD; LRFS — TF; BCLK — TK; DOUT — MISO; DIN — MOSI; CLK — SPCK; CS — NPCS1; NRST — NRST

01 - POWER SUPPLY

SERIAL INTERFACES

- RS232: DBGU: DTXD — DTXD; DRXD — DRXD
- RS232: COM0: TXD — TXD0; RXD — RXD0; RTS — RTS0; CTS — CTS0
- USB: DEVICE: USBCNX — PC19; DDM — DDM; DDP — DDP

05 - COMMUNICATION

RMII_MII ETHERNET

- FAST ETHERNET: NOT POPULATED: D[0..15] — D[0..15]; CMD — A12; IOW — NWE; IOR — NRD; CS — NCS2; INT — IRQ1; PWRST — NRST

03 - RMII_MII ETHERNET

AT91SAM7SE

SDCK

PA[0..31]
PB[0..31]
PC[0..23]
NRST
AD[4..7]

02 - AT91SAM7SE

MEMORY

D[0..31]
A[0..22]

- SDRAM: D[0..15] — D[0..15]; A[2..14] — A[2..14]; RAS — RAS; CAS — CAS; SDA10 — SDA10; SDWE — SDWE; SDCS — SDCS; SDCK — SDCK; SDCKE — SDCKE; A0 — NBS0; NBS1 — NBS1; A16 — BA0; A17 — BA1
- NANFLASH: A22 — CLE; A21 — ALE; NANDOE — NANDOE; NANDWE — NANDWE; NANDCS — NANDCS; RDYBSY — RDYBSY; D[0..15] — D[0..15]
- SERIAL DATAFLASH: NOT POPULATED: MOSI — SI; MISO — SO; SPCK — SCK; NPCS0 — CS; NRST — NRST
- SERIAL EEPROM: NOT POPULATED: TWCK — SCL; TWD — SDA

03 - MEMORY

EXPANSION CONNECTORS

D[0..31]
A[0..22]
SDCK
PA[0..31]
PB[0..31]
PC[0..23]
NRST
AD[4..7]

06 - EXPANSION CONNECTORS

PIO USAGE

PA[0..31]	PB[0..31]	PC[0..23]	A[0..22]	D[0..31]
PA0 PWM0	PB0	PC0	PB0 A0	PC0 D0
PA1 PWM1	PB1	PC1	PB1 A1	PC1 D1
PA2 PWM2	PB2	PC2	PB2 A2	PC2 D2
PA3 TWD	PB3	PC3	PB3 A3	PC3 D3
PA4 TWCK	PB4	PC4	PB4 A4	PC4 D4
PA5 RXD0	PB5	PC5	PB5 A5	PC5 D5
PA6 TXD0	PB6	PC6	PB6 A6	PC6 D6
PA7 RTS0	PB7	PC7	PB7 A7	PC7 D7
PA8 CTS0	PB8	PC8	PB8 A8	PC8 D8
PA9 DRXD	PB9	PC9	PB9 A9	PC9 D9
PA10 DTXD	PB10	PC10	PB10 A10	PC10 D10
PA11 NPCS0	PB11	PC11	PB11 A11	PC11 D11
PA12 MISO	PB12	PC12	PB12 A12	PC12 D12
PA13 MOSI	PB13	PC13	PB13 A13	PC13 D13
PA14 SPCK	PB14	PC14	PB14 A14	PC14 D14
PA15 TF	PB15	PC15	PB15 A15	PC15 D15
PA16 TK	PB16	PC16	PB16 A16	PB18 D16
PA17 TD	PB17	PC17 NANDOE	PB17 A17	PB19 D17
PA18	PB18 NANDCS	PC18 NANDWE	PC16 A18	PB20 D18
PA19	PB19 RDYBSY	PC19	PC17 A19	PB21 D19
PA20 NCS2	PB20	PC20	PC18 A20	PB22 D20
PA21	PB21	PC21 NWE	PC19 A21	PB23 D21
PA22	PB22	PC22 NRD	PC20 A22	PB24 D22
PA23 NBS1	PB23	PC23		PB25 D23
PA24 SDA10	PB24			PB26 D24
PA25 SDCKE	PB25			PB27 D25
PA26 SDCS	PB26			PB28 D26
PA27 SDWE	PB27			PB29 D27
PA28 CAS	PB28			PB30 D28
PA29 RAS	PB29			PB31 D29
PA30 IRQ1	PB30			PA30 D30
PA31 NPCS1	PB31 PCK2			PA31 D31

ATMEL ROUSSET

REV	MODIF.	DES.	DATE	VER.	DATE
A	INIT EDIT	JPG	12/09/06		

AT91SAM7SE-EK

DIAGRAM

SCALE 1/1

REV. A

SHEET 1/7

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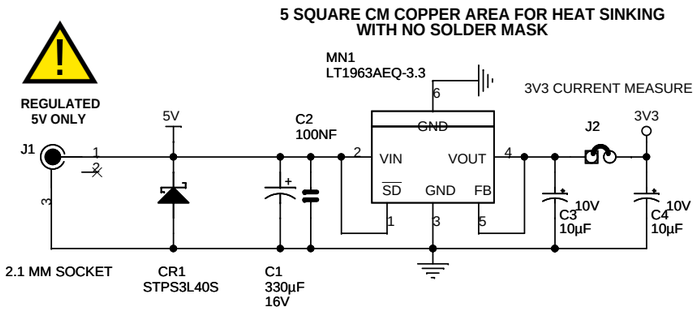

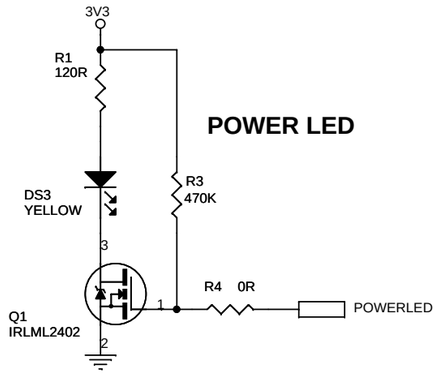

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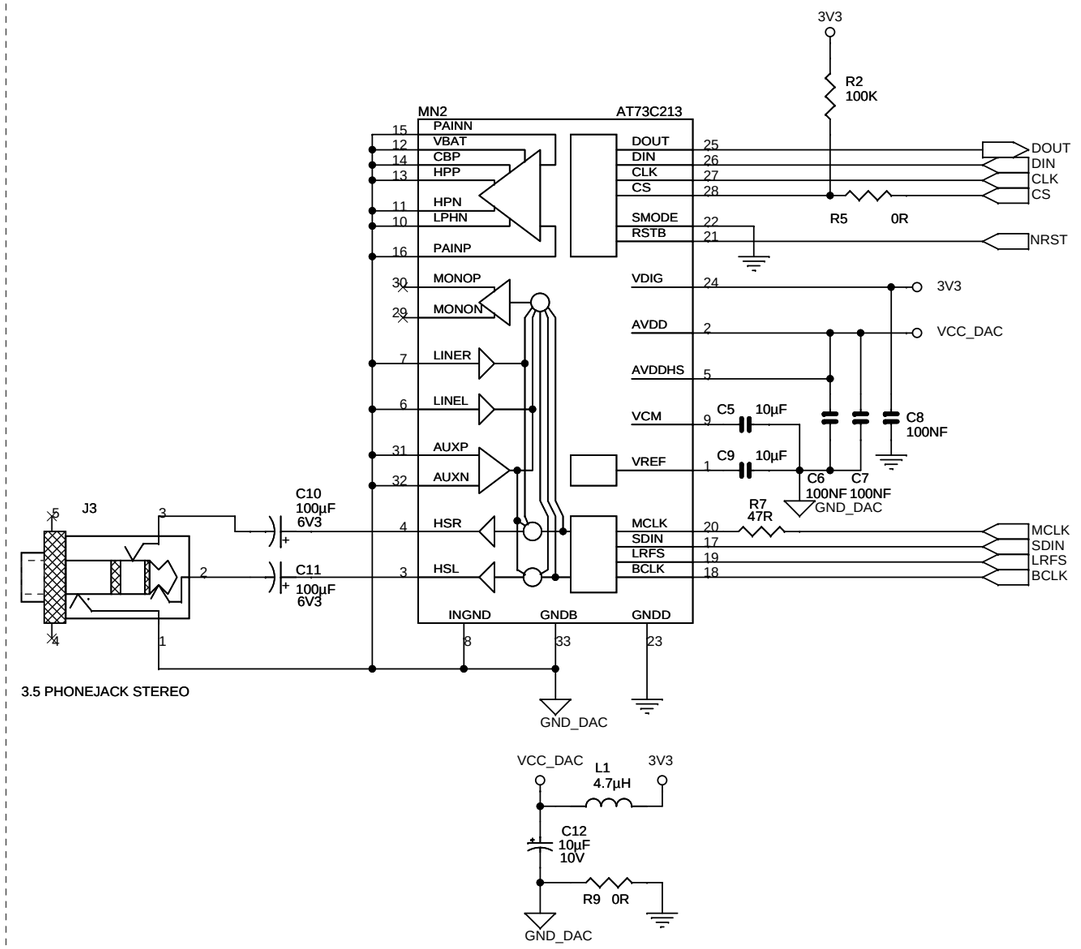

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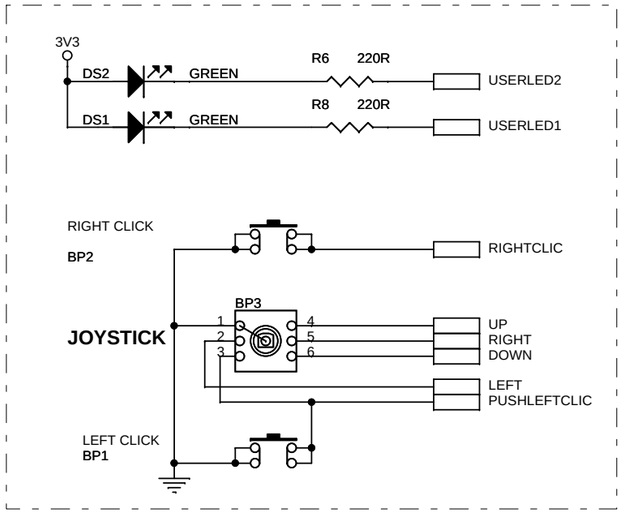

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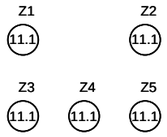

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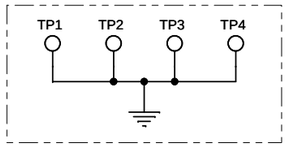

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SCALE 1/1				REV. A	SHEET 2/7

AT91SAM7SE-EK

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AT91SAM7SE512

ICE INTERFACE

3V3
RR1
100K
J4
TDI
TMS
TCK
TDO
JTAGSEL
R11 0R
NRST
S1
3V3
C14
10NF
C15
1NF
R12 1,5K
PLLRC
J5-5
VDDOUT
VDDPLL CURRENT MEASURE
C16
100NF
VDDPLL
C17
NOT POPULATED
R13 0R
XOUT
Y1
18.432MHz
C18
NOT POPULATED
R15 0R
XIN
J6
S3
SMB MALE
NOT POPULATED
PB[0..31]
PC[0..23]
PA[0..31]
MN3
DDP
DDM
DP
DM
J5-4
J5-3
J5-2
J5-6
J5-1
VDDIN
VDDOUT
VDDCORE
VDDIO
VDDFLASH
GND
ERASE
10µF
100NF
C22
C29
C19
C21
C23
C20
C24
C30
C31
C32
C33
C28
C25
C26
C27
VDDCORE CURRENT MEASURE
VDDIO CURRENT MEASURE
VDDFLASH CURRENT MEASURE
SDCK
AD[4..7]
AD7
AD6
AD5
AD4
ADVREF
R10 22R
C13
100NF
S2
TST
NRST
R14
1K
BP4
RESET

REV	MODIF.	DES.	DATE	VER.	DATE
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SCALE 1/1

REV. A

SHEET 3/7

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AT91SAM7SE512-LQFP128

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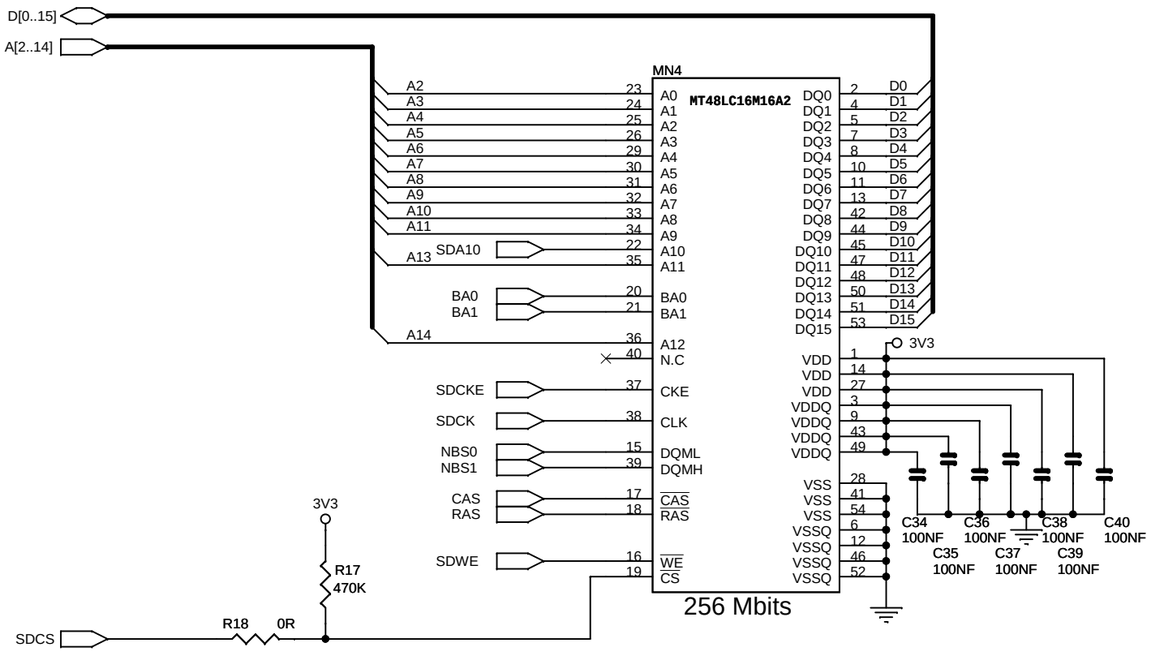
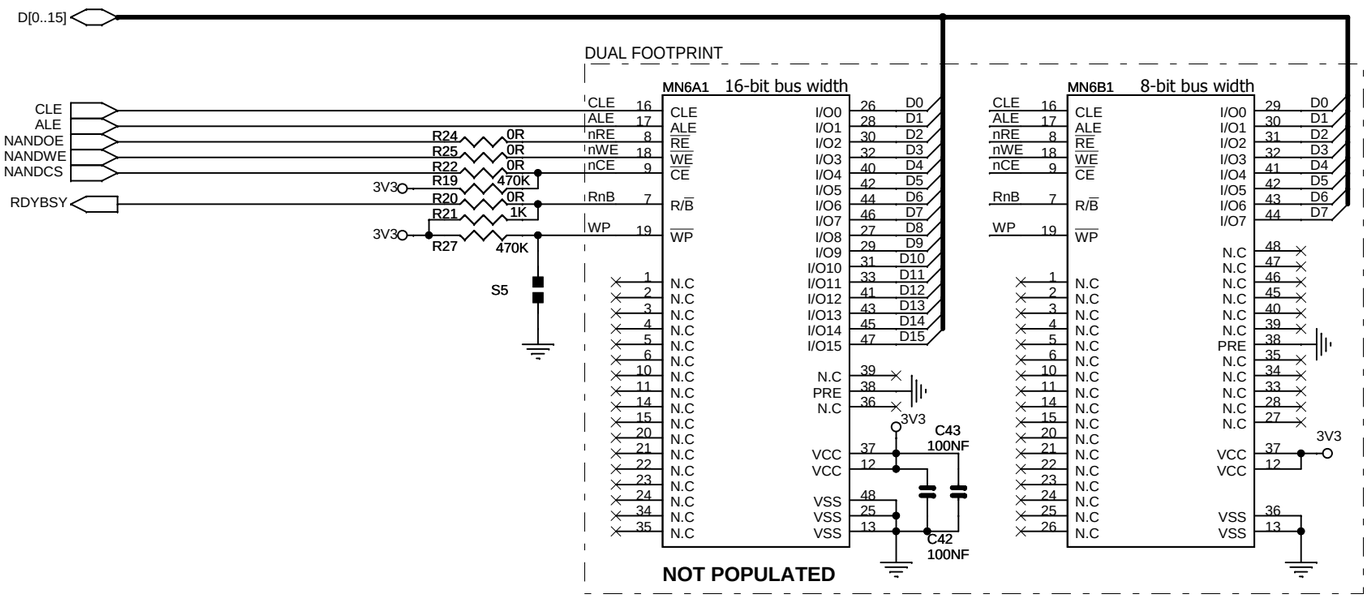


NAND FLASH



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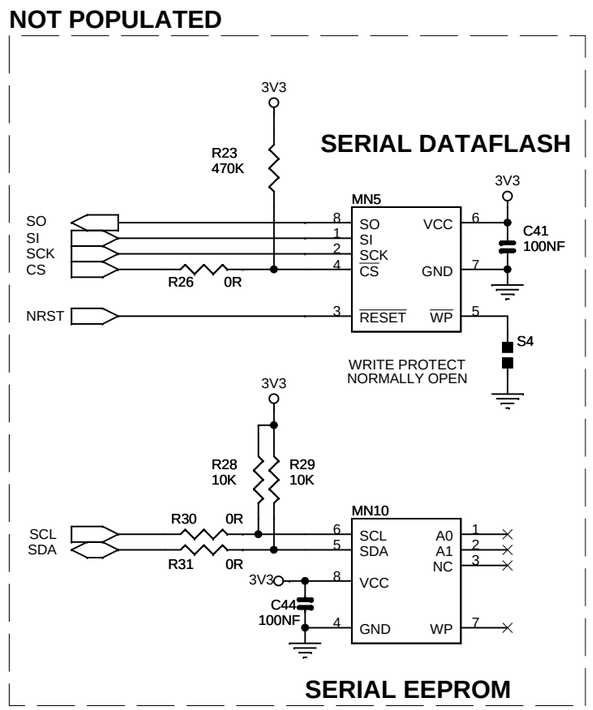

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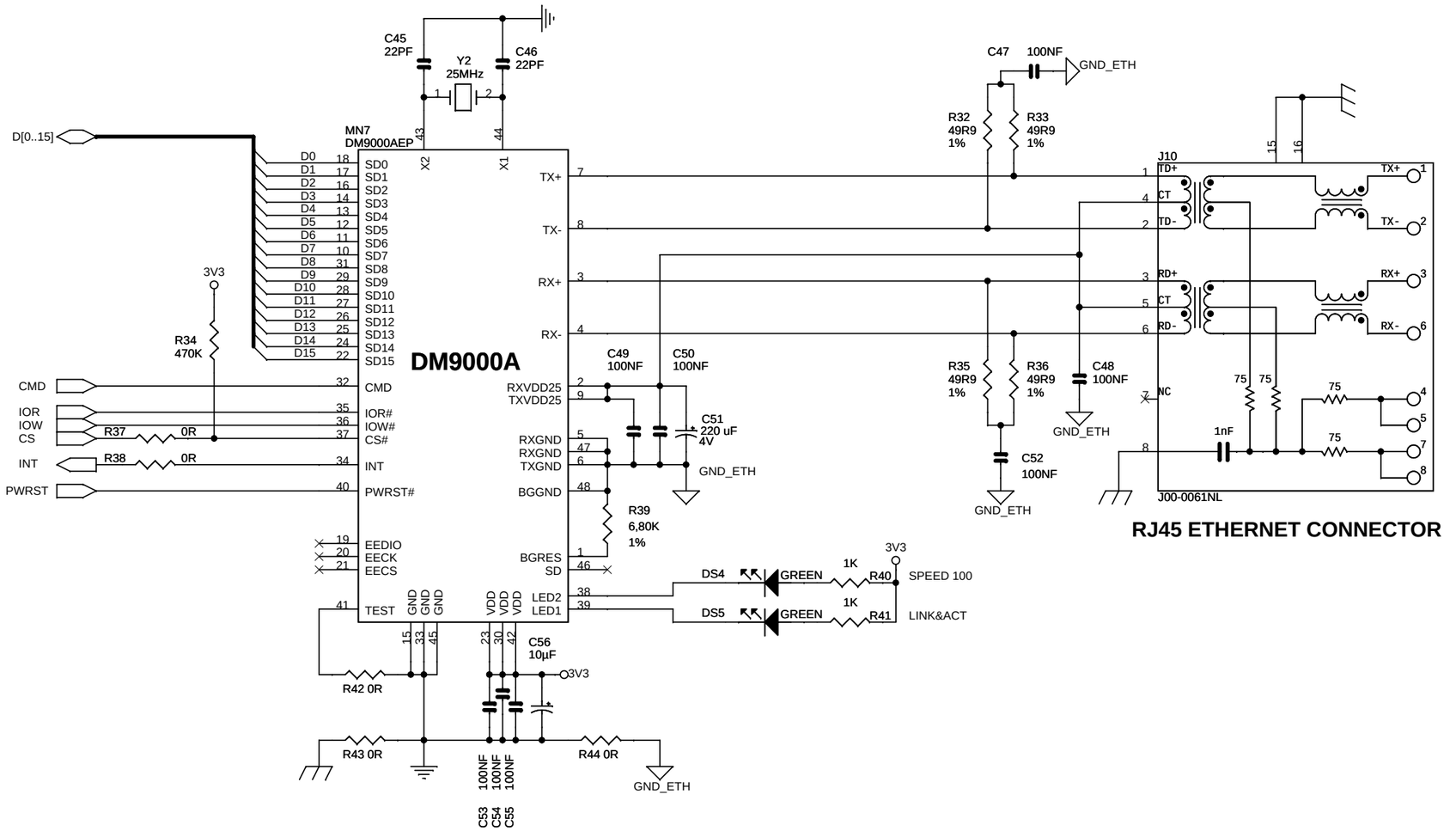

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AT91SAM7SE-EK

ETHERNET

SCALE 1/1

REV. A

SHEET 5/7

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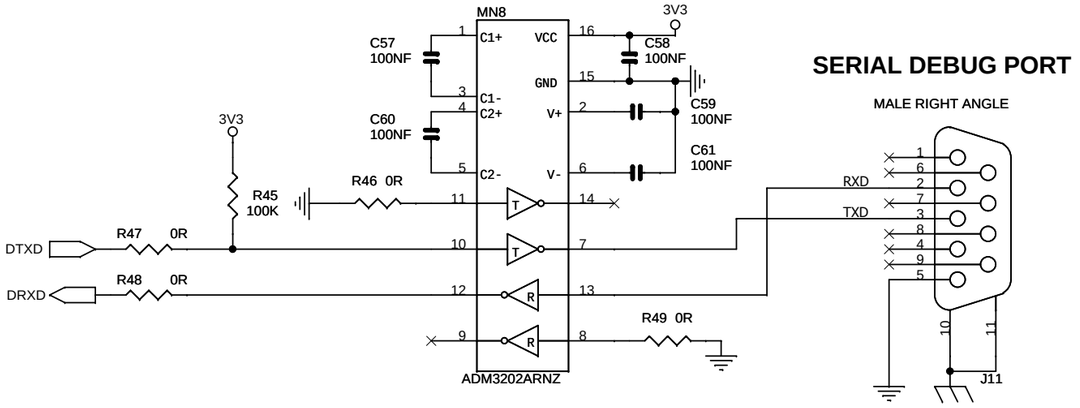
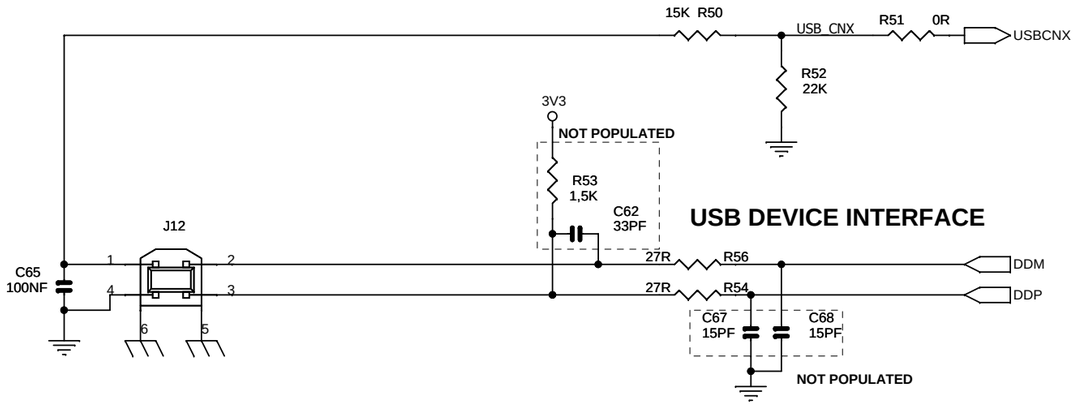
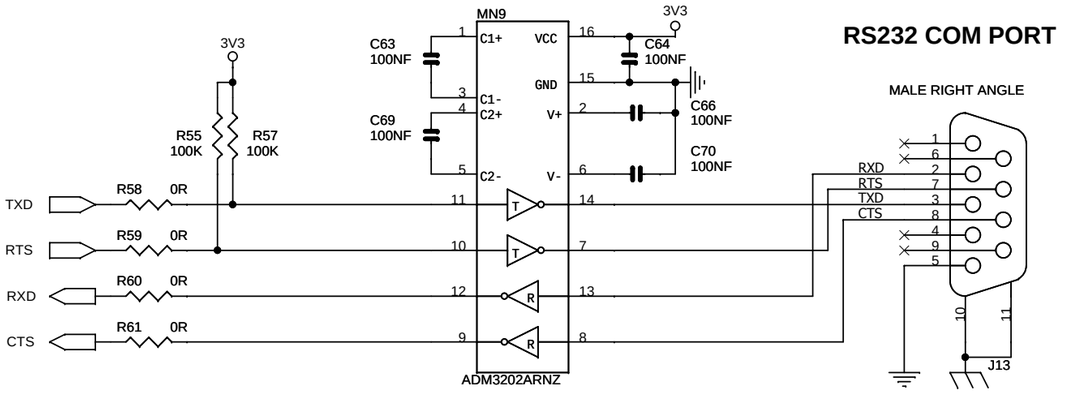
SERIAL DEBUG PORT



USB DEVICE INTERFACE



RS232 COM PORT



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SERIAL INTERFACES

SCALE 1/1

REV. A

SHEET 6/7

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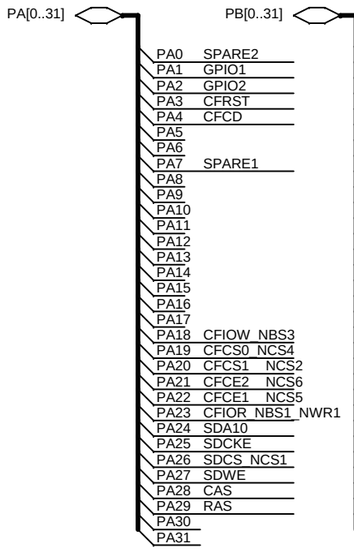

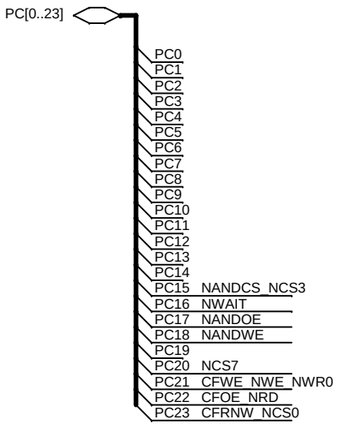

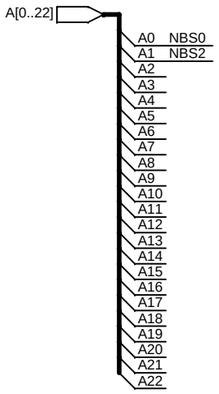

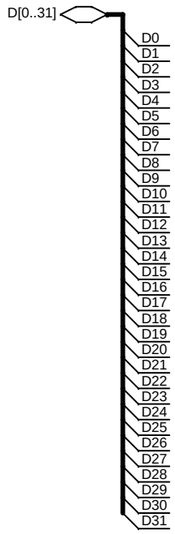

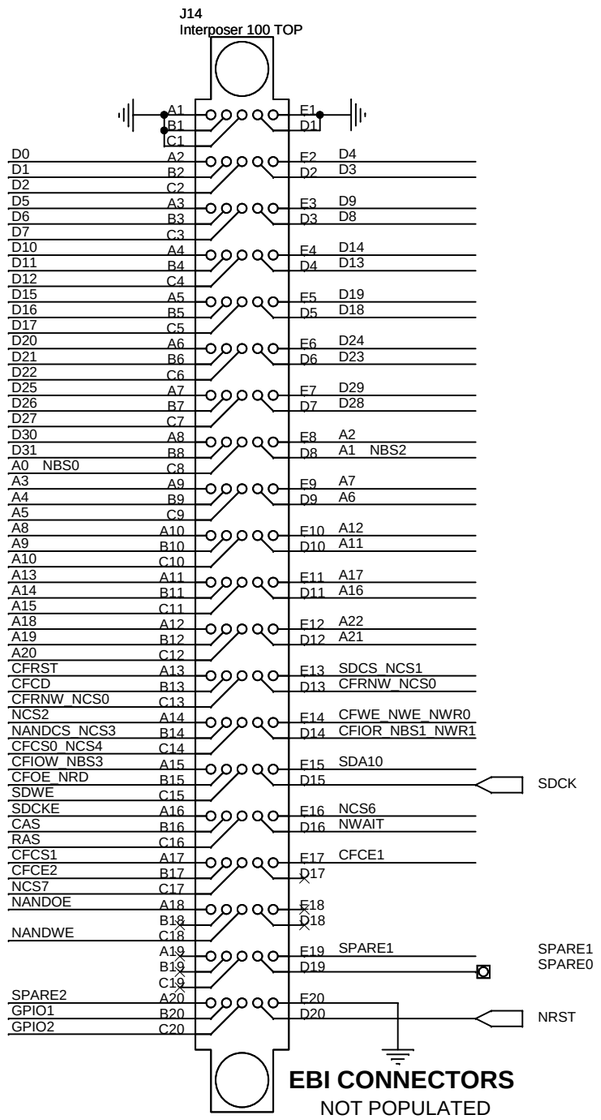

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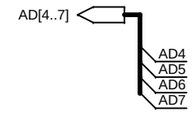
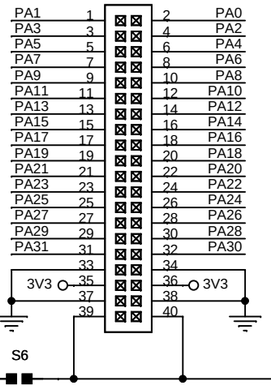


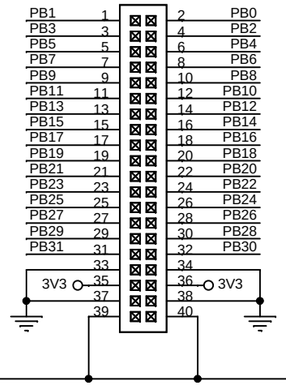
PIO A

J15



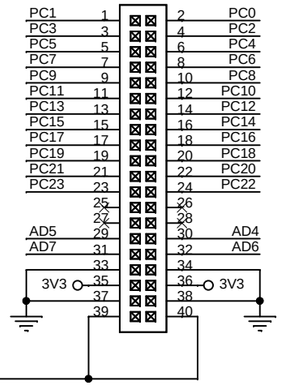
PIO B

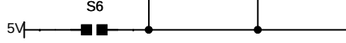
J16



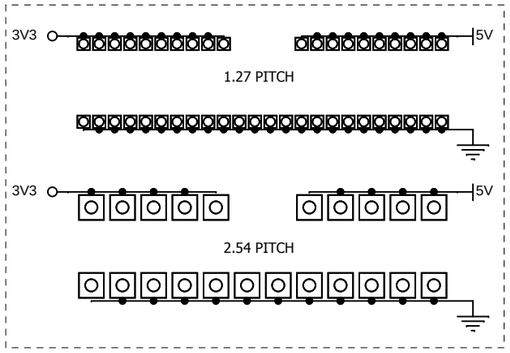
PIO C & ADC

J17





USER'S GRID AERA



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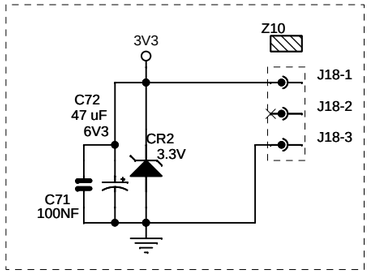

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EXPANSION
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Section 6

Errata

6.1 PIO Usage

The PIO PC19 is erroneously used twice.

USB_CNX (VBUS detect) and A21/ALE (NAND Flash Address Latch Enable) uses this PIO. There is no effect when PC19 is configured as A21 for the NAND Flash usage, but USB_CNX state (VBUS) cannot be read at the same time.

The user has to swap PC19 to input mode to detect the VBUS state, but the NANDFlash cannot be accessed in this configuration.

6.2 TWI line pullups for Fast Mode operation

In order to use the TWI in Fast Mode (up to 400 Kbits/s), the default 10 KΩ resistors R28 and R29 should be replaced by smaller values (e.g., 2.2 KΩ).

Note that there is no need to change the pull-up resistors if the TWI is used in Standard Mode (up to 100 Kbits/s).

6.3 AT73C213 clocking

In the schematics (sheet 1/7, ”AT91SAM7SE-EK Diagram”), the MCLK and BCLK sources implementation does not guarantee a correct phase relation as specified in the AT73C213 datasheet.

Problem Fix/Workaround

In his own design, the user must make sure the BCLK and MCLK clocks generation implements the timing specified in the AT73C213 datasheet.

Section 7

Revision History

7.1 Revision History

Table 7-1.

Document	Comments	Change Request Ref.
6241A	First issue.	
6241B	Added errata Section 6.2 ”TWI line pullups for Fast Mode operation” . Added errata Section 6.3 ”AT73C213 clocking” .	4085 4226

Atmel Corporation

2325 Orchard Parkway
San Jose, CA 95131, USA
Tel: 1(408) 441-0311
Fax: 1(408) 487-2600

Regional Headquarters

Atmel Europe

Le Krebs
8, rue Jean-Pierre Timbaud
BP 309
78054 Saint-Quentin-en-Yvelines
Cedex
France
Tel: (33) 1-30-60-70-00
Fax: (33) 1-30-60-71-11

Asia

Room 1219
Chinachem Golden Plaza
77 Mody Road Tsimshatsui
East Kowloon
Hong Kong
Tel: (852) 2721-9778
Fax: (852) 2722-1369

Japan

9F, Tonetsu Shinkawa Bldg.
1-24-8 Shinkawa
Chuo-ku, Tokyo 104-0033
Japan
Tel: (81) 3-3523-3551
Fax: (81) 3-3523-7581

Atmel Operations

Memory

2325 Orchard Parkway
San Jose, CA 95131, USA
Tel: 1(408) 441-0311
Fax: 1(408) 436-4314

Microcontrollers

2325 Orchard Parkway
San Jose, CA 95131, USA
Tel: 1(408) 441-0311
Fax: 1(408) 436-4314

La Chantrerie
BP 70602
44306 Nantes Cedex 3, France
Tel: (33) 2-40-18-18-18
Fax: (33) 2-40-18-19-60

ASIC/ASSP/Smart Cards

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13106 Rousset Cedex, France
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Fax: (33) 4-42-53-60-01

1150 East Cheyenne Mtn. Blvd.
Colorado Springs, CO 80906, USA
Tel: 1(719) 576-3300
Fax: 1(719) 540-1759

Scottish Enterprise Technology Park
Maxwell Building
East Kilbride G75 0QR, Scotland
Tel: (44) 1355-803-000
Fax: (44) 1355-242-743

RF/Automotive

Theresienstrasse 2
Postfach 3535
74025 Heilbronn, Germany
Tel: (49) 71-31-67-0
Fax: (49) 71-31-67-2340

1150 East Cheyenne Mtn. Blvd.
Colorado Springs, CO 80906, USA
Tel: 1(719) 576-3300
Fax: 1(719) 540-1759

Biometrics

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