



SM802109

ClockWorks™ PCI-e Quad 100MHz Ultra-Low Jitter, HCSL Frequency Synthesizer

General Description

The SM802109 is a member of the ClockWorks™ family of devices from Micrel and provides an extremely low-noise timing solution for PCI-Express clock signals. It is based on a unique patented RotaryWave® architecture that provides very-low phase noise.

The device operates from a 3.3V or 2.5V power supply and synthesizes four HCSL output clocks at 100MHz. The SM802109 accepts a 25MHz crystal or LVCMOS reference clock.

Data sheets and support documentation can be found on Micrel's web site at: www.micrel.com.

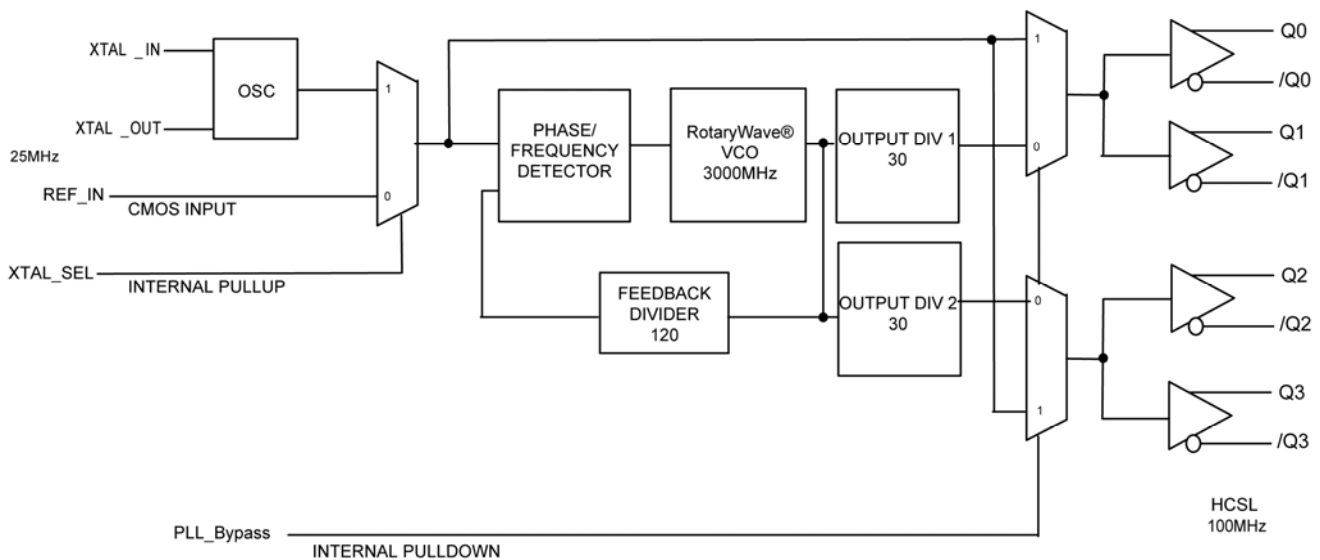
Features

- Generates four HCSL clock outputs at 100MHz
- 2.5V or 3.3V operating range
- Typical phase jitter @ 100MHz (1.875MHz to 20MHz): 105fs
- Industrial temperature range (–40°C to +85°C)
- Green, RoHS, and PFOS compliant
- Available in 24-pin 4mm × 4mm QFN package

Applications

- PCI-Express

Block Diagram



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RotaryWave is a registered trademark of Multigig, Inc.

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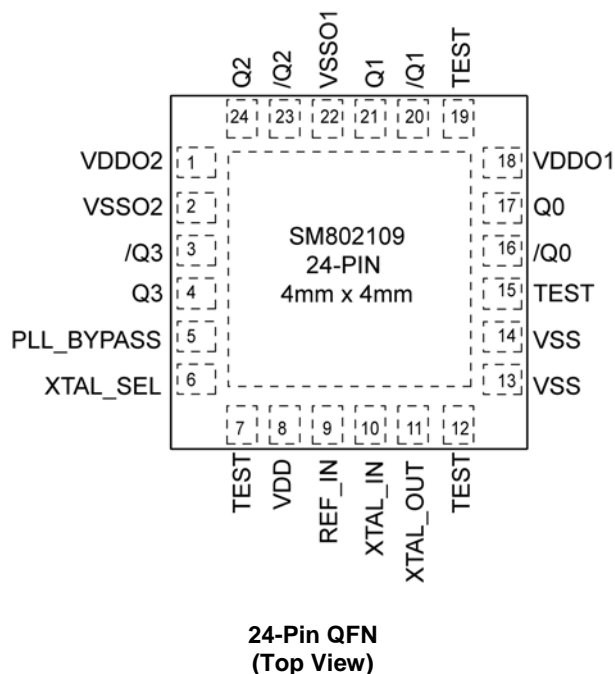
Ordering Information⁽¹⁾

| Part Number | Marking | Shipping | Temperature Range | Package |
|---------------|---------|---------------|-------------------|------------|
| SM802109UMG | 802109 | Tube | -40°C to +85°C | 24-Pin QFN |
| SM802109UMGTR | 802109 | Tape and Reel | -40°C to +85°C | 24-Pin QFN |

Note:

1. Devices are Green, RoHS, and PFOS compliant.

Pin Configuration



Pin Description

| Pin Number | Pin Name | Pin Type | Pin Level | Pin Function |
|------------------|--------------------|----------|-----------|--|
| 16, 17 20, 21 | /Q0, Q0 /Q1, Q1 | O, (DIF) | HCSL | Differential Clock Outputs from Bank 1 100MHz |
| 23, 24 3, 4 | /Q2, Q2 /Q3, Q3 | O, (DIF) | HCSL | Differential Clock Outputs from Bank 2 100MHz |
| 1 | VDDO2 | PWR | | Power Supply for Output Bank 2 |
| 2 | VSSO2 | PWR | | Power Supply Ground for Output Bank 2 |
| 5 | PLL_BYPASS | I, (SE) | LVC MOS | PLL Bypass, Selects Output Source 0 = Normal PLL Operation 1 = Output from Input Reference Clock or Crystal 45KΩ pulldown |
| 6 | XTAL_SEL | I, (SE) | LVC MOS | Selects PLL Input Reference Source 0 = REF_IN, 1 = XTAL, 45KΩ pullup |

Pin Description (Continued)

| Pin Number | Pin Name | Pin Type | Pin Level | Pin Function |
|---------------|----------------------|----------|-----------|--|
| 7, 12, 15, 19 | TEST | | | Factory Test pins, Do not connect anything to these pins. |
| 8 | VDD | PWR | | Core Power Supply |
| 13, 14 | VSS (Exposed Pad) | PWR | | Core Power Supply Ground. The exposed pad must be connected to the VSS ground plane. |
| 18 | VDDO1 | PWR | | Power Supply for Output Bank 1 |
| 22 | VSSO1 | PWR | | Power Supply Ground for Output Bank 1 |
| 9 | REF_IN | I, (SE) | LVC MOS | Reference Clock Input |
| 10 | XTAL_IN | I, (SE) | Crystal | Crystal Reference Input, no load caps needed (see Figure 5). |
| 11 | XTAL_OUT | O, (SE) | Crystal | Crystal Reference Output, no load caps needed (see Figure 5). |

Truth Table

| PLL_BYPASS | XTAL_SEL | INPUT | OUTPUT |
|------------|----------|--------|-------------|
| 0 | – | – | PLL |
| 1 | – | – | XTAL/REF_IN |
| – | 0 | REF_IN | – |
| – | 1 | XTAL | – |

Absolute Maximum Ratings⁽¹⁾

| | |
|--|---------------------------|
| Supply Voltage (V_{DD} , $V_{DDO1/2}$) | +4.6V |
| Input Voltage (V_{IN}) | -0.50V to $V_{DD} + 0.5V$ |
| Lead Temperature (soldering, 20s) | 260°C |
| Case Temperature | 115°C |
| Storage Temperature (T_s) | -65°C to +150°C |

Operating Ratings⁽²⁾

| | |
|--|--------------------|
| Supply Voltage (V_{DD} , $V_{DDO1/2}$) | +2.375V to +3.465V |
| Ambient Temperature (T_A) | -40°C to +85°C |
| Junction Thermal Resistance ⁽³⁾ | |
| QFN (θ_{JA}) | |
| Still-Air | 50°C/W |
| QFN (ψ_{JB}) | |
| Junction-to-Board | 30°C/W |

DC Electrical Characteristics⁽⁴⁾

$V_{DD} = V_{DDO1/2} = 3.3V \pm 5\%$ or $2.5V \pm 5\%$
 $V_{DD} = 3.3V \pm 5\%$, $V_{DDO1/2} = 3.3V \pm 5\%$ or $2.5V \pm 5\%$
 $T_A = -40^\circ C$ to $+85^\circ C$.

| Symbol | Parameter | Condition | Min. | Typ. | Max. | Units |
|-------------------------|-----------------------------------|---|-------|------|-------|-------|
| V_{DD} , $V_{DDO1/2}$ | 2.5V Operating Voltage | | 2.375 | 2.5 | 2.625 | V |
| V_{DD} , $V_{DDO1/2}$ | 3.3V Operating Voltage | | 3.135 | 3.3 | 3.465 | V |
| I_{DD} REF_IN | Supply current $V_{DD} + V_{DDO}$ | XTAL_SEL = 0 Outputs 50Ω to V_{SS} | | 140 | 175 | mA |
| I_{DD} XTAL | Supply current $V_{DD} + V_{DDO}$ | XTAL_SEL = 1 Outputs 50Ω to V_{SS} | | 150 | 185 | mA |

HCSL DC Electrical Characteristics⁽⁴⁾

$V_{DD} = V_{DDO1/2} = 3.3V \pm 5\%$ or $2.5V \pm 5\%$
 $V_{DD} = 3.3V \pm 5\%$, $V_{DDO1/2} = 3.3V \pm 5\%$ or $2.5V \pm 5\%$
 $T_A = -40^\circ C$ to $+85^\circ C$. $R_L = 50\Omega$ to V_{SS}

| Symbol | Parameter | Condition | Min | Typ. | Max. | Units |
|-------------|------------------------|-----------|------|------|------|-------|
| V_{OH} | Output High Voltage | | 660 | 700 | 850 | mV |
| V_{OL} | Output Low Voltage | | -150 | 0 | 27 | mV |
| V_{CROSS} | Crossing Point Voltage | | 250 | 350 | 550 | mV |

Notes:

1. Permanent device damage may occur if absolute maximum ratings are exceeded. This is a stress rating only and functional operation is not implied at conditions other than those detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
2. The data sheet limits are not guaranteed if the device is operated beyond the operating ratings.
3. Package thermal resistance assumes exposed pad is soldered (or equivalent) to the devices most negative potential on the PCB.
4. The circuit is designed to meet the AC and DC specifications shown in the above table(s) after thermal equilibrium has been established.

LVC MOS (PLL_BYPASS, XTAL_SEL) DC Electrical Characteristics⁽⁴⁾

$V_{DD} = 3.3V \pm 5\%$, or $2.5V \pm 5\%$, $T_A = -40^\circ C$ to $+85^\circ C$.

| Symbol | Parameter | Condition | Min. | Typ. | Max. | Units |
|----------|--------------------|--------------------------------|------|------|----------------|---------|
| V_{IH} | Input High Voltage | | 2 | | $V_{DD} + 0.3$ | V |
| V_{IL} | Input Low Voltage | | -0.3 | | 0.8 | V |
| I_{IH} | Input High Current | $V_{DD} = V_{IN} = 3.465V$ | | | 150 | μA |
| I_{IL} | Input Low Current | $V_{DD} = 3.465V, V_{IN} = 0V$ | -150 | | | μA |

REF_IN DC Electrical Characteristics⁽⁴⁾

$V_{DD} = 3.3V \pm 5\%$, or $2.5V \pm 5\%$, $T_A = -40^\circ C$ to $+85^\circ C$.

| Symbol | Parameter | Condition | Min. | Typ. | Max. | Units |
|----------|--------------------|---|------|------|----------------|---------|
| V_{IH} | Input High Voltage | | 1.1 | | $V_{DD} + 0.3$ | V |
| V_{IL} | Input Low Voltage | | -0.3 | | 0.6 | V |
| I_{IN} | Input Current | $XTAL_SEL = V_{IL}, V_{IN} = 0V$ to V_{DD} | -5 | | 5 | μA |
| | | $XTAL_SEL = V_{IH}, V_{IN} = V_{DD}$ | | 20 | | μA |

Crystal Characteristics

| Parameter | Condition | Min. | Typ. | Max. | Units |
|------------------------------------|-------------------|---------------------------------------|------|------|----------|
| Mode of Oscillation | 10pF to 12pF Load | Fundamental, Parallel Resonant | | | |
| Frequency | | | 25 | | MHz |
| Equivalent Series Resistance (ESR) | | | | 50 | Ω |
| Shunt Capacitor, C0 | | | 1 | 5 | pF |
| Correlation Drive Level | | | 10 | 100 | μW |

AC Electrical Characteristics^(4, 5)
 $V_{DD} = V_{DDO1/2} = 3.3V \pm 5\% \text{ or } 2.5V \pm 5\%$
 $V_{DD} = 3.3V \pm 5\%, V_{DDO1/2} = 3.3V \pm 5\% \text{ or } 2.5V \pm 5\%$
 $T_A = -40^\circ\text{C to } +85^\circ\text{C. } R_L = 50\Omega \text{ to } V_{SS}$

| Symbol | Parameter | Condition | Min. | Typ. | Max. | Units |
|--------------------------------|---------------------------------|---|------|------------|------|-------|
| F _{OUT} | Output Frequency | | | 100 | | MHz |
| F _{REF} | Reference Input Frequency | | | 25 | | MHz |
| T _R /T _F | LVPECL Output Rise/Fall Time | 20% – 80% | 150 | 300 | 450 | ps |
| ODC | Output Duty Cycle | | 48 | 50 | 52 | % |
| T _{SKEW} | Output-to-Output Skew | Note 6 | | | 45 | ps |
| T _{LOCK} | PLL Lock Time | | | | 20 | ms |
| T _{jitter} (∅) | RMS Phase Jitter ⁽⁷⁾ | 100MHz Integration Range (1.875MHz – 20MHz) Integration Range (12kHz – 20MHz) | | 105 250 | | fs |
| | Spurious Noise Components | 25MHz | | -95 | | dBc |

Notes:

5. All phase noise measurements were taken with an Agilent 5052B phase noise system.
6. Defined as skew between outputs at the same supply voltage and with equal load conditions; measured at the output differential crossing points.
7. Measured using 25MHz crystal as the input reference source. If using an external reference input, use a low phase noise source. With an external reference, the phase noise will follow the input source phase noise up to about 1MHz.

Application Information

Input Reference

When operating with a crystal input reference, do not apply a switching signal to REF_IN.

Crystal Layout

Keep the layers under the crystal as open as possible and do not place switching signals or noisy supplies under the crystal.

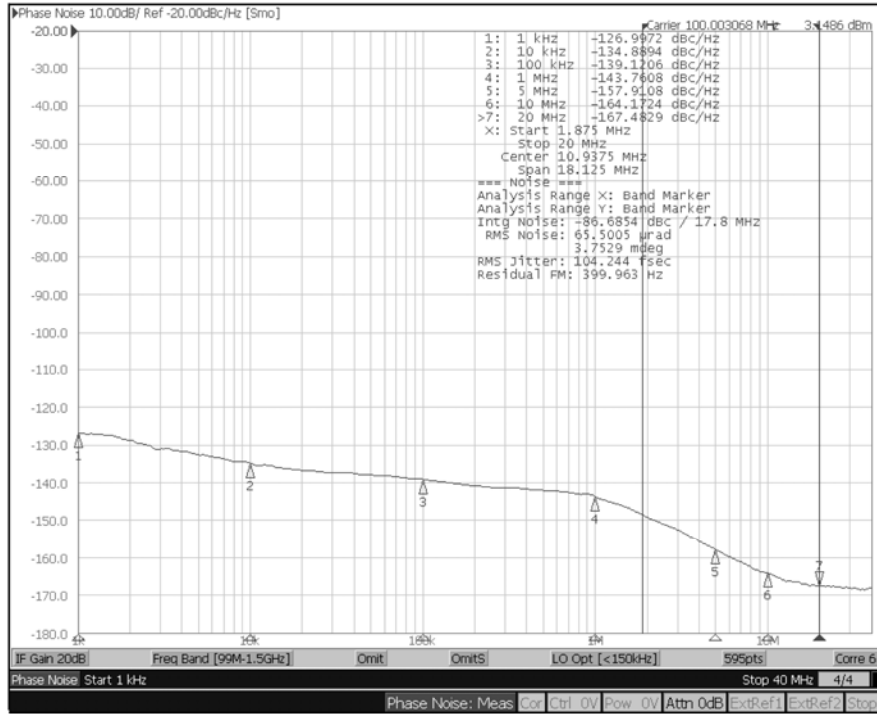
Crystal load capacitance is built inside the die so no external capacitance is needed. See the *Selecting a Quartz crystal for the Clockworks Flex I Family of Precision Synthesizers* application note for further details.

Contact Micrel's HBW applications group if you need assistance on selecting a suitable crystal for your application at: hbwhelp@micrel.com.

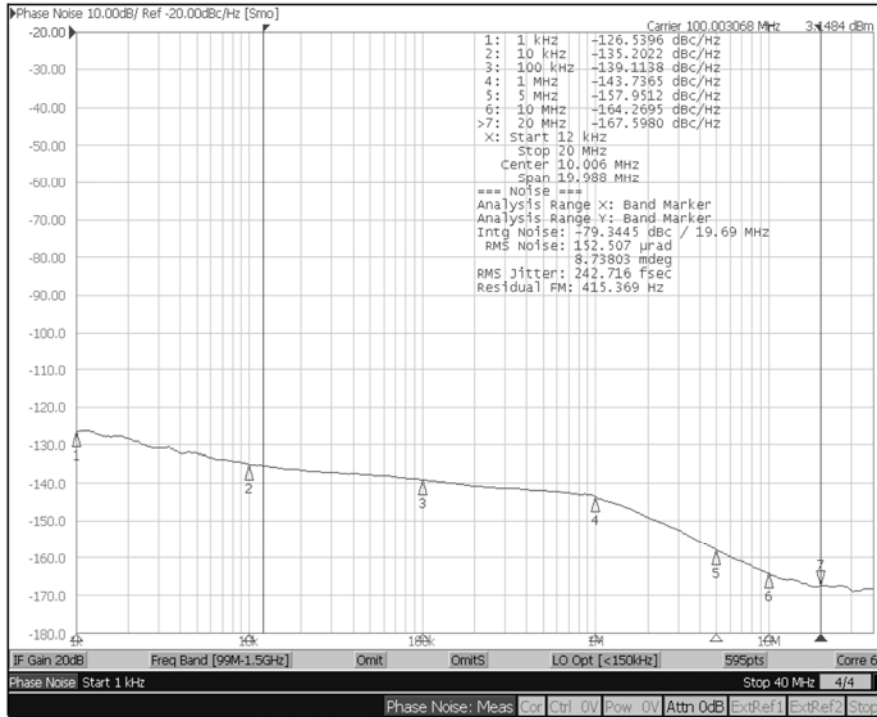
HCSL Outputs

HCSL outputs are to be terminated with 50Ω to V_{SS} . For best performance load all outputs. If you want to AC-couple or change the termination, contact Micrel's application group: hbwhelp@micrel.com.

Phase Noise Plots



Phase Noise Plot: 100MHz, 1.875MHz – 20MHz 104fS



Phase Noise Plot: 100MHz, 12kHz – 20MHz 242fS

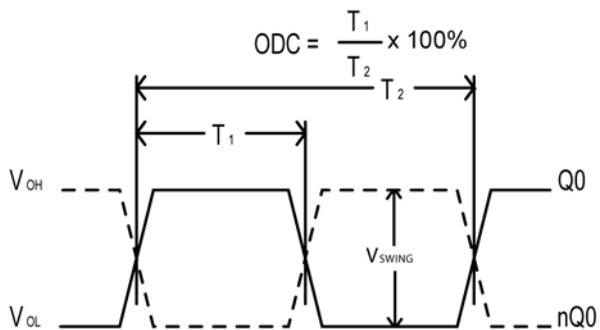


Figure 1. Duty Cycle Timing

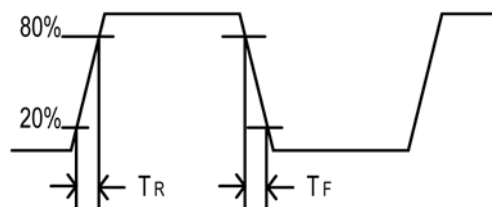


Figure 2. All Outputs Rise/Fall Time

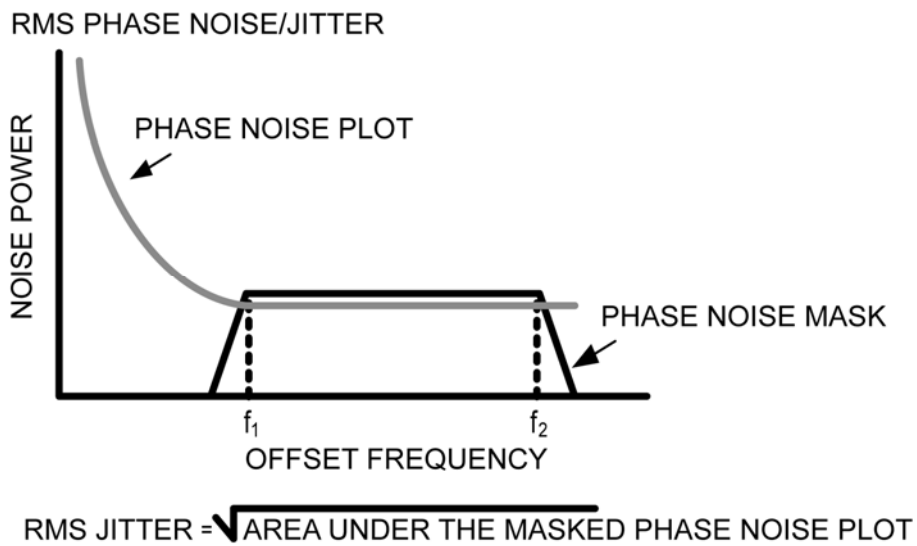


Figure 3. RMS Phase/Noise Jitter

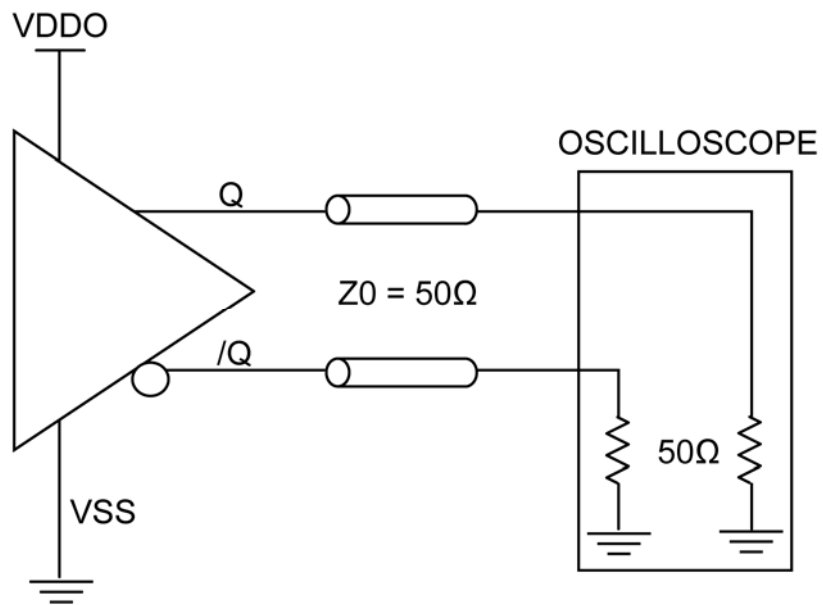


Figure 4. HCSL Output Load and Test Circuit

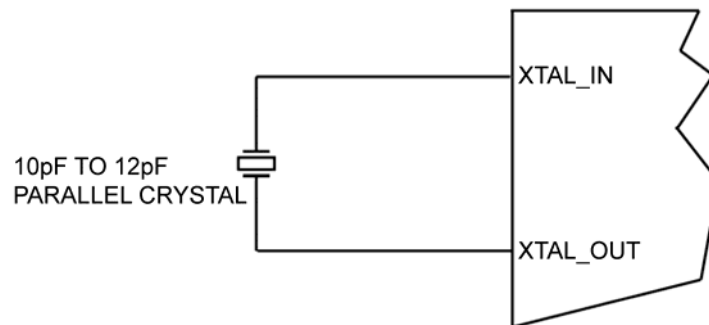
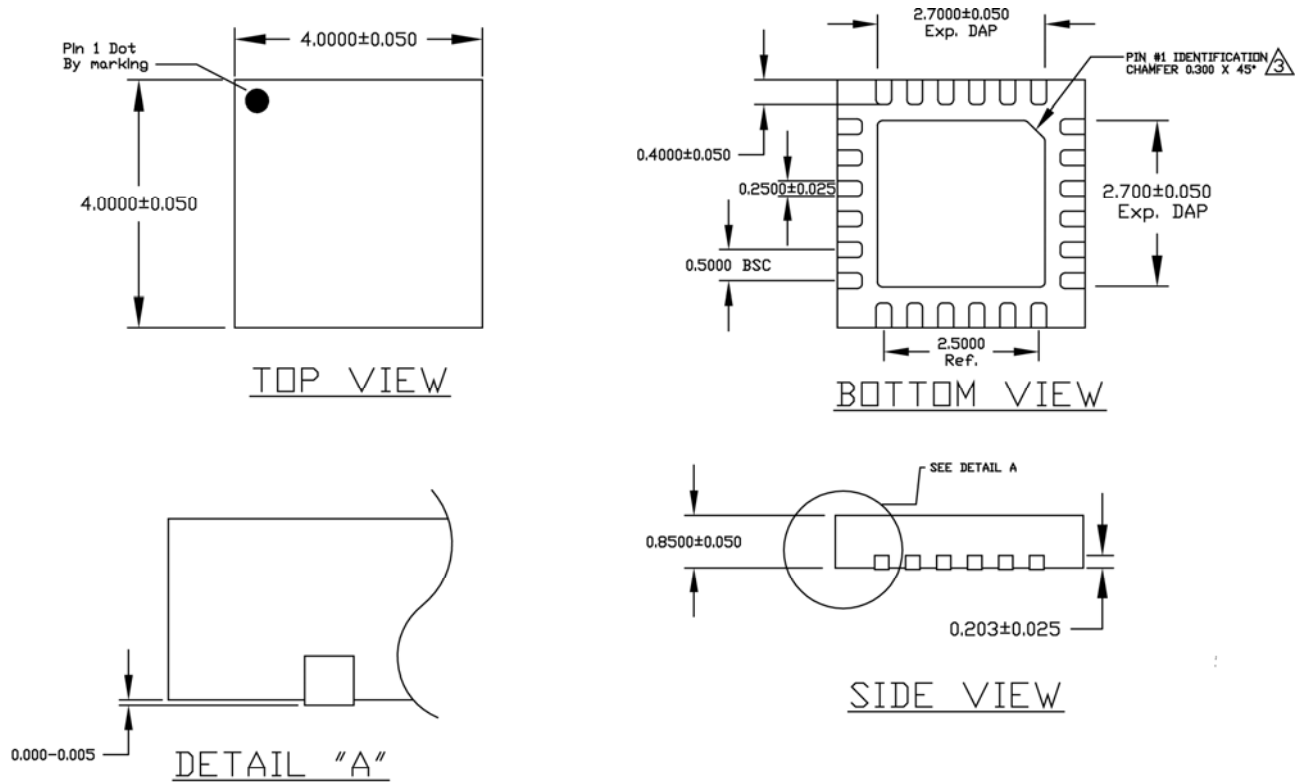


Figure 5. Crystal Input Interface

Package Information



NOTE:

1. ALL DIMENSIONS ARE IN MILLIMETERS (mm).
2. THE PIN#1 IDENTIFIER MUST EXIST ON THE TOP SURFACE OF PACKAGE BY USING IDENTIFICATION MARK OR OTHER FEATURE OF PACKAGE BODY.

CHAMFER STYLE PIN 1 IDENTIFIER ON BOTTOM SIDE

24-Pin Package Type

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