

IRFS4115-7PPbF

HEXFET® Power MOSFET

Applications

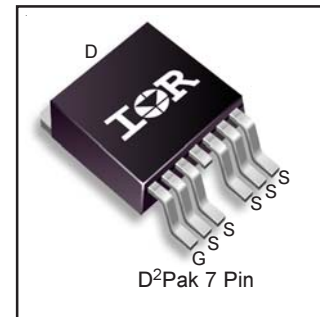
- High Efficiency Synchronous Rectification in SMPS
- Uninterruptible Power Supply
- High Speed Power Switching
- Hard Switched and High Frequency Circuits

Benefits

- Improved Gate, Avalanche and Dynamic dV/dt Ruggedness
- Fully Characterized Capacitance and Avalanche SOA
- Enhanced body diode dV/dt and dI/dt Capability
- Lead-Free



| | |
|--------------------------|---------------|
| V_{DSS} | 150V |
| $R_{DS(on)}$ typ. | 10.0mΩ |
| | max |
| I_D | 105A |



| | | |
|----------|----------|----------|
| G | D | S |
| Gate | Drain | Source |

Absolute Maximum Ratings

| Symbol | Parameter | Max. | Units |
|-----------------------------------|--|------------------|-------|
| I_D @ $T_C = 25^\circ\text{C}$ | Continuous Drain Current, V_{GS} @ 10V | 105 | A |
| I_D @ $T_C = 100^\circ\text{C}$ | Continuous Drain Current, V_{GS} @ 10V | 74 | |
| I_{DM} | Pulsed Drain Current ① | 420 | |
| P_D @ $T_C = 25^\circ\text{C}$ | Maximum Power Dissipation | 380 | W |
| | Linear Derating Factor | 2.5 | W/°C |
| V_{GS} | Gate-to-Source Voltage | ± 20 | V |
| dv/dt | Peak Diode Recovery ③ | 32 | V/ns |
| T_J | Operating Junction and | -55 to + 175 | °C |
| T_{STG} | Storage Temperature Range | | |
| | Soldering Temperature, for 10 seconds (1.6mm from case) | 300 | |
| | Mounting torque, 6-32 or M3 screw | 10lb·in (1.1N·m) | |

Avalanche Characteristics

| | | | |
|------------------------------|---------------------------------|----------------------------|----|
| E_{AS} (Thermally limited) | Single Pulse Avalanche Energy ② | 230 | mJ |
| I_{AR} | Avalanche Current ① | See Fig. 14, 15, 22a, 22b, | A |
| E_{AR} | Repetitive Avalanche Energy ④ | | mJ |

Thermal Resistance

| Symbol | Parameter | Typ. | Max. | Units |
|-----------------|------------------------------------|------|------|-------|
| $R_{\theta JC}$ | Junction-to-Case ⑧⑨ | — | 0.40 | °C/W |
| $R_{\theta JA}$ | Junction-to-Ambient (PCB Mount) ⑦⑧ | — | 40 | |

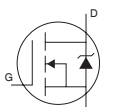
Static @ T_J = 25°C (unless otherwise specified)

| Symbol | Parameter | Min. | Typ. | Max. | Units | Conditions |
|--|--------------------------------------|------|------|------|-------|--|
| V _{(BR)DSS} | Drain-to-Source Breakdown Voltage | 150 | — | — | V | V _{GS} = 0V, I _D = 250μA |
| ΔV _{(BR)DSS} /ΔT _J | Breakdown Voltage Temp. Coefficient | — | 0.18 | — | V/°C | Reference to 25°C, I _D = 3.5mA ^① |
| R _{DS(on)} | Static Drain-to-Source On-Resistance | — | 10. | 11.8 | mΩ | V _{GS} = 10V, I _D = 63A ^④ |
| V _{GS(th)} | Gate Threshold Voltage | 3.0 | — | 5.0 | V | V _{DS} = V _{GS} , I _D = 250μA |
| I _{DSS} | Drain-to-Source Leakage Current | — | — | 20 | μA | V _{DS} = 150V, V _{GS} = 0V |
| | | — | — | 250 | | V _{DS} = 150V, V _{GS} = 0V, T _J = 125°C |
| I _{GSS} | Gate-to-Source Forward Leakage | — | — | 100 | nA | V _{GS} = 20V |
| | Gate-to-Source Reverse Leakage | — | — | -100 | | V _{GS} = -20V |
| R _{G(int)} | Internal Gate Resistance | — | 2.1 | — | Ω | |

Dynamic @ T_J = 25°C (unless otherwise specified)

| Symbol | Parameter | Min. | Typ. | Max. | Units | Conditions |
|----------------------------|---|------|------|------|-------|---|
| gfs | Forward Transconductance | 93 | — | — | S | V _{DS} = 50V, I _D = 62A |
| Q _g | Total Gate Charge | — | 73 | 110 | nC | I _D = 63A |
| Q _{gs} | Gate-to-Source Charge | — | 28 | — | | V _{DS} = 75V |
| Q _{gd} | Gate-to-Drain ("Miller") Charge | — | 28 | — | | V _{GS} = 10V ^④ |
| Q _{sync} | Total Gate Charge Sync. (Q _g - Q _{gd}) | — | 45 | — | | I _D = 63A, V _{DS} = 0V, V _{GS} = 10V |
| t _{d(on)} | Turn-On Delay Time | — | 18 | — | ns | V _{DD} = 98V |
| t _r | Rise Time | — | 50 | — | | I _D = 63A |
| t _{d(off)} | Turn-Off Delay Time | — | 37 | — | | R _G = 2.1Ω |
| t _f | Fall Time | — | 23 | — | | V _{GS} = 10V ^④ |
| C _{iss} | Input Capacitance | — | 5320 | — | | V _{GS} = 0V |
| C _{oss} | Output Capacitance | — | 490 | — | | V _{DS} = 50V |
| C _{rss} | Reverse Transfer Capacitance | — | 110 | — | pF | f = 1.0MHz |
| C _{oss eff. (ER)} | Effective Output Capacitance (Energy Related) ^⑥ | — | 450 | — | | V _{GS} = 0V, V _{DS} = 0V to 120V ^⑥ |
| C _{oss eff. (TR)} | Effective Output Capacitance (Time Related) ^⑤ | — | 520 | — | | V _{GS} = 0V, V _{DS} = 0V to 120V ^⑤ |

Diode Characteristics

| Symbol | Parameter | Min. | Typ. | Max. | Units | Conditions |
|------------------|--|--|------|------|-------|--|
| I _S | Continuous Source Current (Body Diode) | — | — | 104 | A | MOSFET symbol showing the integral reverse p-n junction diode.  |
| I _{SM} | Pulsed Source Current (Body Diode) ^① | — | — | 420 | | |
| V _{SD} | Diode Forward Voltage | — | — | 1.3 | V | T _J = 25°C, I _S = 63A, V _{GS} = 0V ^④ |
| t _{rr} | Reverse Recovery Time | — | 82 | — | ns | T _J = 25°C V _R = 130V, T _J = 125°C I _F = 63A |
| Q _{rr} | Reverse Recovery Charge | — | 271 | — | nC | T _J = 25°C T _J = 125°C |
| I _{RRM} | Reverse Recovery Current | — | 6.0 | — | A | T _J = 25°C |
| t _{on} | Forward Turn-On Time | Intrinsic turn-on time is negligible (turn-on is dominated by LS+LD) | | | | |

Notes:

- ① Repetitive rating; pulse width limited by max. junction temperature.
- ② Limited by T_{Jmax}, starting T_J = 25°C, L = 0.115mH
R_G = 25Ω, I_{AS} = 63A, V_{GS} = 10V. Part not recommended for use above this value.
- ③ I_{SD} ≤ 63A, di/dt ≤ 2510A/μs, V_{DD} ≤ V_{(BR)DSS}, T_J ≤ 175°C.
- ④ Pulse width ≤ 400μs; duty cycle ≤ 2%.
- ⑤ C_{oss eff. (TR)} is a fixed capacitance that gives the same charging time as C_{oss} while V_{DS} is rising from 0 to 80% V_{DSS}.
- ⑥ C_{oss eff. (ER)} is a fixed capacitance that gives the same energy as C_{oss} while V_{DS} is rising from 0 to 80% V_{DSS}.
- ⑦ When mounted on 1" square PCB (FR-4 or G-10 Material). For recommended footprint and soldering techniques refer to application note #AN-994.
- ⑧ R_θ is measured at T_J approximately 90°C.
- ⑨ R_{θJC} value shown is at time zero.

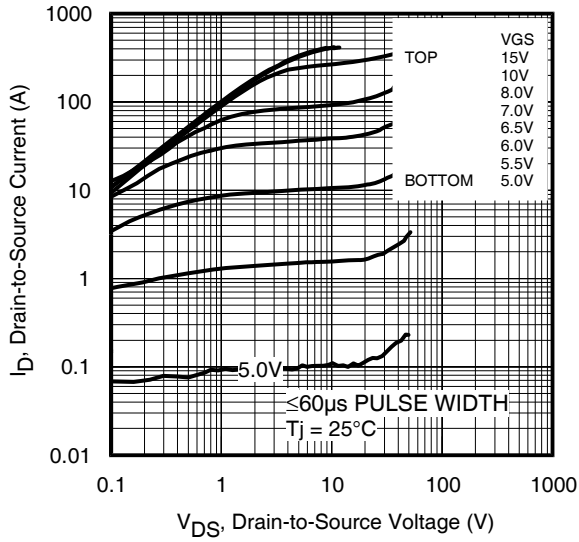


Fig 1. Typical Output Characteristics

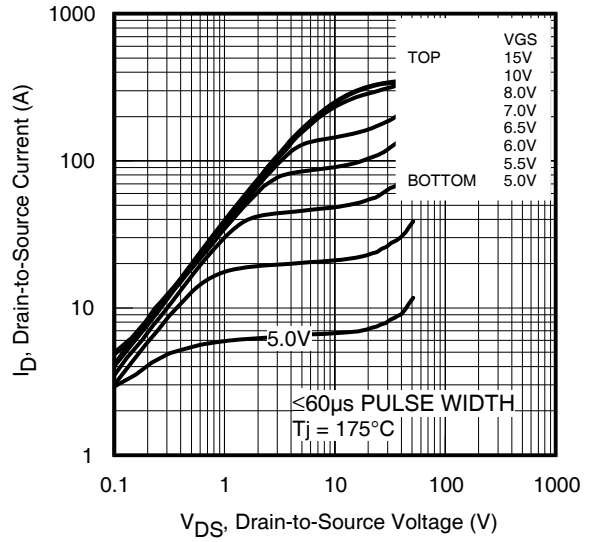


Fig 2. Typical Output Characteristics

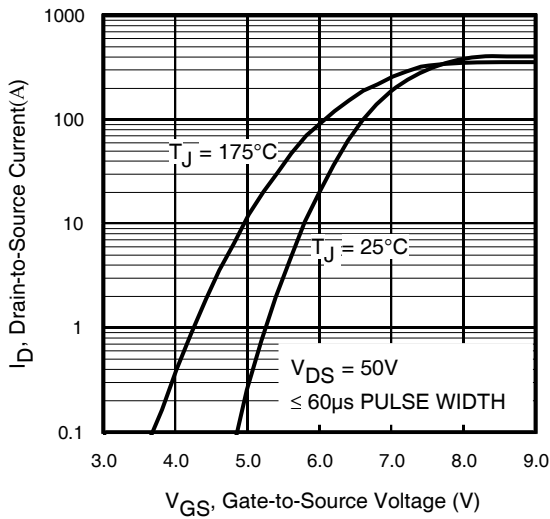


Fig 3. Typical Transfer Characteristics

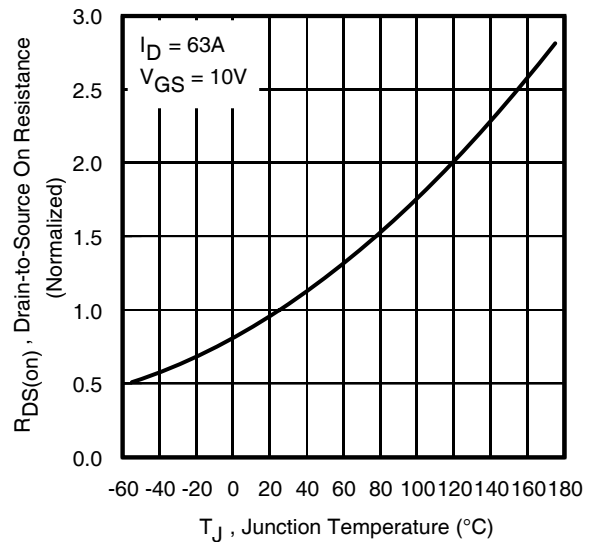


Fig 4. Normalized On-Resistance vs. Temperature

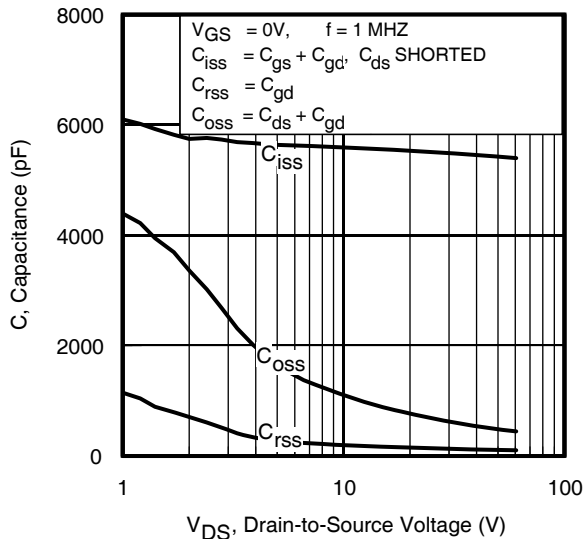


Fig 5. Typical Capacitance vs. Drain-to-Source Voltage

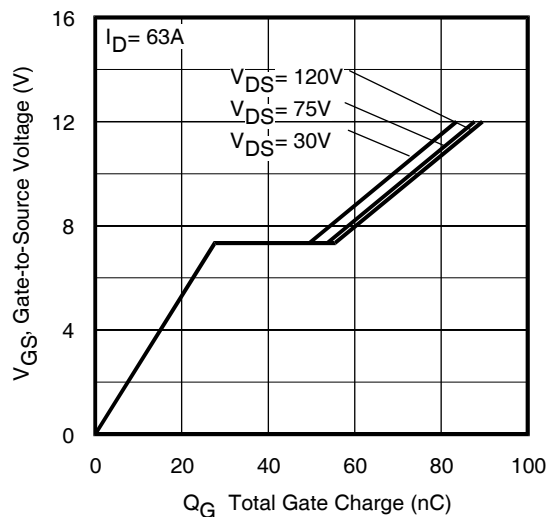


Fig 6. Typical Gate Charge vs. Gate-to-Source Voltage

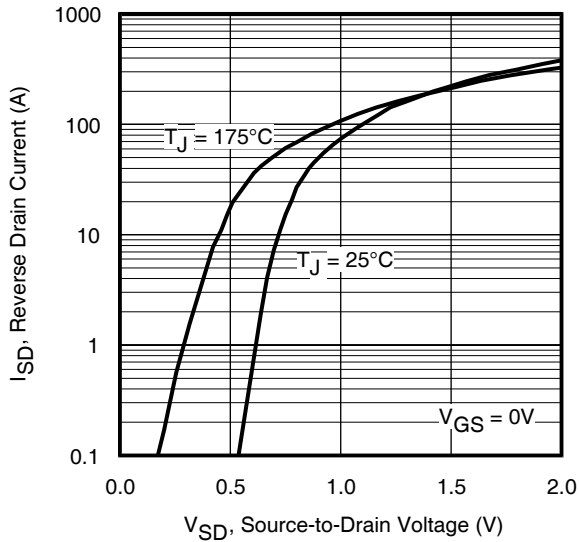


Fig 7. Typical Source-Drain Diode Forward Voltage

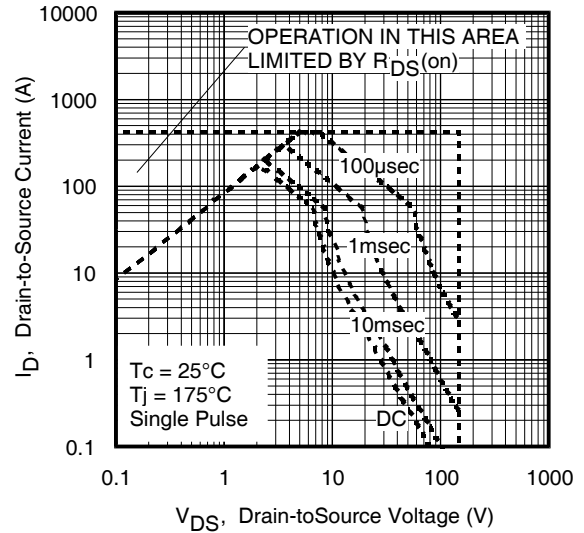


Fig 8. Maximum Safe Operating Area

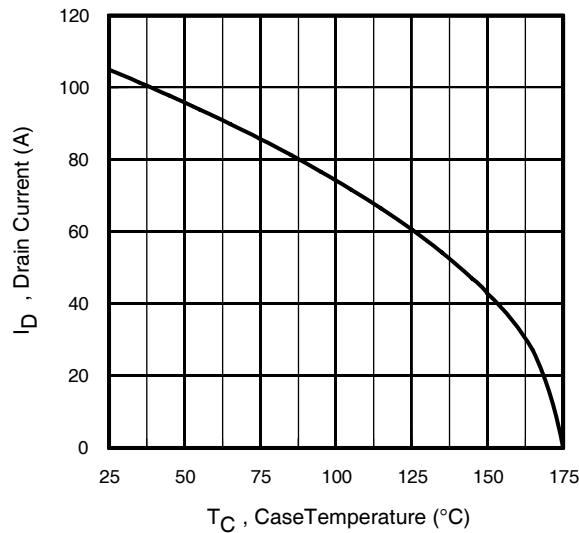


Fig 9. Maximum Drain Current vs. Case Temperature

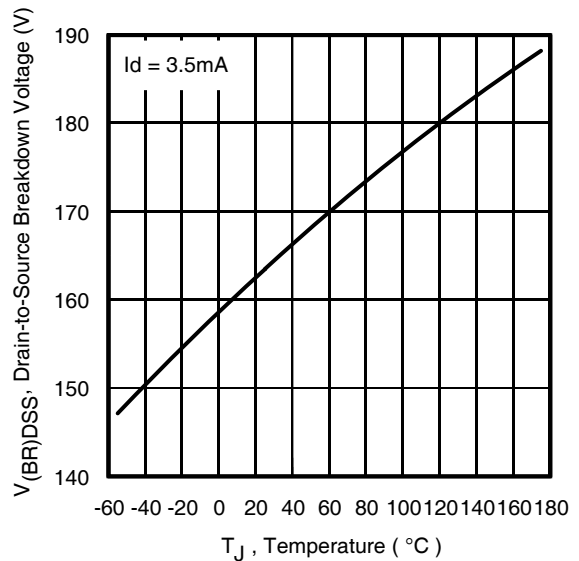


Fig 10. Drain-to-Source Breakdown Voltage

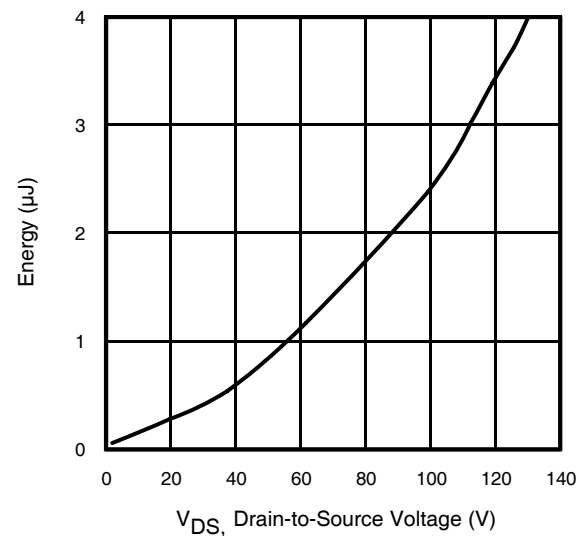


Fig 11. Typical C_{OSS} Stored Energy

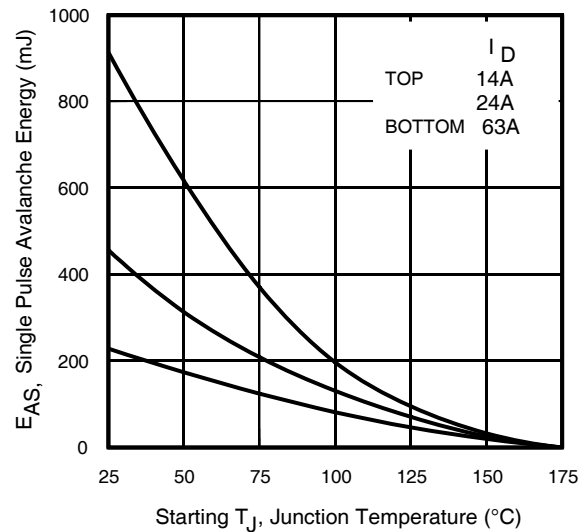


Fig 12. Maximum Avalanche Energy Vs. Drain Current

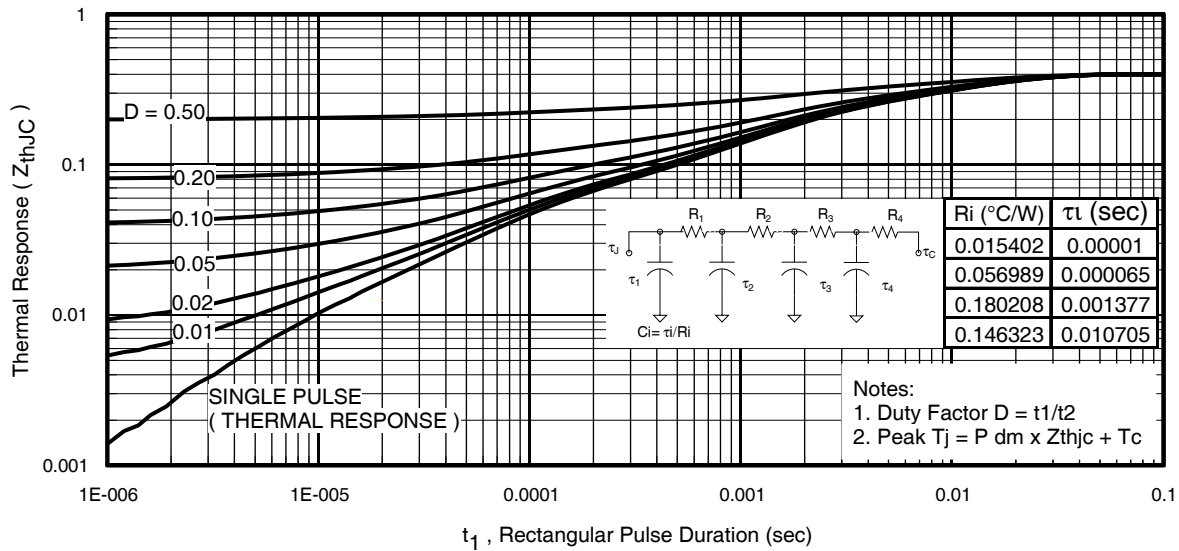


Fig 13. Maximum Effective Transient Thermal Impedance, Junction-to-Case

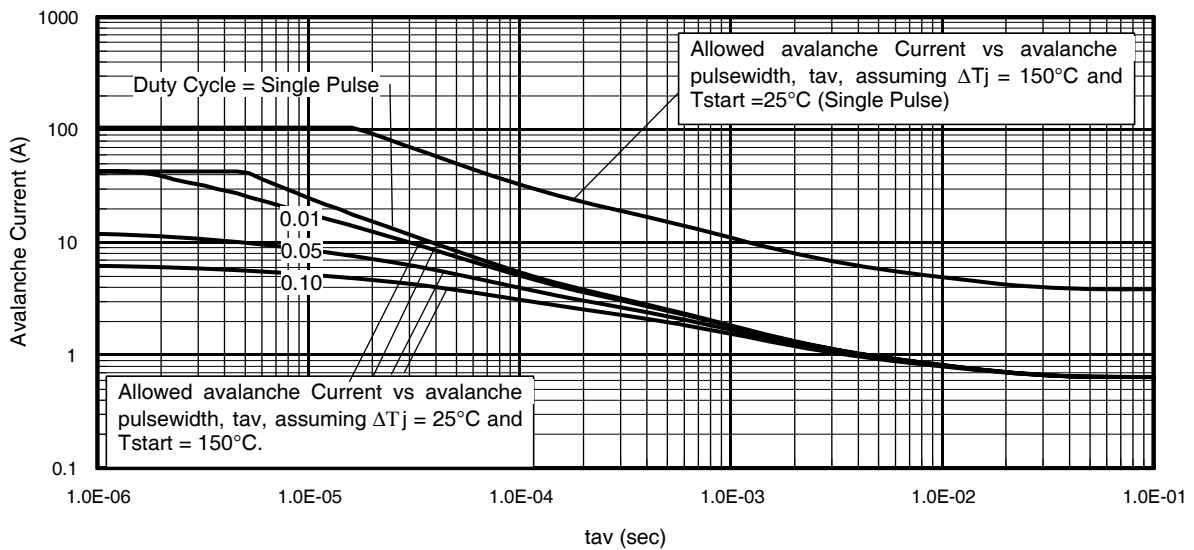
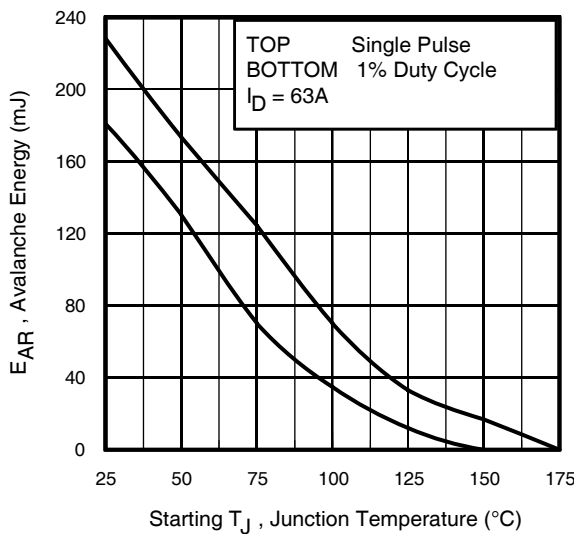


Fig 14. Typical Avalanche Current vs. Pulsewidth



Notes on Repetitive Avalanche Curves, Figures 14, 15:
(For further info, see AN-1005 at www.irf.com)

- Avalanche failures assumption: Purely a thermal phenomenon and failure occurs at a temperature far in excess of T_{jmax} . This is validated for every part type.
- Safe operation in Avalanche is allowed as long as T_{jmax} is not exceeded.
- Equation below based on circuit and waveforms shown in Figures 22a, 22b.
- $P_{D(ave)}$ = Average power dissipation per single avalanche pulse.
- BV = Rated breakdown voltage (1.3 factor accounts for voltage increase during avalanche).
- I_{av} = Allowable avalanche current.
- ΔT = Allowable rise in junction temperature, not to exceed T_{jmax} (assumed as 25°C in Figure 14, 15).
 t_{av} = Average time in avalanche.
 D = Duty cycle in avalanche = $t_{av} \cdot f$
 $Z_{thJC}(D, t_{av})$ = Transient thermal resistance, see Figures 13)

$$P_{D(ave)} = 1/2 (1.3 \cdot BV \cdot I_{av}) = \Delta T / Z_{thJC}$$

$$I_{av} = 2\Delta T / [1.3 \cdot BV \cdot Z_{th}]$$

$$E_{AS(AR)} = P_{D(ave)} \cdot t_{av}$$

Fig 15. Maximum Avalanche Energy vs. Temperature

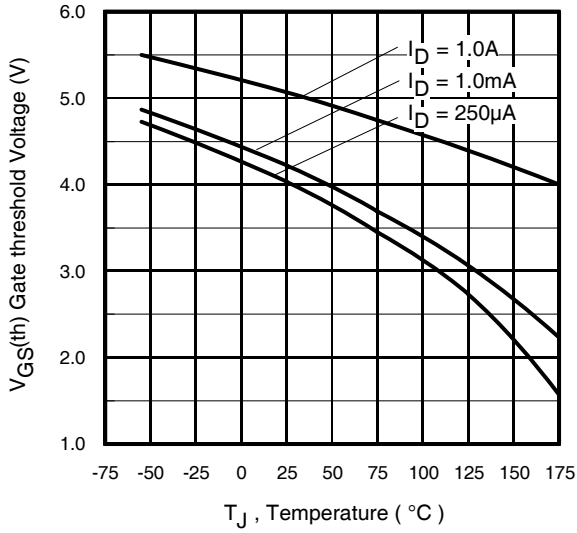


Fig 16. Threshold Voltage Vs. Temperature

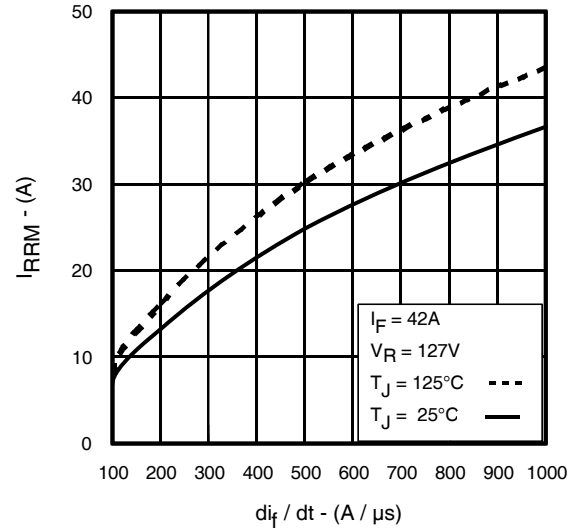


Fig. 17 - Typical Recovery Current vs. di_f/dt

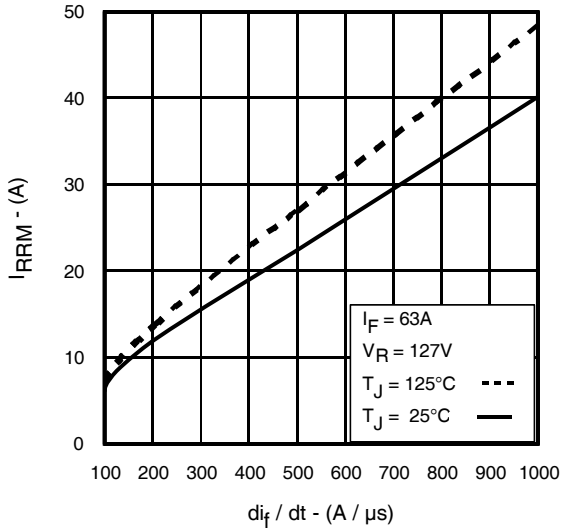


Fig. 18 - Typical Recovery Current vs. di_f/dt

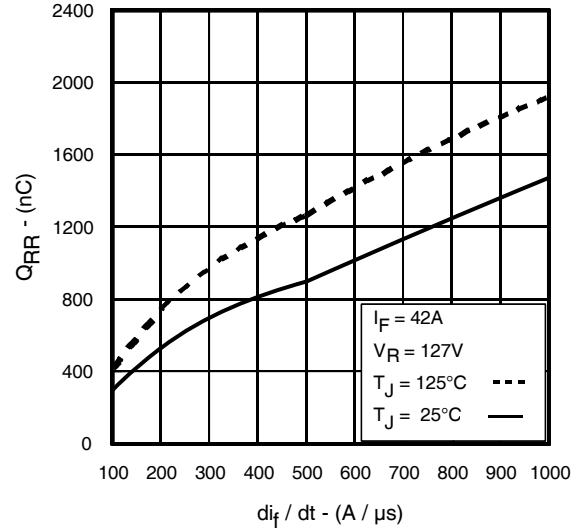


Fig. 19 - Typical Stored Charge vs. di_f/dt

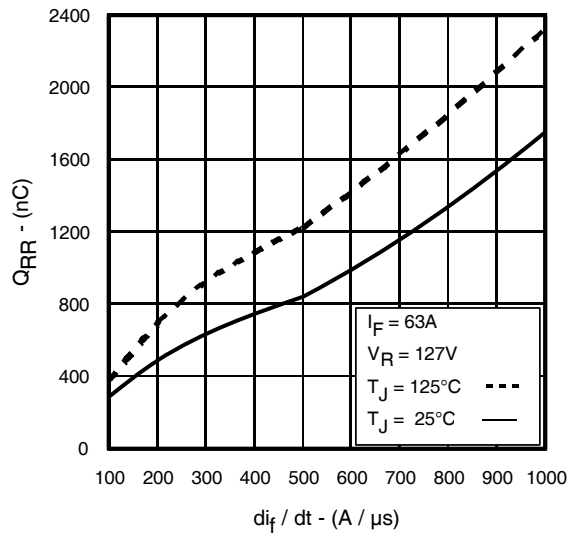


Fig. 20 - Typical Stored Charge vs. di_f/dt



Fig 21. Peak Diode Recovery dv/dt Test Circuit for N-Channel HEXFET® Power MOSFETs



* $V_{GS} = 5V$ for Logic Level Devices

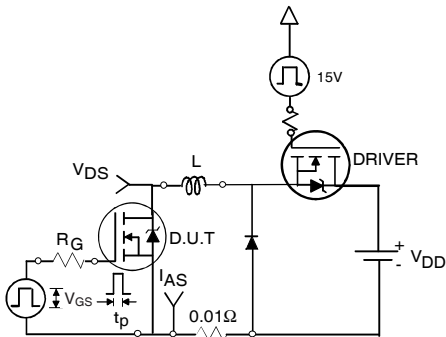


Fig 22a. Unclamped Inductive Test Circuit



Fig 22b. Unclamped Inductive Waveforms

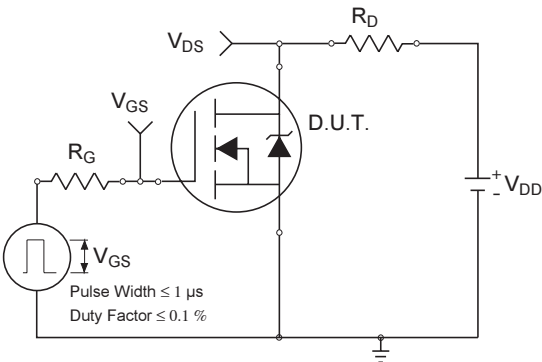


Fig 23a. Switching Time Test Circuit



Fig 23b. Switching Time Waveforms



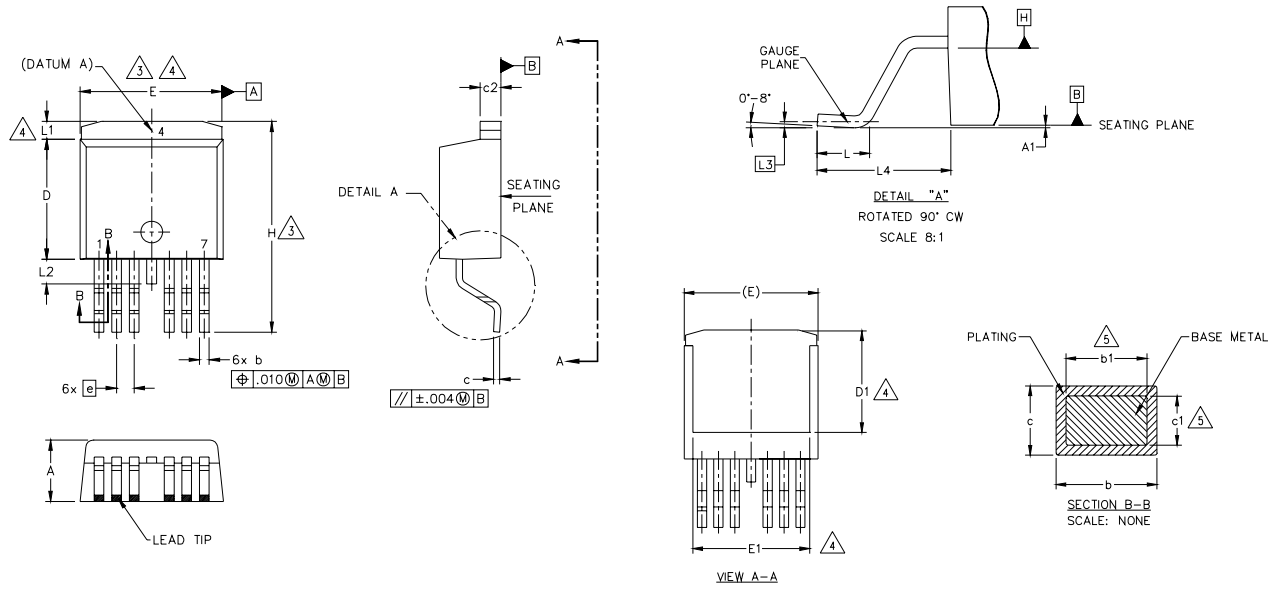
Fig 24a. Gate Charge Test Circuit



Fig 24b. Gate Charge Waveform

D²Pak - 7 Pin Package Outline

Dimensions are shown in millimeters (inches)



| SYMBOL | DIMENSIONS | | | | NOTES | |
|--------|-------------|-------|----------|------|-------|-----|
| | MILLIMETERS | | INCHES | | | |
| | MIN. | MAX. | MIN. | MAX. | | |
| A | 4.06 | 4.83 | .160 | .190 | 5 | |
| A1 | — | 0.254 | — | .010 | | |
| b | 0.51 | 0.99 | .020 | .036 | | |
| b1 | 0.51 | 0.89 | .020 | .032 | | |
| c | 0.38 | 0.74 | .015 | .029 | | |
| c1 | 0.38 | 0.58 | .015 | .023 | | |
| c2 | 1.14 | 1.65 | .045 | .065 | | |
| D | 8.38 | 9.65 | .330 | .380 | | 3 |
| D1 | 6.86 | — | .270 | — | | 4 |
| E | 9.65 | 10.67 | .380 | .420 | | 3,4 |
| E1 | 6.22 | — | .245 | — | 4 | |
| e | 1.27 BSC | | .050 BSC | | 4 | |
| H | 14.61 | 15.88 | .575 | .625 | | |
| L | 1.78 | 2.79 | .070 | .110 | | |
| L1 | — | 1.68 | — | .066 | | |
| L2 | — | 1.78 | — | .070 | | |
| L3 | 0.25 BSC | | .010 BSC | | | |
| L4 | 4.78 | 5.28 | .188 | .208 | | |

NOTES:

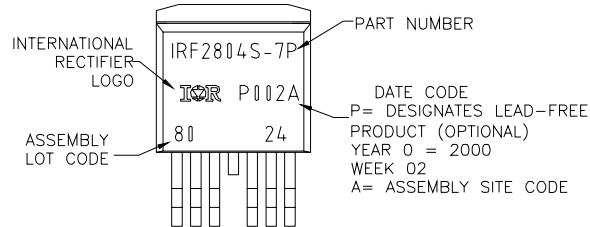
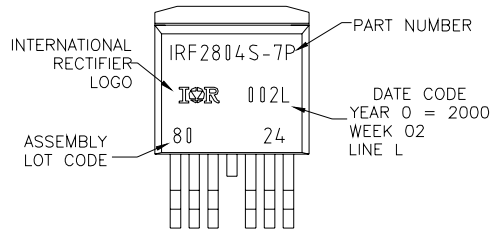
1. DIMENSIONING AND TOLERANCING AS PER ASME Y14.5M-1994
2. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
3. DIMENSION D & E DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.127 [.005"] PER SIDE. THESE DIMENSIONS ARE MEASURED AT THE OUTMOST EXTREMES OF THE PLASTIC BODY AT DATUM H.
4. THERMAL PAD CONTOUR OPTIONAL WITHIN DIMENSION E, L1, D1 & E1.
5. DIMENSION b1 AND c1 APPLY TO BASE METAL ONLY.
6. DATUM A & B TO BE DETERMINED AT DATUM PLANE H.
7. CONTROLLING DIMENSION: INCH.
8. OUTLINE CONFORMS TO JEDEC OUTLINE TO-263CB.

Note: For the most current drawing please refer to IR website at <http://www.irf.com/package/>

D²Pak - 7 Pin Part Marking Information

EXAMPLE: THIS IS AN IRF2804S-7P WITH
 LOT CODE 8024
 ASSEMBLED ON WW02,2000
 IN THE ASSEMBLY LINE "L"

Note: "P" in assembly line
 position indicates "Lead Free"

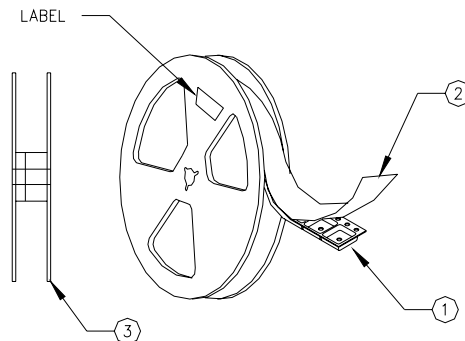
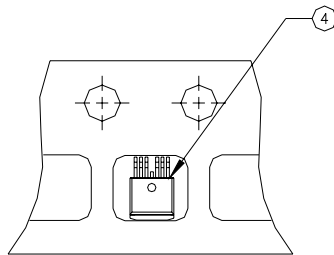


D²Pak - 7 Pin Tape and Reel

NOTES, TAPE & REEL, LABELLING:

1. TAPE AND REEL.
 - 1.1 REEL SIZE 13 INCH DIAMETER.
 - 1.2 EACH REEL CONTAINING 800 DEVICES.
 - 1.3 THERE SHALL BE A MINIMUM OF 42 SEALED POCKETS CONTAINED IN THE LEADER AND A MINIMUM OF 15 SEALED POCKETS IN THE TRAILER.
 - 1.4 PEEL STRENGTH MUST CONFORM TO THE SPEC. NO. 71-9667.
 - 1.5 PART ORIENTATION SHALL BE AS SHOWN BELOW.
 - 1.6 REEL MAY CONTAIN A MAXIMUM OF TWO UNIQUE LOT CODE/DATE CODE COMBINATIONS. REWORKED REELS MAY CONTAIN A MAXIMUM OF THREE UNIQUE LOT CODE/DATE CODE COMBINATIONS. HOWEVER, THE LOT CODES AND DATE CODES WITH THEIR RESPECTIVE QUANTITIES SHALL APPEAR ON THE BAR CODE LABEL FOR THE AFFECTED REEL.

2. LABELLING (REEL AND SHIPPING BAG).
 - 2.1 CUST. PART NUMBER (BAR CODE): IRFXXXXSTR-L-7P
 - 2.2 CUST. PART NUMBER (TEXT CODE): IRFXXXXSTR-L-7P
 - 2.3 I.R. PART NUMBER: IRFXXXXSTR-L-7P
 - 2.4 QUANTITY:
 - 2.5 VENDOR CODE: IR
 - 2.6 LOT CODE:
 - 2.7 DATE CODE:



Note: For the most current drawing please refer to IR website at: <http://www.irf.com/package/>

Data and specifications subject to change without notice.
 This product has been designed and qualified for the Industrial market.
 Qualification Standards can be found on IR's Web site.

International
IR Rectifier

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 TAC Fax: (310) 252-7903

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