ANALOG DEVICES

Evaluation Board for True Differential, Dual, Simultaneous Sampling, 12-/14-Bit ADC with PGA

EVAL-AD7262/AD7264

FEATURES

Full-featured evaluation board for the AD7262 and AD7264
EVAL-CED1Z compatible
Standalone capability
On-board analog buffering and voltage reference
Various linking options
PC software for control and data analysis when used with
EVAL-CED1Z

PART DESCRIPTION

This data sheet describes the evaluation board for the AD7262 and the AD7264, which are dual, 12-bit/14-bit, high speed, low power, successive approximation analog-to-digital (ADCs). The parts operate from a single 5 V power supply and feature throughput rates up to 1 MSPS per on-chip ADC. Two complete ADC functions allow simultaneous sampling and conversion of two channels. Both devices contains two ADCs, each preceded by a true differential analog input with a PGA. There are fourteen gain settings available, ×1, ×2, ×3, ×4, ×6, ×8, ×12, ×16, ×24, ×32, ×48, ×64, ×96, and ×128. In addition, the AD7264 and AD7262 contain four comparators. Full details on the AD7262 and AD7264 are available in the AD7262 and AD7264 data sheets available from Analog Devices, Inc., which should be consulted in conjunction with this data sheet when using the evaluation board.

GENERAL DESCRIPTION

On-board components include: an AD780, a pin-programmable 2.5 V or 3 V ultrahigh, precision, band gap reference, and two SN74LVC1G125 digital buffers.

Various link options are explained in the Evaluation Board Hardware section. Interfacing to this board is done through a 96-way connector. This 96-way connector is compatible with the EVAL-CED1Z also available from Analog Devices. External sockets are provided for multiple signals.

FUNCTIONAL BLOCK DIAGRAM

Figure 1.

EVAL-AD7262/AD7264

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REVISION HISTORY

12/08—Revision 0: Initial Version

EVALUATION BOARD HARDWARE

POWER SUPPLIES

When using this evaluation board with the EVAL-CED1Z, all supplies are provided from the EVAL-CED1Z through the 96-way connector. When using the board as a standalone unit, external supplies must be provided. This evaluation board has the following power supply inputs: +12 V, AV_{CC} (+5 V), AGND, V_{DRIVE}, and DGND. The (+12 V) supply is only required if the external AD780 voltage reference is to be used, however if the AD7262 or AD7264 is used with an internal reference then the ±12 V supplies are not required.

The supplies are decoupled to the relevant ground plane with 10 μF tantalum and 0.1 μF multilayer ceramic capacitors at the point where they enter the board. The supply pins for the external reference are also decoupled to AGND with a 10 μF tantalum and a 0.1 μF ceramic capacitor. The AV_{CC}, $C_A\_C_BV_{CC}$ and $C_C\_C_DV_{CC}$ supply pins are decoupled to AGND with a 0.1 μF multilayer ceramic capacitors per supply pin and one 10 μF tantalum capacitor for all the previously mentioned supply pins.

Extensive ground planes are used on this board to minimize the effect of high frequency noise interference. There are two ground planes, AGND and DGND. These are connected at one location close to the AD7262 or AD7264.

LINK OPTIONS

There are 14 link options and 5 solder links that must be set correctly to select the appropriate operating setup before using the evaluation board. The functions of these options are outlined in Table 1.

The evaluation board also contains two resistor links which enable the user to access the digital output from the part via the SMB connectors. In normal operation with the EVAL-CED1Z board these resistors are not inserted and the output from the AD7262 or AD7264 is fed directly to the EVAL-CED1Z board for processing.

Table 1. Link Option Functions

Link No.	Function
LK1, LK2	These links select the source of the reference input voltage applied to the $V_{REF}A$ and $V_{REF}B$ pins of the AD7262 and AD7264.
	In Position A, the reference input must be supplied through the $V_{REF}A$ and $V_{REF}B$ SMB connectors if the internal reference on the AD7264 and AD7262 is not used.
	In Position B, the AD780 supplies a 2.5 V reference to the AD7262 or AD7264.
LK3	This link selects whether the AD7262 or AD7264 uses the internal or external reference by setting the logic state of the REFSEL pin.
	In Position A, the on-chip 2.5 V internal reference is used as the reference source for both ADC A and ADC B. In this case, LK1 and LK2 can be left unconnected.
	In Position B, an external reference can be supplied to the AD7262 or AD7264 through the $V_{REF}A$ or $V_{REF}B$ pins. In this case, LK1 and LK2 must be in Position A or Position B.
LK4	This link option selects the source of the V_{DRIVE} supply for the AD7262 or AD7264 digital interface.
	In Position A, a 3.3 V V_{DRIVE} input is supplied to the AD7264 or AD7262 from the EVAL-CED1Z board.
	In Position B, the V_{DRIVE} input on the AD7264 or AD7262 is tied to the AV_{CC} supply.
	In Position C, V_{DRIVE} must be supplied from an external source via the J5-1 SMB.
LK5	This link option selects the source of the AV_{CC} supply for the AD7262 or AD7264.
	In Position A, AV_{CC} is supplied from the EVAL-CED1Z board.
	In Position B, AV_{CC} must be supplied from an external source via the J6-1 SMB connector.
LK6	This link option selects the source of the logic input to the CAL pin, thus selecting the gain of the AD7262 or AD7264.
	In Position A, the CAL pin is connected to the V_{DRIVE} supply, that is, it is tied to a logic high state.
	In Position B, the CAL pin is supplied by the EVAL-CED1Z board.
	In Position C, the CAL pin is connected to DGND, that is, it is tied to a logic low state.
LK7	This link option selects the source of the logic input to the PD0/D_{IN} pin, thus selecting the power-down configuration for the AD7262 or AD7264.
	In Position A, the PD0/D_{IN} pin is connected to the V_{DRIVE} supply. That is, it is tied to a logic high state.
	In Position B, the PD0/D_{IN} pin is supplied by the EVAL-CED1Z board.
	In Position C, the PD0/D_{IN} pin is connected to DGND, that is, it is tied to a logic low state.
	Position D should not be selected.

Link No.	Function
LK8	This link option selects the source of the logic input to the PD1 pin, thus selecting the power-down configuration for the AD7262 or AD7264.
	In Position A, the PD1 pin is connected to the V_{DRIVE} supply, that is, it is tied to a logic high state.
	In Position B, PD1 is supplied by the EVAL-CED1Z board.
	In Position C, the PD1 pin is connected to DGND, that is, it is tied to a logic low state.
LK9	This link option selects the source of the logic input to the PD2 pin, thus selecting the power down configuration for the AD7262 or AD7264.
	In Position A, the PD2 pin is connected to the V_{DRIVE} supply, that is, it is tied to a logic high state.
	In Position B, the PD2 pin is supplied by the EVAL-CED1Z board.
	In Position C, the PD2 pin is connected to DGND, that is, it is tied to a logic low state.
LK10	This link option selects the source of the logic input to the G0 pin, thus selecting the gain of the AD7262 or AD7264.
	In Position A, the G0 pin is connected to the V_{DRIVE} supply, that is, it is tied to a logic high state.
	In Position B, the G0 pin is supplied by the EVAL-CED1Z board.
	In Position C, the G0 pin is connected to DGND, that is, it is tied to a logic low state.
LK11	This link option selects the source of the logic input to the G1 pin, thus selecting the gain of the AD7262 or AD7264.
	In Position A, the G1 pin is connected to the V_{DRIVE} supply, that is, it is tied to a logic high state.
	In Position B, the G1 pin is supplied by the EVAL-CED1Z board.
	In Position C, the G1 pin is connected to DGND, that is, it is tied to a logic low state.
LK12	This link option selects the source of the logic input to the G2 pin, thus selecting the gain of the AD7262 or AD7264
	In Position A, the G2 pin is connected to the V_{DRIVE} supply, that is, it is tied to a logic high state.
	In Position B, the G2 pin is supplied by the EVAL-CED1Z board.
	In Position C, the G2 pin is connected to DGND, that is, it is tied to a logic low state.
LK13	This link option selects the source of the logic input to the G3 pin, thus selecting the gain of the AD7262 or AD7264
	In Position A, the G3 pin is connected to the V_{DRIVE} supply, that is, it is tied to a logic high state.
	In Position B, the G3 pin is supplied by the EVAL-CED1Z board.
	In Position C, the G3 pin is connected to DGND, that is, it is tied to a logic low state.
LK14	This link option is used to select the source of the +12 V supply, which is used to power the external reference.
	In Position A, +12 V is supplied from the EVAL-CED1Z board through the 96-way connector.
	In Position B, +12 V is supplied from an external source via the power connector, J17.
SL1	This link option selects the source of one of the AV_{CC} supplies for the AD7262 or AD7264.
	In Position A, AV_{CC} is tied to the other AV_{CC} supply.
	In Position B, AV_{CC} is supplied from an external source via J5-3 SMB. This option should not be used.
SL2, SL3	These link options select the source of the $C_A\_C_BV_{CC}$ and $C_C\_C_DV_{CC}$ supplies for the AD7262/AD7264.
	In Position A, $C_A\_C_BV_{CC}$ and $C_C\_C_DV_{CC}$ are tied to the AVCC supply.
	In Position B, $C_A\_C_BV_{CC}$ and $C_C\_C_DV_{CC}$ are supplied from an external source via $C_A\_C_BV_{CC}$ and $C_C\_C_DV_{CC}$ SMB.
SL4	This link selects the source of the SCLK signal for the AD7262 or AD7264.
	In Position A, the SCLK signal is taken directly from the EVAL-CED1Z board through the 96-way connector.
	In Position B, the SCLK signal must be supplied from an external source via the SCK SMB.
SL5	This link in conjunction selects the source of the $\overline{CS}$ input to the ADC.
	In Position A, $\overline{CS}$ is supplied by the EVAL-CED1Z board.
	In Position B, $\overline{CS}$ is supplied from an external source via the CS SMB.
R12, R13	These resistors must be inserted if the $D_{OUT}A$ and $D_{OUT}B$ signal as to be fed to the DOUT-A, DOUT-B SMB.

SETUP CONDITIONS

Care should be taken before applying power and signals to the evaluation board to ensure that all link positions are as per the required operating mode. There are two different modes in which to operate the evaluation board. Either the user can operate the board with the EVAL-CED1Z or it can be used as a standalone board. The board can accept differential analog input voltages.

Table 2 and Table 3 shows the position in which all the links are set when the evaluation board is packaged. When the board is shipped, it is assumed that the user is operating with the EVAL-CED1Z board. The links are set so that all power supplies and control signals are supplied by the EVAL-CED1Z. The board is configured to enable the user to supply a differential input signal directly to the device for both ADCs. Each ADC on the AD7262 or AD7264 is preceded by an internal PGA, which implies that no external buffers are required on the analog input. Accordingly, it is recommended that the AD7262 or AD7264 analog inputs be driven directly with a differential signal.

The EVAL-AD7262/AD7264 is configured to use an external reference with differential analog inputs directly from the user's source.

Table 2. Link Positions on the Packaged EVAL-AD7262/AD7264

Link No.	Position	Function
LK1	B	The AD780 supplies an external reference to the AD7262 or AD7264 through $V_{REF}A$.
Lk2	B	The AD780 supplies an external reference to the AD7262 or AD7264 through $V_{REF}B$.
LK3	B	REFSEL is tied to ground (low logic state). Thus, an external reference is selected.
LK4	A	The V_{DRIVE} supply is supplied from the EVAL-CED1Z. The EVAL-CED1Z can supply this pin with 3.3 V only.
LK5	A	The AV_{CC} supply for the AD7262 or AD7264 is supplied by the EVAL-CED1Z board.
LK6	B	The logic input to the CAL pin of the AD7262 or AD7264 is supplied from the EVAL-CED1Z.
LK7	B	The logic input to the PD0/D_{IN} pin of the AD7262 or AD7264 is supplied from the EVAL-CED1Z.
LK8	B	The logic input to the PD1 pin of the AD7262 or AD7264 is supplied from the EVAL-CED1Z.
LK9	B	The logic input to the PD2 pin of the AD7262 or AD7264 is supplied from the EVAL-CED1Z.
LK10	B	The logic input to the G0 pin of the AD7262 or AD7264 is supplied from the EVAL-CED1Z.
Lk11	B	The logic input to the G1 pin of the AD7262 or AD7264 is supplied from the EVAL-CED1Z.
LK12	B	The logic input to the G2 pin of the AD7262 or AD7264 is supplied from the EVAL-CED1Z.
LK13	B	The logic input to the G3 pin of the AD7262 or AD7264 is supplied from the EVAL-CED1Z.
LK14	A	+12 V is supplied from the EVAL- CED1Z board.

Table 3. Solder Link Positions on the Packaged EVAL-AD7262/AD7264

Link No.	Position	Function
SL1	A	The AV_{CC} supply for the AD7262 or AD7264 is ties to the other AV_{CC} supply and thus is supplied by the EVAL-CED1Z.
SL2	A	The $C_A\_C_BV_{CC}$ and $C_C\_C_DV_{CC}$ are tied to the AV_{CC} supply and thus are supplied by the EVAL-CED1Z.
SL3	A	The $C_A\_C_BV_{CC}$ and $C_C\_C_DV_{CC}$ are tied to the AV_{CC} supply and thus are supplied by the EVAL-CED1Z.
SL4	A	The SCLK signal is supplied directly from the EVAL-CED1Z board through the 96-way connector.
SL5	A	The $\overline{CS}$ signal is supplied directly from the EVAL-CED1Z board through the 96-way connector.
R12, R13		Do not insert.

INTERFACING THE EVALUATION BOARD TO THE EVAL-CED1Z

Interfacing the EVAL-CED1Z board to the evaluation board is via a 96-way connector, J1. The pinout for the J1 connector is shown in Figure 2. Table 5 gives a description of the pins on the 96-way connector used to interface between the EVAL-CED1Z board and the EVAL-AD7262/AD7264. Table 4 gives its pin designations.
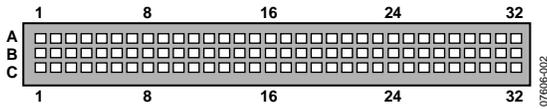

Figure 2. Pin Configuration for the 96-Way Connector, J1

Table 4. 96-Way Connector Pin Functions[1]

Pin	Row A	Row B	Row C
1	DTPRI	GPIO3	DR1PRI
2	TFS1		RFS1
3	TSCLK1		RSCLK1
4	DGND	DGND	DGND
5	DT0PRI		DR0PRI
6	TFS0		RFS0
7	TSCLK0		RSCLK0
8	V_{DRIVE} (+3.3 V)	V_{DRIVE} (+3.3 V)	V_{DRIVE} (+3.3 V)
9			
10			
11	DTOSEC		GPIO6
12	DGND	DGND	DGND
13			DROSEC
14	GPIO5		GPIO7
15	GPIO0		GPIO4
16	DGND	DGND	DGND
17			GPIO2
18			
19		GPIO1	
20	DGND	DGND	DGND
21	AGND	AGND	AGND
22	AGND	AGND	AGND
23	AGND	AGND	AGND
24	AGND	AGND	AGND
25	AGND	AGND	AGND
26	AGND	AGND	AGND
27		AGND	
28		AGND	
29	AGND	AGND	AGND
30	−12 V	AGND	+12 V
31	(−5 V)	(−5 V)	(−5 V)
32	AV_{DD} (+5 V)	AV_{DD} (+5 V)	AV_{DD} (+5 V)

[1] The unused pins of the 96-way connector are not shown.

Table 5. 96-Way Connector Pin Description

Signal	Description
DRPRI	Data Receive Primary. This input is connected to the $D_{OUT}A$ pin of the AD7262 or AD7264.
DRSEC	Data Receive Secondary. This input is connected to the $D_{OUT}B$ pin of the AD7262 or AD7264.
RSCLK	Receive Clock. This continuous clock is connected to the SCLK pin of the AD7262 or AD7264 via SL4.
TFS	Transmit Frame Sync. This output is connected to the $\overline{CS}$ pin of the AD7262 or AD7264 via SL5 to frame the serial data transfer.
RFS	Receive Frame Sync. This input is connected to the TFS pin on the EVAL-CED1Z board to frame the serial data read.
AV_{DD}	Analog +5 V Supply. These lines are connected to the AV_{CC} line on the board via LK5.
V_{DRIVE}	Digital +3.3 V supply. This is used to provide the V_{DRIVE} supply to the board via LK4 for the digital logic.
−5 V	Analog −5 V Supply. This supply is not used on the EVAL-AD7262/AD7264.
DGND	Digital Ground. These lines are connected to the digital ground plane on the evaluation board.
AGND	Analog Ground. These lines are connected to the analog ground plane on the evaluation board.
+12 V	+12 V Supply (V_{CC}). This line is connected to the +12 V supply line on the board via LK14.
−12 V	−12 V Supply (V_{SS}). This supply is not used on the EVAL-AD7262/AD7264.
GPIO 0	General-Purpose Input/Output. This input is connected to the G0 pin of the AD7262 or AD7264 via LK10.
GPIO1	General-Purpose Input/Output. This input is connected to the G1 pin of the AD7262 or AD7264 via LK11.
GPIO2	General-Purpose Input Output. This input is connected to the PD0 pin of the AD7262 or AD7264 via LK7.
GPIO3	General-Purpose Input/Output. This input is connected to the PD2 pin of the AD7262 or AD7264 via LK9.
GPIO4	General-Purpose Input/Output. This input is connected to the G3 pin of the AD7262 or AD7264 via LK13.
GPIO5	General-Purpose Input/Output. This input is connected to the CAL pin of the AD7262 or AD7264 via LK6.
GPIO6	General-Purpose Input/Output. This input is connected to the PD1 pin of the AD7262 or AD7264 via LK8.
GPIO7	General-Purpose Input/Output. This input is connected to the G2 pin of the AD7262 or AD7264 via LK12.

SOCKETS

There are 24 SMB input sockets relevant to the operation of the AD7262 or AD7264 on this evaluation board. All of these sockets are used for applying an externally generated signal to the evaluation board. When operating the board with the EVAL-CED1Z, the only external sockets necessary are those used to supply the differential signal to the analog inputs to the ADC and the comparators (that is, VA−, VA+, VB−, VB+, CA+,

CA−, CB+, CB−, CC+, CC−, CD+, and CD−). All of the other sockets are optional and if they are not used, their signals are supplied by the EVAL-CED1Z. Most of these sockets are used when operating the board as a standalone unit, as all the signals required are supplied from external sources. The functions of these sockets are outlined in Table 6.

Table 6. Socket Functions

Socket	Function
VA−	Subminiature BNC socket for a unipolar differential input that is applied directly to the V_A− pin of the AD7262 or AD7264.
VA+	Subminiature BNC socket for a unipolar differential input that is applied directly to the V_A+ pin of the AD7262 or AD7264.
VB−	Subminiature BNC socket for a unipolar differential input that is applied directly to the V_B− pin of the AD7262 or AD7264.
VB+	Subminiature BNC socket for a unipolar differential input that is applied directly to the V_B+ pin of the AD7262 or AD7264.
VREFA	Subminiature BNC socket for an external reference voltage to be applied to $V_{REF}A$ or to access the internal reference from the AD7262 and AD7264.
VREFB	Subminiature BNC socket for an external reference voltage to be applied to $V_{REF}B$ or to access the internal reference from the AD7262 and AD7264.
DOUT-A	Subminiature BNC socket for $D_{OUT}A$ output.
DOUT-B	Subminiature BNC socket for $D_{OUT}B$ output.
CS	Subminiature BNC socket for an external $\overline{CS}$ input.
SCK	Subminiature BNC socket for an external SCLK input.
CA+	Subminiature BNC socket for C_A+ input.
CA−	Subminiature BNC socket for C_A− input.
CB+	Subminiature BNC socket for C_B+ input.
CB−	Subminiature BNC socket for C_B− input.
CC+	Subminiature BNC socket for C_C+ input.
CC−	Subminiature BNC socket for C_C− input.
CD+	Subminiature BNC socket for C_D+ input.
CD−	Subminiature BNC socket for C_D− input.
COUT_A	Subminiature BNC socket for $C_{OUT}A$ output.
COUT_B	Subminiature BNC socket for $C_{OUT}B$ output.
COUT_C	Subminiature BNC socket for $C_{OUT}C$ output.
COUT_D	Subminiature BNC socket for $C_{OUT}D$ output.
CA_CB_VCC	Subminiature BNC socket for an external $C_A\_C_B\_V_{CC}$ input.
CC_CD_VCC	Subminiature BNC socket for an external $C_C\_C_D\_V_{CC}$ input.

CONNECTORS

There are four connectors on the EVAL-AD7262/AD7264 as outlined in Table 7.

Table 7. Connector Functions

Connector	Function
J1	96-way connector for the digital interface and power supply connections.
J5 -1	External V_{DRIVE} power connector.
J5-2	External DGND power connector.
J5-3	External AV_{CC} power connector.
J6-1	External AV_{CC} power connector.
J6-2	External AGND power connector.
J7	External +12 V and AGND power connector.

TEST POINTS

There are numerous test points on the EVAL-AD7262/AD7264. These test points enable the user to have easy access to the signals for probing, evaluation, and debugging.

OPERATING WITH THE EVAL-CED1Z BOARD

The evaluation board can be operated in a standalone mode or operated in conjunction with the EVAL-CED1Z board. This evaluation board controller is available from Analog Devices under the order entry EVAL-CED1Z.

When interfacing the EVAL-AD7262/AD7264 directly to the EVAL-CED1Z board, all supplies and control signals to operate the EVAL-AD7262/AD7264 are provided by the EVAL-CED1Z. The AD7264 can operate at 1 MSPS with SCLK frequencies up to 34 MHz while the AD7262 can operate with a 40 MHz SCLK. The SCLK frequency supplied by the EVAL-CED1Z is fixed at 34 MHz for the AD7264 and 40 MHz for the AD7262. The software allows the user to change the throughput rate by effectively modifying the $\overline{CS}$ high time.

Software to communicate with the EVAL-CED1Z and AD7262 or AD7264 is provided with the EVAL-AD7262/AD7264 package.

The 96-way connector on the EVAL-AD7262/AD7264 plugs directly into the 96-way connector on the EVAL-CED1Z. The EVAL-CED1Z provides all the supplies for the evaluation board. It is powered from a 7 V, 15 W power supply, which accepts input voltages from 100 V to 240 V ac and contains the relevant adaptors for worldwide use. The power supply is provided with the EVAL-CED1Z.

Connection between the EVAL-CED1Z and the USB port of a PC is via a standard USB 2.0 connection cable that is provided as part of the EVAL-CED1Z package.

EVALUATION BOARD SOFTWARE

INSTALLING THE SOFTWARE

The EVAL-AD7262/AD7264 evaluation kit includes self-installing software on CD. The software controls and evaluates the performance of the AD7262/AD7264 when it is operated with the EVAL-CED1Z. The software is compatible with Windows® 2000/XP®. If the setup file does not run automatically, **setup.exe** can be run directly from the CD.

When the CD is inserted into the PC, an installation program automatically begins. This program installs the evaluation software. The user interface on the PC is a dedicated program written especially for the AD7262 or AD7264 when operating with the EVAL-CED1Z.

The software should be installed before the USB cable is connected between the EVAL-CED1Z and the PC. This ensures that the appropriate USB driver files have been properly installed before the EVAL-CED1Z is connected to the PC.

When the software runs for the first time with the EVAL-CED1Z board connected to the PC, the PC automatically finds the new device and identifies it. Follow the on-screen instructions that appear. This installs the drivers for the CED on the PC. If an error appears on screen when the software is first opened, then the PC is not recognizing the USB device. This error is corrected by the following steps:

1. Click **My Computer**, then select **Properties**. When the **System Properties** window opens, select the **Hardware** tab.
2. Click **Device Manager**.
3. Examine the devices listed under the **Universal Serial Bus Controller** heading. If an unknown device is listed, right click this option and select **Update Driver**.
4. Note that the New Hardware Wizard runs twice. Under **ADI Development Tools**, the hardware is listed as **ADI Converter Evaluation and Development Board (WF)**.
5. Reboot your PC.

SETTING UP THE EVAL-CED1Z

This section describes how the evaluation board, the EVAL-CED1Z board, and the software should be setup to begin using the complete system.

1. Install the AD7262/AD7264 evaluation board software.
2. Connect the EVAL-CED1Z board and the evaluation board together via the 96-way connector. Apply power to the EVAL-CED1Z via +7 V, 15 W power supply provided. At this stage, the green LED labeled **Power** on the EVAL-CED1Z should be lit, which indicates that the EVAL-CED1Z is receiving power.
3. Connect the USB cable between the PC and the EVAL-CED1Z. A green LED positioned beside the USB connector on the EVAL-CED1Z board lights up indicating that the USB connection has been established.
4. The EVAL-AD7262/AD7264 is detected. Proceed through any dialog boxes that appear (use the recommended options) to finalize the installation.
5. Start the EVAL-AD7262/AD7264 software.

The FPGA on the EVAL-CED1Z is automatically programmed when the software is opened. The two red LEDs (D14 and D15) on the EVAL-CED1Z now light up. This indicates that the EVAL-CED1Z is functional and ready to receive instructions.
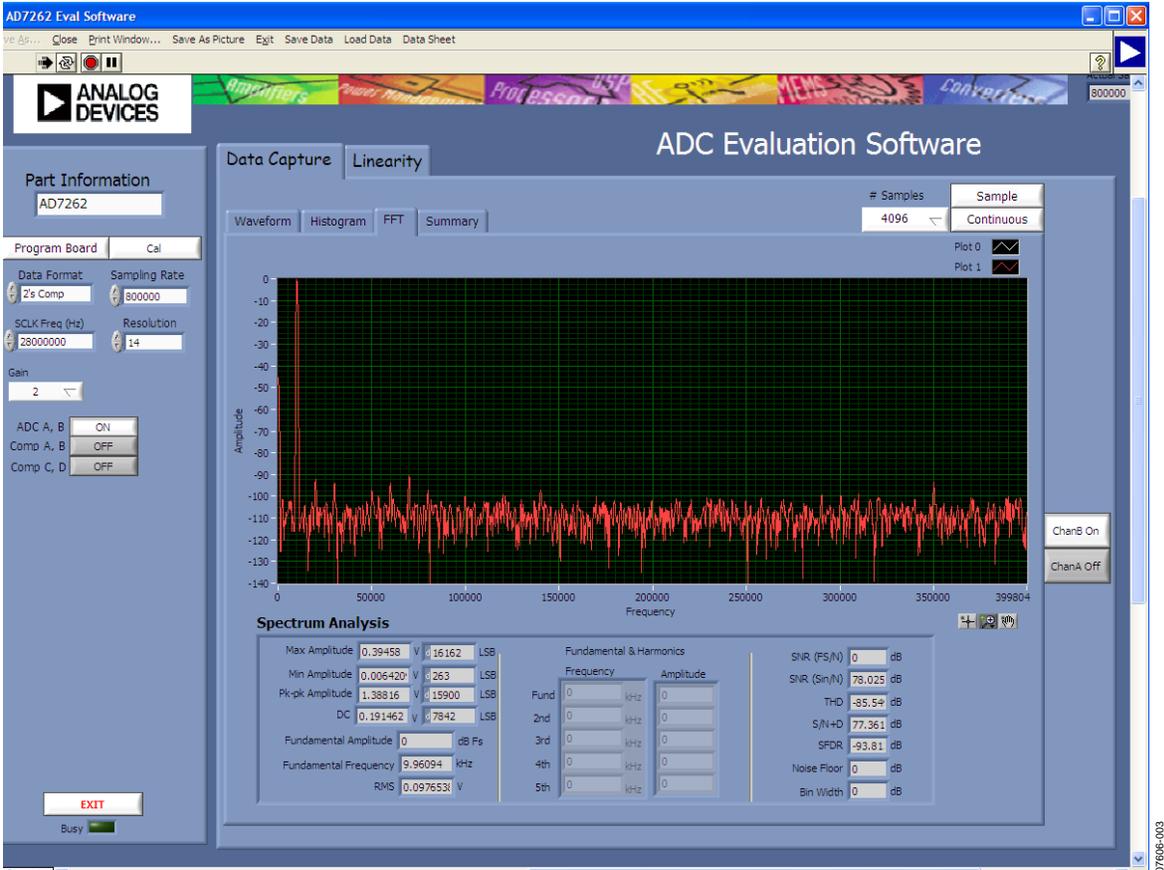
Figure 3. AD7262 Main Window

SOFTWARE OPERATION

With the hardware set up, use the software to control the EVAL-CED1Z and the EVAL-AD7262/AD7264. To launch the software from the **Analog Devices** menu, use the following steps:

1. Click the **AD7274/AD7262** submenu.
2. Click the **AD7274/AD7262 icon.** Figure 3 displays the main window that is opened.
3. If an error message appears, click **OK** and restart the application after checking the connection between the adapter board and the USB port on the PC. Also check that the USB device is identified by the device manager as detailed in the Installing the Software section.

The software that controls the EVAL-CED1Z and, therefore, the AD7262/AD7264 evaluation board, has two main windows. Figure 3 shows the window that appears when the software is run. The main function of this window is to allow you to read a predetermined number of samples from the evaluation board and display them in both the time and frequency domain. The top portion of the screen contains the menu bar and the screen can be divided into three main sections: **Part Information**, **Data Capture**, and **Linearity**. The **Data Capture** tab consists of four subtabs: **Waveform**, **Histogram**, **FFT**, and **Summary**.

The **Linearity** tab enables you to generate a linearity plot for the device.

USING THE SOFTWARE

MENU BAR

The menu bar consists of the following items: **File**, **Edit**, **Operate**, **Tools**, **Window**, and **Help**.

PART INFORMATION SECTION

The **Part Information** section allows you to select the following configuration options:

- Part Number: AD7264 or AD7262; the software automatically sets the resolution to 14 or 12 bits, respectively.
- Sampling Frequency: The maximum sampling frequency supported by the EVAL-AD7262/AD7264 is 1 MSPS.
- PGA Gain: The drop-down menu allows you to select the required AD7264 or AD7262 PGA gain setting. The AD7264 or AD7262 allow you to select PGA gains from 1 to 128.
- Power-On Setting: You can select the desired power on or off configuration by selecting to power on either, **ADC A, B**; **Comp A, B**; **Comp C, D**.
- Initiate a Calibration: A calibration of the AD7264 or AD7262 can be initiated by clicking **Cal**.

The **Part Information** tab also includes a **Busy** status indicator, which lights when the evaluation board is busy and an **Exit** button to allow you to quit the program.

DATA CAPTURE TAB

In the **Data Capture** tab, the user can select the number of samples to be captured from the drop-down menu. The default number of samples is 4096; you are free to change this as required. The desired display option is selected by clicking any one of the **Waveform**, **Histogram**, or **FFT** tab.

Waveform Tab

The **Waveform** tab displays a digital storage oscilloscope (DSO) that allows you to display a waveform. Samples are displayed here when uploaded from the EVAL-CED1Z board. The samples are displayed as integer code values.

At the bottom left of the graph are the zoom options. These allow you to zoom in and out to get a closer look at a sample. The **Waveform Analysis** section, which is located beneath the waveform graph, contains information about the samples taken; for example, minimum/maximum position or velocity, the spread, the standard deviation, and the mean.

The waveform graph displays the information for both ADC A and ADC B, or either ADC as desired. Two buttons located on the bottom right hand side of the graph, labeled **ChanA On/ Off** and **ChanB On/Off** are used to select which ADC's data is displayed. An indicator, located on the top right hand corner of the graph, shows what color graph represents each ADC when the data from both ADC's is displayed.

Histogram Tab

The **Histogram** tab displays a histogram of the captured ADC codes. It can be used to give an indication of the performance of the ADC in response to dc inputs. The **Histogram Analysis** section contains information about the samples taken; for example, maximum and minimum codes captured.

FFT Tab

The FFT tab displays an fast Fourier transform (FFT) plot. The FFT is typically used for examining the performance of the ADC in the frequency domain. The **Spectrum Analysis** section contains information about the samples taken, such as ac specifications (see Figure 3).

You can choose whether to display the information for ADC A, or ADC B, or both in the window using the **ChanA On/Off** and **ChanB On/Off** buttons, as explained in the Waveform Tab section.

LINEARITY TAB

In the **Linearity** tab, you can select the number of hits per code to be captured for the linearity analysis. The desired display option is selected by clicking the **Histogram**, **INL**, **DNL**, or **Summary** tab. To initiate the data collection, select the **Get Linearity Data** button. The data collection and analysis takes a few seconds to complete. The greater the number of hits per code selected, the longer the analysis takes.

Histogram Tab

The **Histogram** tab displays a histogram of the captured ADC codes. It can be used to give an indication of the performance of the ADC in response to dc inputs. The **Histogram Analysis** section contains information about the samples taken, for example, maximum and minimum codes captured.

INL Tab

The **INL** tab displays an INL plot for the AD7262 or AD7264. This plot can be used to examine the dc performance of the ADC. The **Linearity Analysis** section contains information on the maximum and minimum INL error and the code at which this error occurred. It also shows the total number of hits per code and the number of samples taken.

DNL Tab

The **DNL** tab displays a DNL plot for the AD7262 or AD7264. This plot can be used to examine the dc performance of the ADC in conjunction with the INL plot. The **Linearity Analysis** section contains information on the maximum and minimum DNL error and the code at which this error occurred. It also shows the total number of hits per code and the number of samples taken.

Summary Tab

The **Summary** tab displays the INL/DNL/histogram plots and results in the same place for convenient analysis.

TAKING SAMPLES

To initiate a conversion and capture the sample data, click the **Sample** button or the **Continuous** button. Both the **Sample** and the **Continuous** buttons are located on the top right hand corner of the **Data Capture** tab. When you click the **Sample** button, the software instructs the EVAL-CED1Z board to take the required number of samples at the required frequency from the evaluation board. The EVAL-AD7262/ AD7264 runs with sampling speeds less than or equal to 1 MSPS. You can choose the sampling frequency up to this rate and the number of samples to be taken.

The samples taken are then uploaded and displayed. An FFT and/or histogram can be calculated and displayed. If you click the **Continuous** button, the software repeats the process indefinitely until you click **Stop.** (The **Continuous** button switches to **Stop** when clicked). You can switch between displaying data from ADC A, ADC B, or both while the software is running continuously.

Note that no data appears on the screen if the ADCs are not powered on. The **ADC A, B,** button in the **Part Information** section should be set to **ON** to power on both ADCs.

EVALUATION BOARD SCHEMATICS AND ARTWORK

EVAL-AD7262/AD7264 schematics, silkscreen, and layout can be found in Figure 4 to Figure 8.
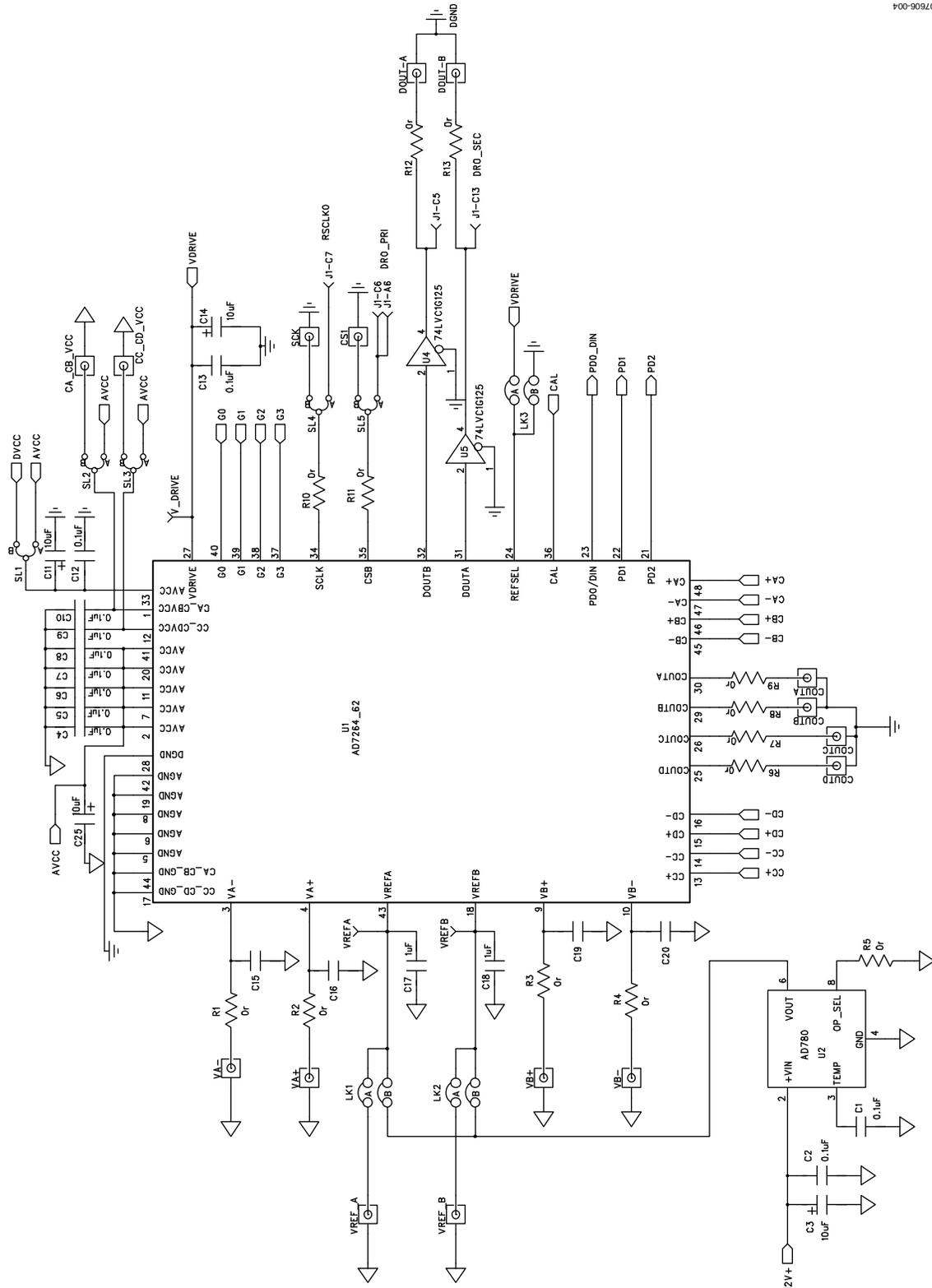

Figure 4. EVAL-AD7262/AD7264 Circuit Diagram 1

07606-005
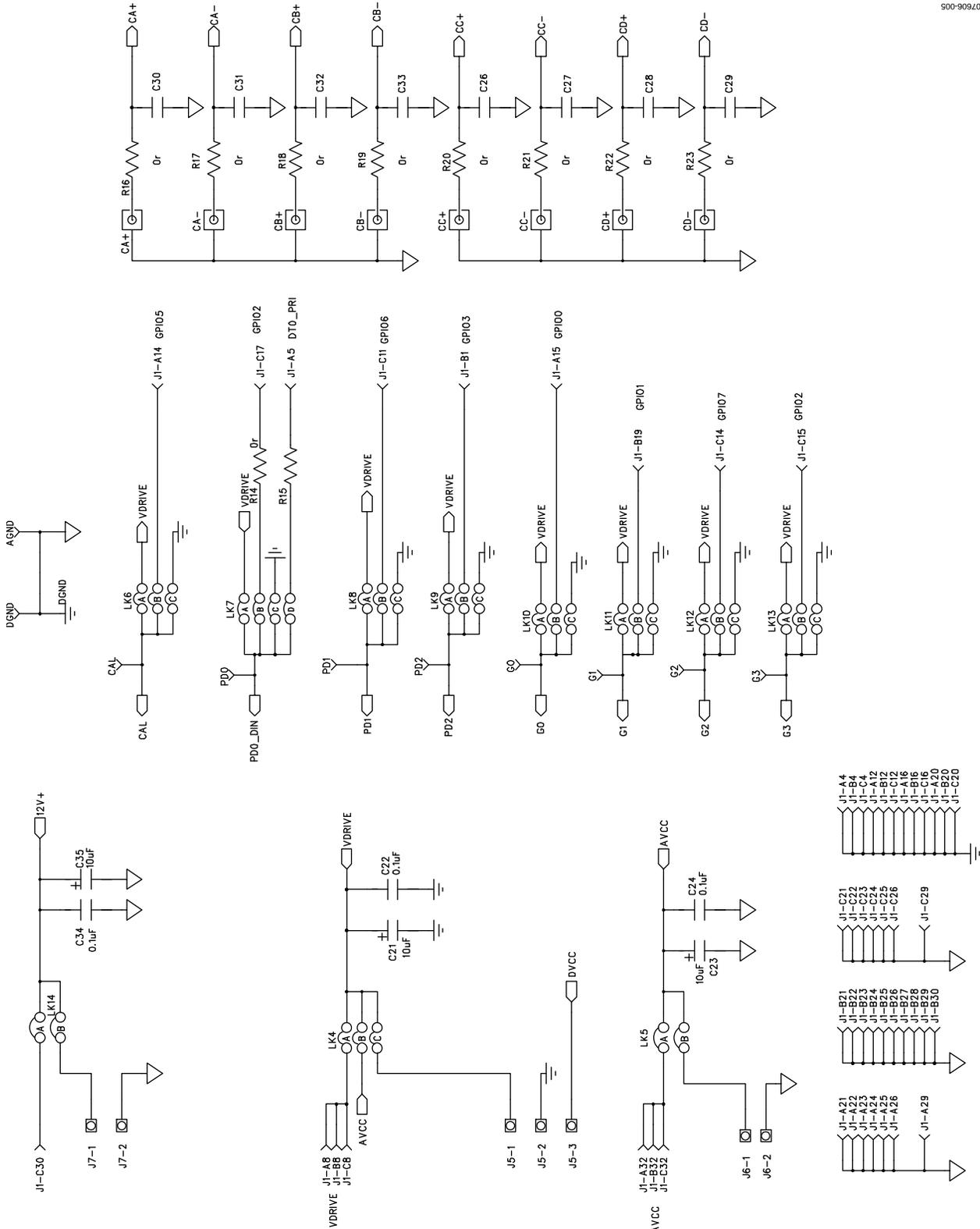
Figure 5. EVAL-AD7262/AD7264 Circuit Diagram 2
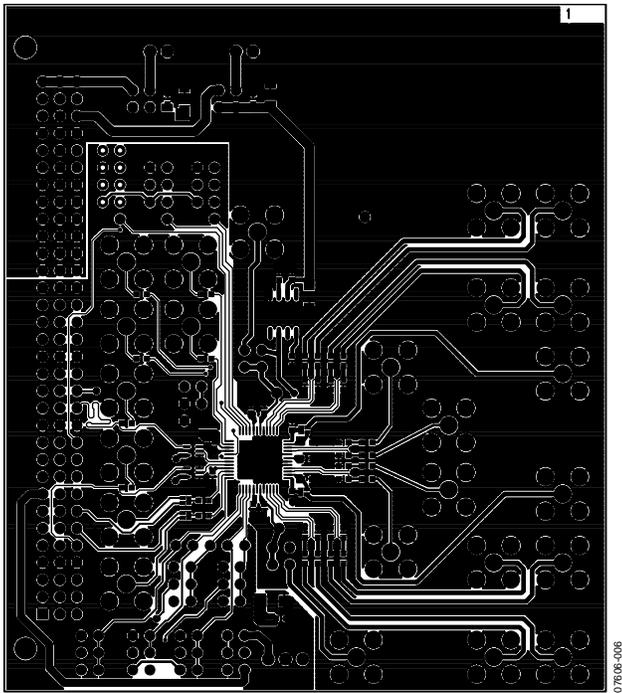
Figure 6. Component Side Artwork
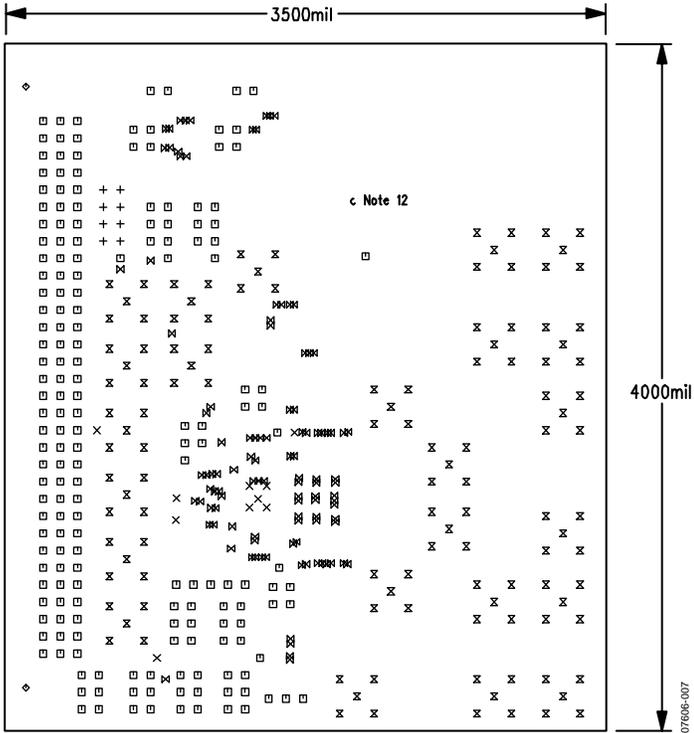
Figure 7. Solder Side Artwork
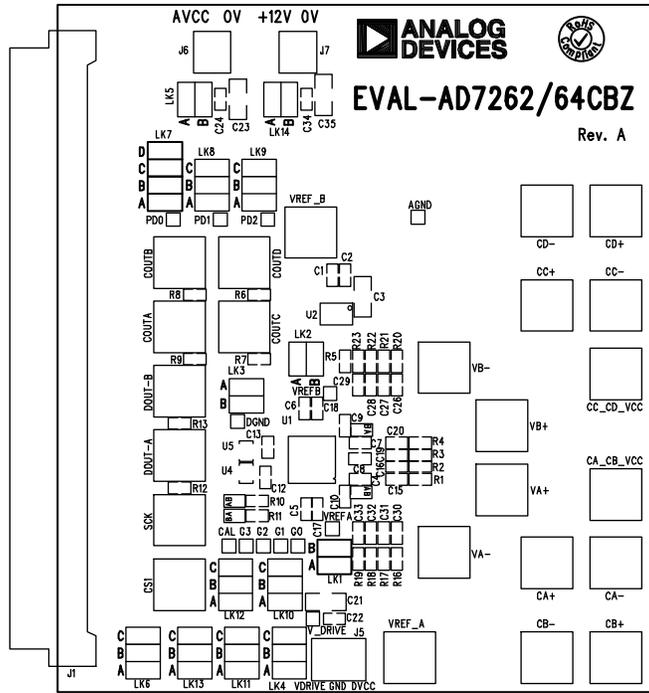
Figure 8. Silkscreen

ORDERING INFORMATION

BILL OF MATERIALS

Table 8.

Qty	Reference Designator	Description	Supplier/Number[1]
7	C1, C2, C12, C13, C22, C24, C34	0.1 µF capacitor	FEC 9406140
2	C17, C18	1 µF capacitor	FEC 1327680
7	C3, C11, C14, C21, C23, C25, C35	10 µF capacitor	Digi-Key PCC2417CT-ND
21	R1 to R23	0 Ω resistor	FEC 933-1662
1	U1	ADC, AD7262 or AD7264	Analog Devices AD7262BSTZ, AD7264BSTZ
1	U2	AD780	Analog Devices, AD780ARZ
2	U4, U5	74LVC1G125	FEC 147-0771
1	J1	96 -way connector, CON\41612\96	FEC 1096832
2	J6, J7	Terminal block, connector\power 2-way	FEC 3041359
1	J5	Terminal block, connector\power 3-way	FEC 3041360
24	CA+, CA−, CA_CB_VCC, CB+, CB−, CC+, CC−, CC_CD_VCC, CD+, CD−, COUTA, COUTB, COUTC, COUTD, CS1, DOUT-A, DOUT-B, SCK, VA+, VA−, VB−, VB+, VREF_A, VREF_B	SMB connector	FEC 1111349
14	LK1 to LK14	Jumper	FEC 1022244
11	CAL, DGND, G1, G2, G3, G0, PD0, PD1, VREF_A, VREF_B, V_DRIVE	Test points	FEC 8731144

[1] FEC = Farnell Electronics, Inc.

ORDERING GUIDE

Model	Description
EVAL-AD7262EDZ[1]	Evaluation Board for AD7262
EVAL-AD7264EDZ[1]	Evaluation Board for AD7264
EVAL- CED1Z[1]	Controller Board

[1] Z = RoHS Compliant Part.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

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**ANALOG
DEVICES**

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