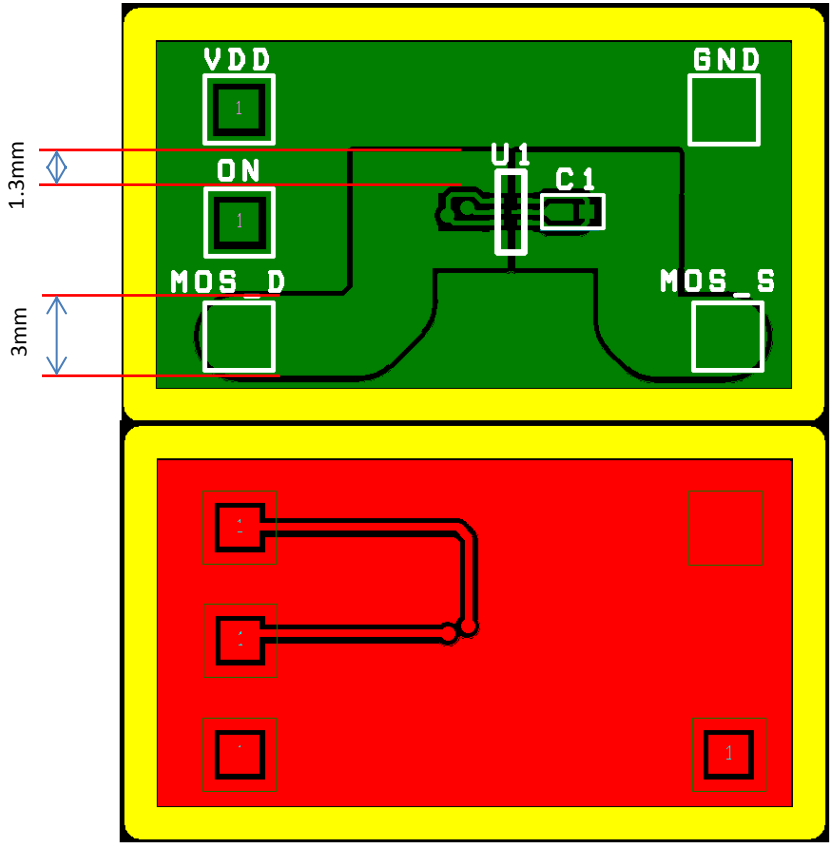

Figure 3. SLG59M1568V PCB Layout Suggestion for handling 9A

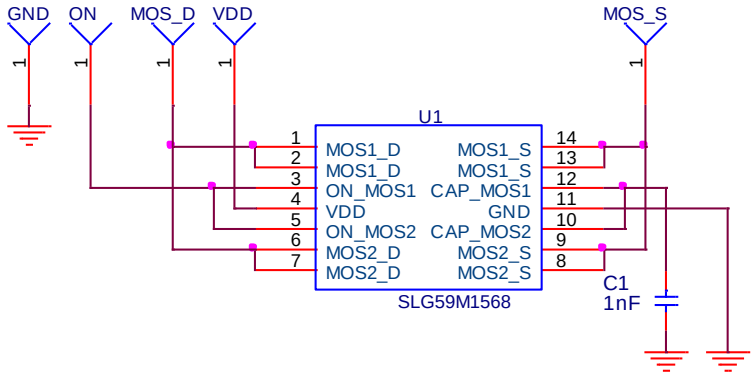

Figure 4. SLG59M1568V Connection Circuit

SILEGO

GreenFET3
SLG59M1568V
Layout Guide

Content

Description

The SLG59M1568V are 9 mΩ, ~ 9 A load switch that is able to switch 1.0 to 5.25 V power rails. The product is packaged in an ultra-small 1 x 3 mm package.

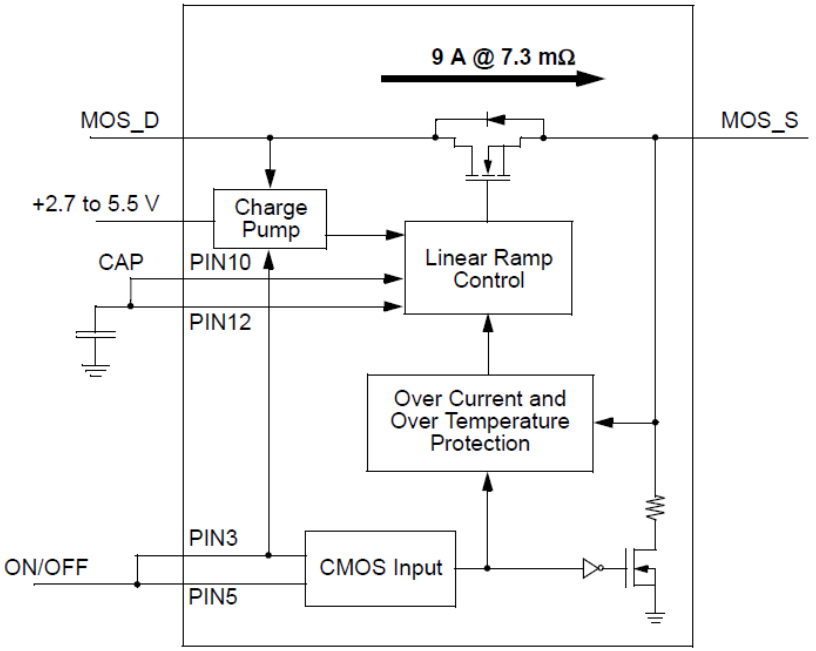

Figure 1: SLG59M1568V Block Diagram

This layout guide provides some important information about the PCB layout of SLG59M1568V applications.

SILEGO STDFN 1 x 3 - 14L PKG

Unit: um

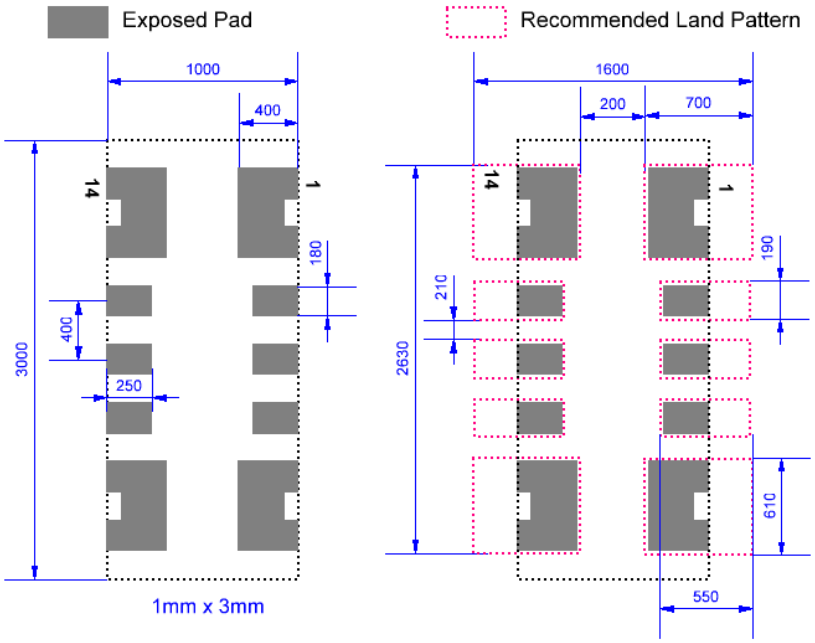

Figure 2. SLG59M1568V Package Dimensions and Recommended Land Pattern

2. Power and Ground Planes

2.1. The VDD pin needs 0.1uF external capacitor to smooth pulses from the power supply. Locate these capacitor close to PIN4.

2.2. The trace length from the control IC to the ON pin should be as short as possible and must avoid crossing this trace with power rails.

2.3. The MOS_D and MOS_S pins carry significant current. Please note how the MOS_D and MOS_S pads are placed directly on the power planes in Figure 3, which minimizes the RDS(ON) associated with long, narrow traces. The MOS_D and MOS_S pins dissipate most of the heat generated during high-load current condition. The layout shown in Figure 3 is illustrating a proper solution for heat to transfer as efficiently as possible out of the device. For handling 9A please use 3mm or higher trace width. Separate traces with 1.3mm width for MOS1_D, MOS2_2, MOS1_S, MOS2_S near device will be enough that each channel can handle 4.5A.

2.4. The GND pin (PIN11) should be connected to GND.

2.5. 2 oz. copper is recommended for higher currents.