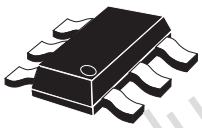
STT2PF60L

P-CHANNEL 60V - 0.20Ω - 2A - SOT-23-6L
STripFET™ II Power MOSFET

General features

Type	V_{DSS}	$R_{DS(on)}$	I_D
STT2PF60L	60V	< 0.25Ω	2A

- Standard outline for easy automated surface mount assembly
- Low threshlod drive

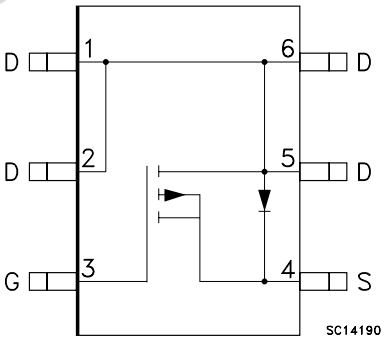


SOT23-6L

Description

This Power MOSFET is the latest development of STMicroelectronics unique “Single Feature Size™” strip-based process. The resulting transistor shows extremely high packing density for low on-resistance, rugged avalanche characteristics and less critical alignment steps therefore a remarkable manufacturing reproducibility.

Internal schematic diagram



Applications

- DC motor drive
- DC-DC converters
- Battery management in nomadic equipment
- Power management in portable/desktop PCs
- Cellular

Order codes

Sales Type	Marking	Package	Packaging
STT2PF60L	STP6	SOT23-6L	Tape & Reel

1 Electrical ratings

Table 1. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-Source Voltage (V_{GS} = 0)	60	V
V_{DGR}	Drain-gate Voltage (R_{GS} = 20kΩ)	60	V
V_{GS}	Gate-Source Voltage	±15	V
I_D	Drain Current (continuous) at T_C = 25°C	2	A
I_D	Drain Current (continuous) at T_C=100°C	1.3	A
I_{DM}(1)	Drain Current (pulsed)	8	A
P_{TOT}	Total Dissipation at T_C = 25°C	1.6	W

1. Pulse width limited by safe operating area

Table 2. Thermal data

Symbol	Parameter	Value	Unit
$R_{thJ\text{-}amb}$(1)	Thermal resistance junction-case Max	78	°C/W
T_j	Maximum operating junction temperature	150	°C
T_{stg}	Storage temperature	-55 to 150	°C

1. Mounted on a 1 in^2 pad of 2 oz Cu in FR-4 board for t<10sec

Note: For the P-Channel MOSFET actual polarity of voltage and current has to be reversed

2 Electrical characteristics

(T_{CASE}=25°C unless otherwise specified)

Table 3. On/off states

Symbol	Parameter	Test Condictions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-Source Breakdown Voltage	I_D = 250µA, V_{GS}= 0	60			V
I_{DSS}	Zero Gate Voltage Drain Current (V_{GS} = 0)	V_{DS} = Max Rating, V_{DS} = Max Rating,Tc=125°C			1 10	µA µA
I_{GSS}	Gate Body Leakage Current (V_{DS} = 0)	V_{GS} = ±15V			±100	nA
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS}= V_{GS}, I_D = 250µA	1			V
$R_{DS(on)}$	Static Drain-Source On Resistance	V_{GS}= 10V, I_D= 1A V_{GS}= 4.5V, I_D= 1A		0.20 0.24	0.25 0.30	Ω Ω

Table 4. Dynamic

Symbol	Parameter	Test Condictions	Min.	Typ.	Max.	Unit
g_{fs} (1)	Forward Transconductance	V_{DS} =10V, I_D = 1A		3		S
C_{iss} C_{oss} C_{rss}	Input Capacitance Output Capacitance Reverse Transfer Capacitance	V_{DS} =25V, f=1 MHz, V_{GS}=0		313 67 25		pF pF pF
Q_g Q_{gs} Q_{gd}	Total Gate Charge Gate-Source Charge Gate-Drain Charge	V_{DD}=30V, I_D = 24A V_{GS} =10V (see Figure 14)		5 0.5 2.2	7	nC nC nC

1. Pulsed: pulse duration=300µs, duty cycle 1.5%

Note: For the P-Channel MOSFET actual polarity of voltage and current has to be reversed

Table 5. Switching times

Symbol	Parameter	Test Condictions	Min.	Typ.	Max.	Unit
$t_{d(on)}$ t_r	Turn-on Delay Time Rise Time	V_{DD}= 30V, I_D=1A, R_G=4.7Ω, V_{GS}=4.5V (see Figure 13)		44 34		ns ns
$t_{d(off)}$ t_f	Turn-off Delay Time Fall Time	V_{DD}= 30V, I_D=1A, R_G=4.7Ω, V_{GS}=4.5V (see Figure 13)		42 15		ns ns

Table 6. Source drain diode

Symbol	Parameter	Test Condictions	Min.	Typ.	Max.	Unit
I_{SD} I_{SDM}(1)	Source-drain Current Source-drain Current (pulsed)				2 8	A A
V_{SD}(2)	Forward on Voltage	I_{SD}=2A, V_{GS}=0			1.2	V
t_{rr} Q_{rr} I_{RRM}	Reverse Recovery Time Reverse Recovery Charge Reverse Recovery Current	I_{SD}=2A, di/dt = 100A/µs, V_{DD}=30 V, Tj=150°C		38 36.3 2.5		ns nC A

1. Pulse width limited by safe operating area
2. Pulsed: pulse duration=300µs, duty cycle 1.5%

Note: For the P-Channel MOSFET actual polarity of voltage and current has to be reversed

2.1 Electrical characteristics (curves)

Figure 1. Safe operating area

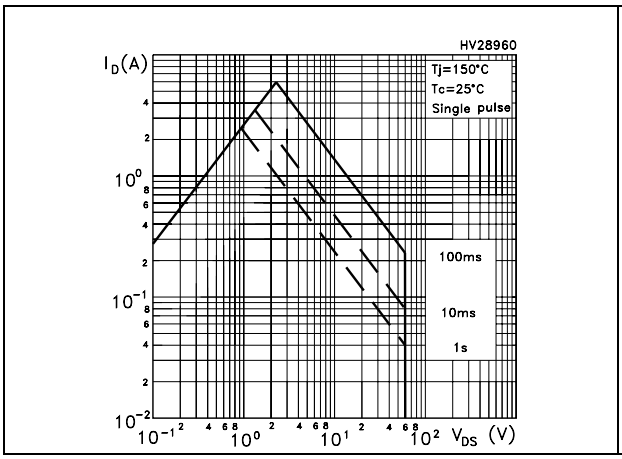


Figure 2. Thermal impedance

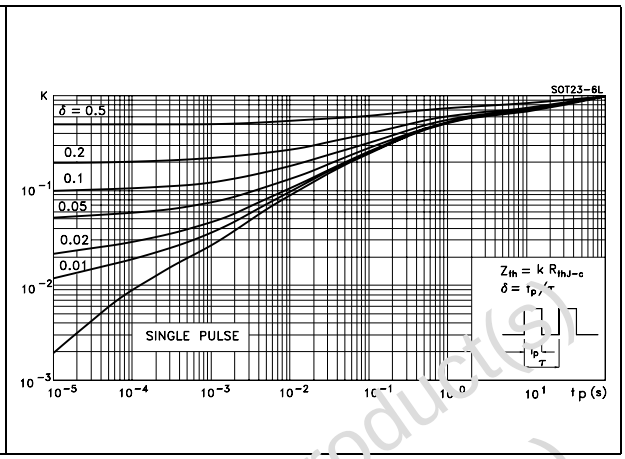


Figure 3. Output characterisics

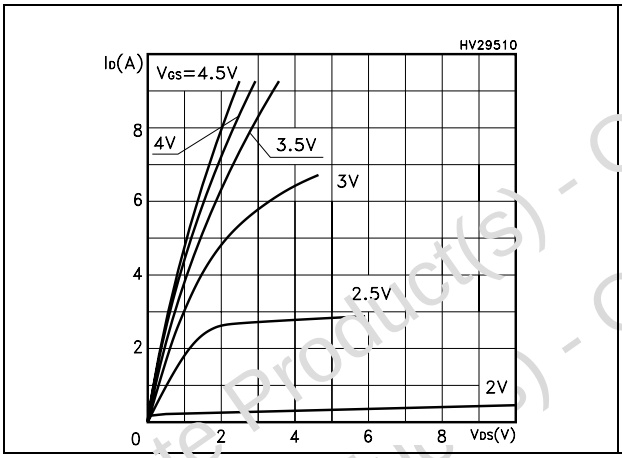


Figure 4. Transfer characteristics

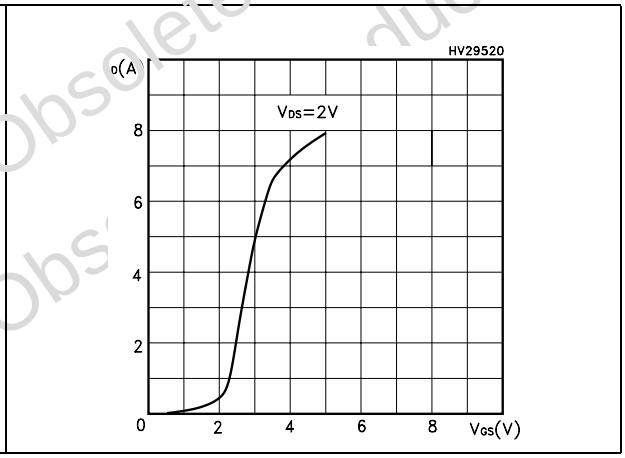


Figure 5. Transconductance

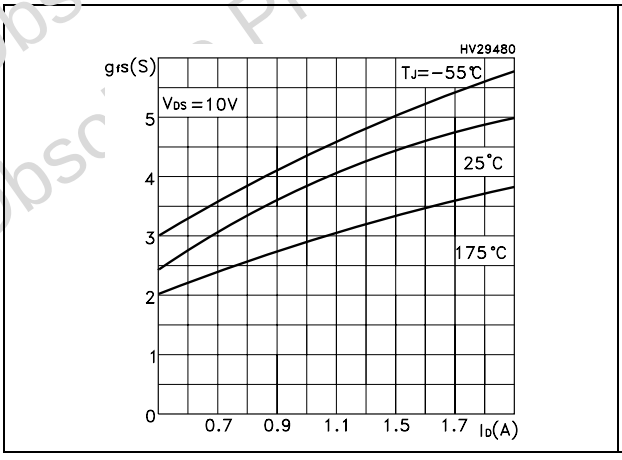


Figure 6. Static drain-source on resistance

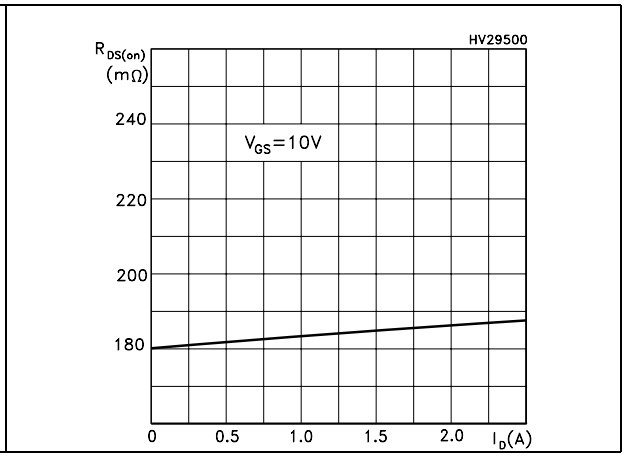


Figure 7. Gate charge vs gate-source voltage

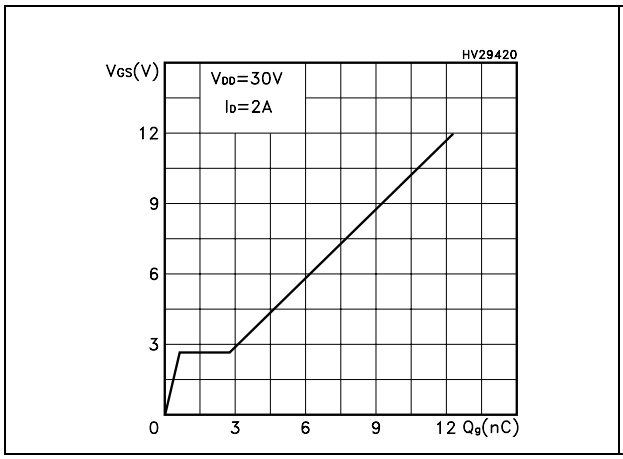


Figure 8. Capacitance variations

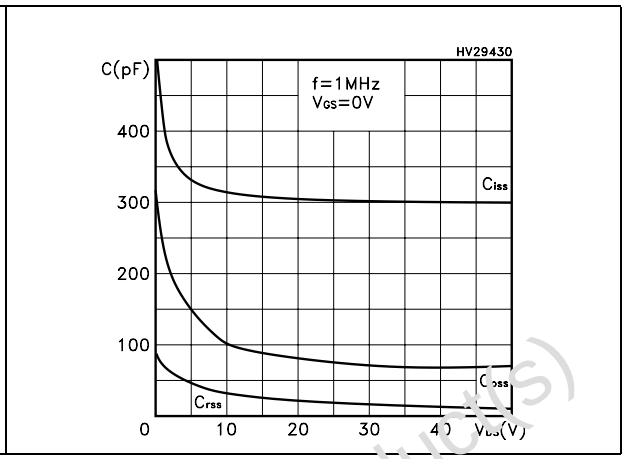


Figure 9. Normalized gate threshold voltage vs temperature

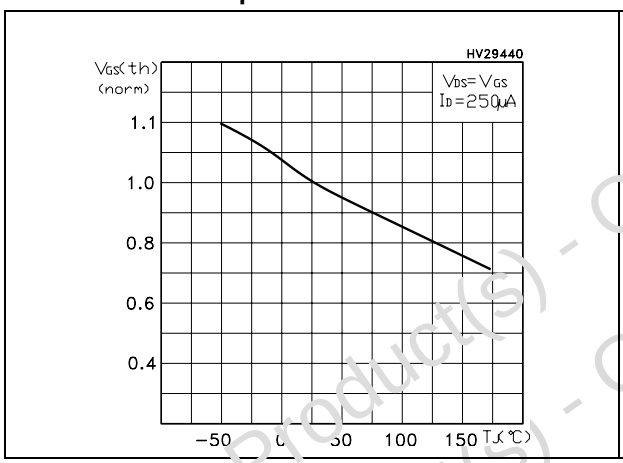


Figure 10. Normalized on resistance vs temperature

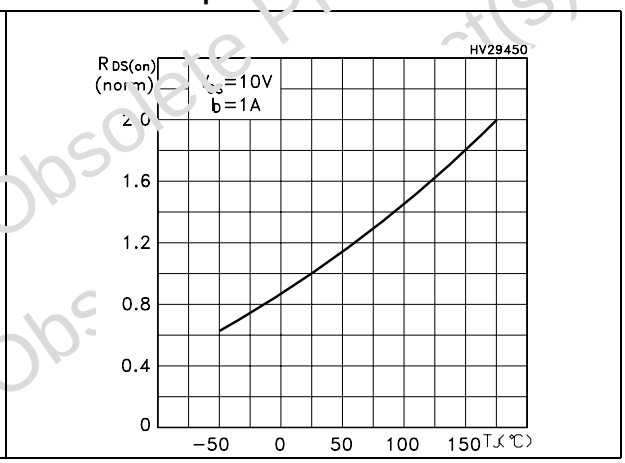


Figure 11. Source-drain diode forward characteristics

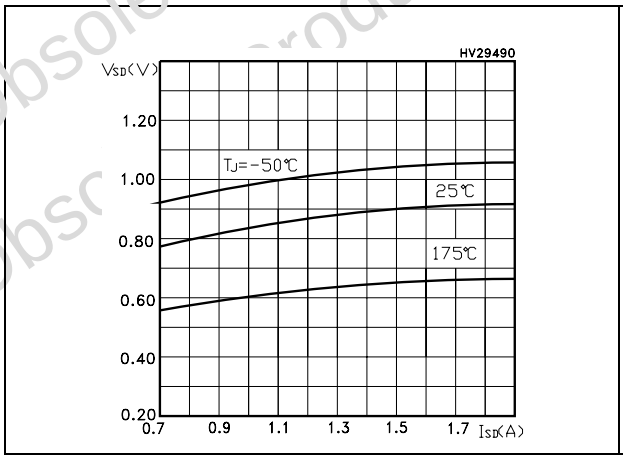
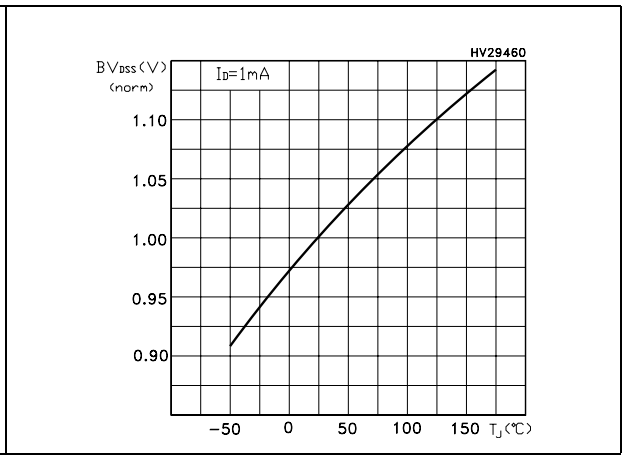


Figure 12. Normalized B_{VDSS} vs temperature



3 Test circuit

Figure 13. Switching times test circuit for resistive load

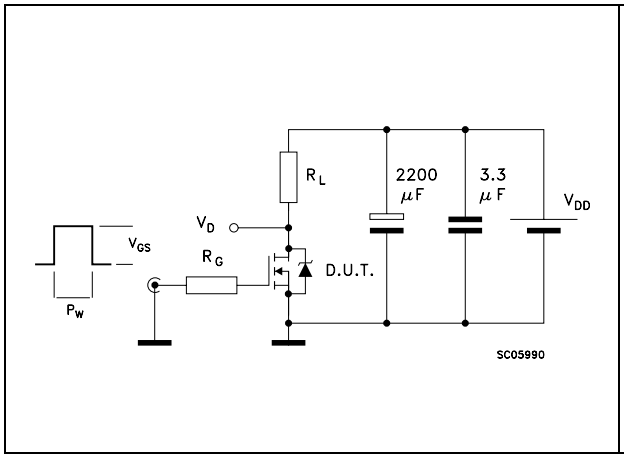


Figure 14. Gate charge test circuit

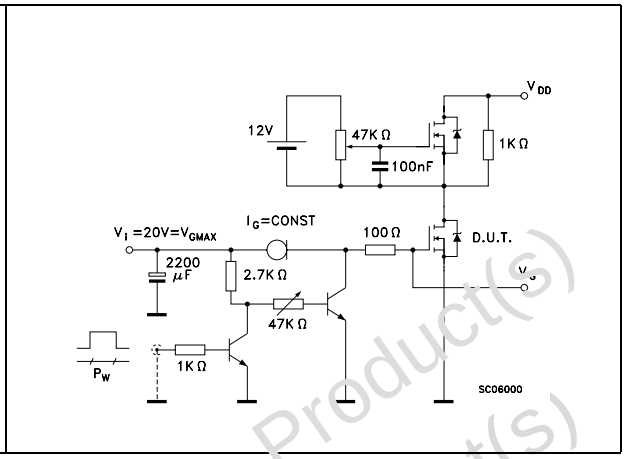


Figure 15. Test circuit for inductive load switching and diode recovery times

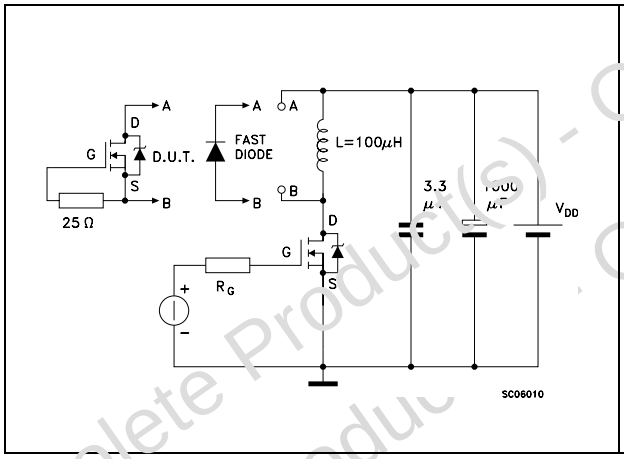


Figure 16. Unclamped Inductive load test circuit

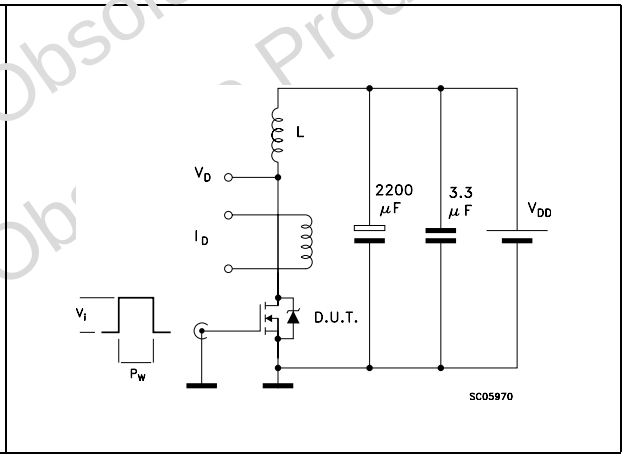
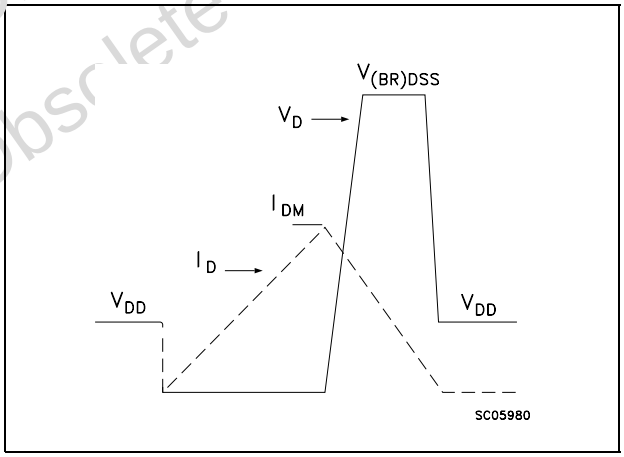


Figure 17. Unclamped inductive waveform

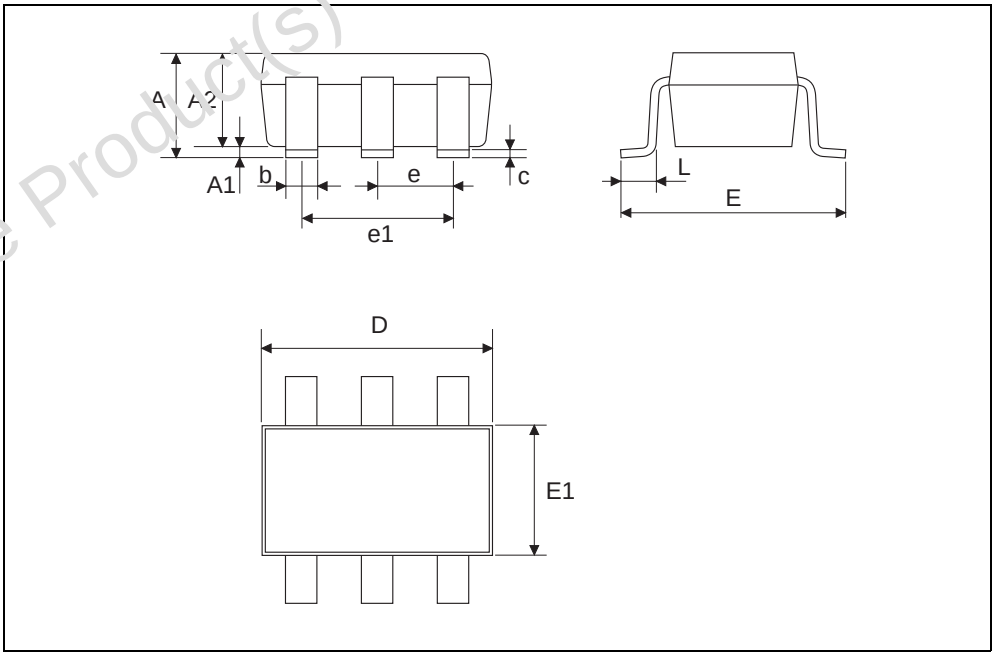


4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a Lead-free second level interconnect . The category of second level interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: www.st.com

TSOP-6 MECHANICAL DATA

DIM.	mm			mils		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	0.90		1.45	0.035		0.057
A1	0.00		0.15	0.000		0.006
A2	0.90		1.30	0.035		0.051
b	0.25		0.50	0.010		0.020
C	0.09		0.20	0.004		0.008
D	2.80		3.10	0.110		0.122
E	2.60		3.00	0.102		0.118
E1	1.50		1.75	0.059		0.069
L	0.35		0.55	0.014		0.022
e		0.95			0.037	
e1		1.90			0.075	



5 Revision history

Table 7. Document revision history

Date	Revision	Changes
07-May-2002	1	Initial release.
19-Apr-2003	2	Preliminary version
22-Dec-2005	3	Final version