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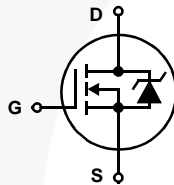## N-Channel UltraFET Power MOSFET
80 V, 75 A, 14 mΩ

Packaging

JEDEC TO-220AB

SOURCE
DRAIN
GATE

DRAIN (FLANGE)

Symbol

D

G

S
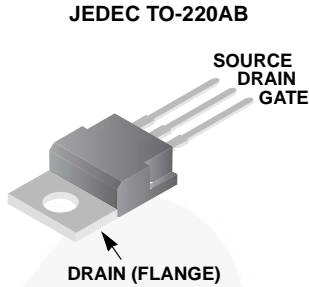
Features

- Ultra Low On-Resistance
  - $r_{DS(ON)} = 0.014\Omega$, $V_{GS} = 10V$
- Simulation Models
  - Temperature Compensated PSPICE® and SABER™ Electrical Models
  - Spice and SABER Thermal Impedance Models
  - www.fairchildsemi.com
- Peak Current vs Pulse Width Curve
- UIS Rating Curve

Ordering Information

PART NUMBER	PACKAGE	BRAND
HUF75542P3	TO-220AB	75542P

Absolute Maximum Ratings $T_C = 25^oC$, Unless Otherwise Specified

		HUF75542P3	UNITS
Drain to Source Voltage (Note 1)	V_{DSS}	80	V
Drain to Gate Voltage ($R_{GS} = 20k\Omega$) (Note 1)	V_{DGR}	80	V
Gate to Source Voltage	V_{GS}	±20	V
Drain Current			
Continuous ($T_C = 25^oC$, $V_{GS} = 10V$) (Figure 2)	I_D	75	A
Continuous ($T_C = 100^oC$, $V_{GS} = 10V$) (Figure 2)	I_D	58	A
Pulsed Drain Current	I_{DM}	Figure 4	
Pulsed Avalanche Rating	UIS	Figures 6, 14, 15	
Power Dissipation	P_D	230	W
Derate Above 25°C		1.54	W/^{o}C
Operating and Storage Temperature	T_J, T_{STG}	-55 to 175	^{o}C
Maximum Temperature for Soldering			
Leads at 0.063in (1.6mm) from Case for 10s.	T_L	300	^{o}C
Package Body for 10s, See Techbrief TB334.	T_{pkg}	260	^{o}C

NOTE:

1. $T_J = 25^oC$ to 150^oC.

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Product reliability information can be found at http://www.fairchildsemi.com/products/discrete/reliability/index.html
For severe environments, see our Automotive HUFA series.
All Fairchild semiconductor products are manufactured, assembled and tested under ISO9000 and QS9000 quality systems certification.

HUF75542P3

Electrical Specifications $T_C = 25^oC$, Unless Otherwise Specified

PARAMETER	SYMBOL	TEST CONDITIONS		MIN	TYP	MAX	UNITS
OFF STATE SPECIFICATIONS							
Drain to Source Breakdown Voltage	BV_{DSS}	$I_D = 250\mu A$, $V_{GS} = 0V$ (Figure 11)		80	-	-	V
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 75V$, $V_{GS} = 0V$		-	-	1	μA
		$V_{DS} = 70V$, $V_{GS} = 0V$, $T_C = 150^oC$		-	-	250	μA
Gate to Source Leakage Current	I_{GSS}	$V_{GS} = \pm 20V$		-	-	± 100	nA
ON STATE SPECIFICATIONS							
Gate to Source Threshold Voltage	$V_{GS(TH)}$	$V_{GS} = V_{DS}$, $I_D = 250\mu A$ (Figure 10)		2	-	4	V
Drain to Source On Resistance	$r_{DS(ON)}$	$I_D = 75A$, $V_{GS} = 10V$ (Figure 9)		-	0.012	0.014	Ω
THERMAL SPECIFICATIONS							
Thermal Resistance Junction to Case	$R_{\theta JC}$	TO-220		-	-	0.65	$^oC/W$
Thermal Resistance Junction to Ambient	$R_{\theta JA}$			-	-	62	$^oC/W$
SWITCHING SPECIFICATIONS ($V_{GS} = 10V$)							
Turn-On Time	t_{ON}	$V_{DD} = 40V$, $I_D = 75A$ $V_{GS} = 10V$, $R_{GS} = 3.9\Omega$ (Figures 18, 19)		-	-	195	ns
Turn-On Delay Time	$t_{d(ON)}$			-	12.5	-	ns
Rise Time	t_r			-	117	-	ns
Turn-Off Delay Time	$t_{d(OFF)}$			-	50	-	ns
Fall Time	t_f			-	80	-	ns
Turn-Off Time	t_{OFF}			-	-	195	ns
GATE CHARGE SPECIFICATIONS							
Total Gate Charge	$Q_{g(TOT)}$	$V_{GS} = 0V$ to $20V$	$V_{DD} = 40V$, $I_D = 75A$, $I_{g(REF)} = 1.0mA$ (Figures 13, 16, 17)	-	150	180	nC
Gate Charge at 10V	$Q_{g(10)}$	$V_{GS} = 0V$ to $10V$		-	80	96	nC
Threshold Gate Charge	$Q_{g(TH)}$	$V_{GS} = 0V$ to $2V$		-	5.7	7	nC
Gate to Source Gate Charge	Q_{gs}			-	15	-	nC
Gate to Drain "Miller" Charge	Q_{gd}			-	33	-	nC
CAPACITANCE SPECIFICATIONS							
Input Capacitance	C_{ISS}	$V_{DS} = 25V$, $V_{GS} = 0V$, f = 1MHz (Figure 12)		-	2750	-	pF
Output Capacitance	C_{OSS}			-	700	-	pF
Reverse Transfer Capacitance	C_{RSS}			-	250	-	pF

Source to Drain Diode Specifications

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Source to Drain Diode Voltage	V_{SD}	$I_{SD} = 75A$	-	-	1.25	V
		$I_{SD} = 37.5A$	-	-	1.00	V
Reverse Recovery Time	t_{rr}	$I_{SD} = 75A$, $dI_{SD}/dt = 100A/\mu s$	-	-	102	ns
Reverse Recovered Charge	Q_{RR}	$I_{SD} = 75A$, $dI_{SD}/dt = 100A/\mu s$	-	-	255	nC

Typical Performance Curves

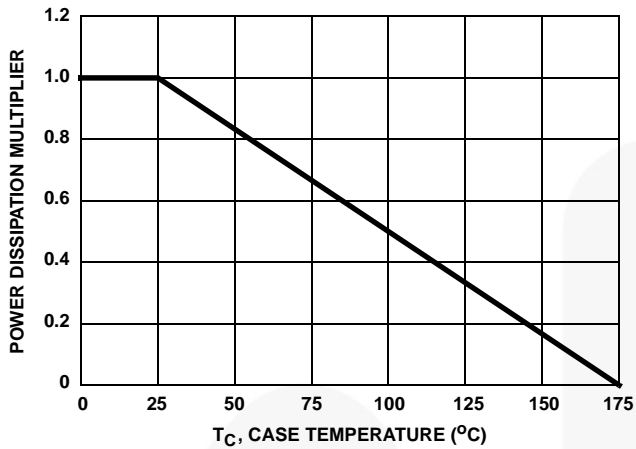
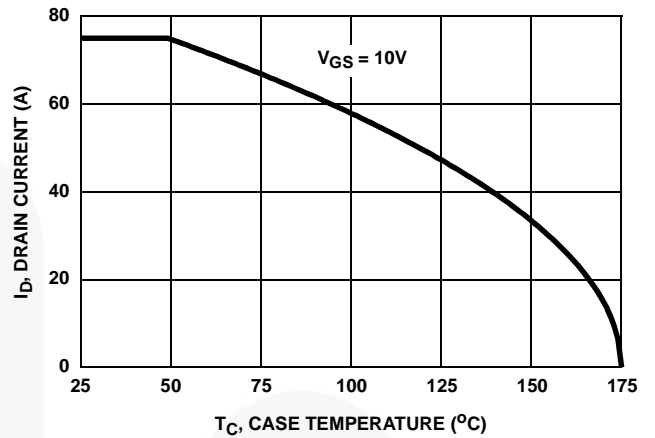FIGURE 1. NORMALIZED POWER DISSIPATION vs CASE TEMPERATURE

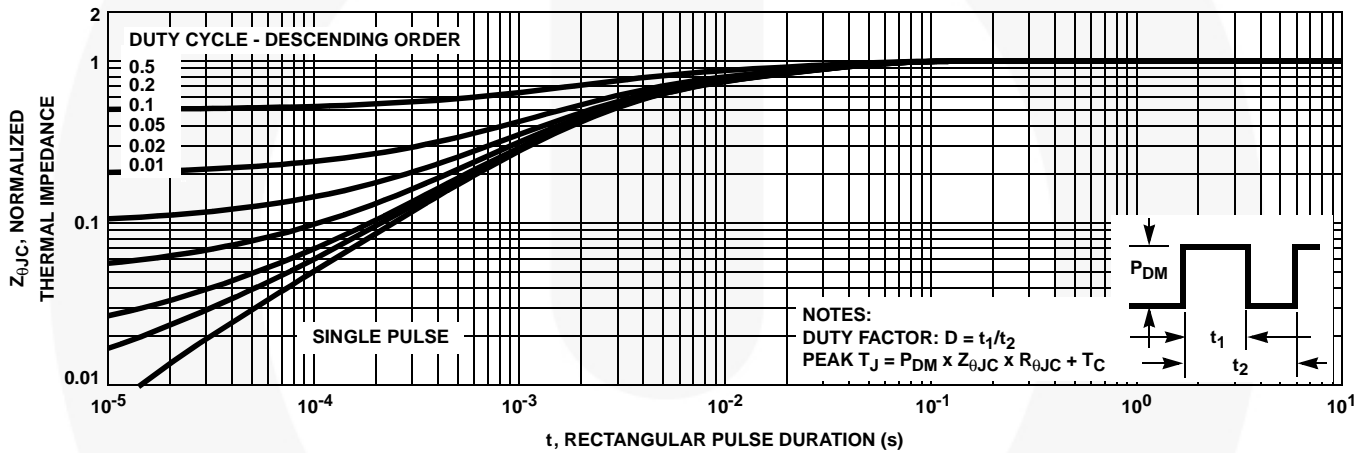FIGURE 2. MAXIMUM CONTINUOUS DRAIN CURRENT vs CASE TEMPERATURE

NOTES:
DUTY FACTOR: $D = t_1/t_2$
PEAK $T_J = P_{DM} \times Z_{\theta JC} \times R_{\theta JC} + T_C$

FIGURE 3. NORMALIZED MAXIMUM TRANSIENT THERMAL IMPEDANCE

$T_C = 25^oC$

FOR TEMPERATURES ABOVE 25°C DERATE PEAK CURRENT AS FOLLOWS:

$I = I_{25} \left[\sqrt{\dfrac{175 - T_C}{150}} \right]$

TRANSCONDUCTANCE MAY LIMIT CURRENT IN THIS REGION
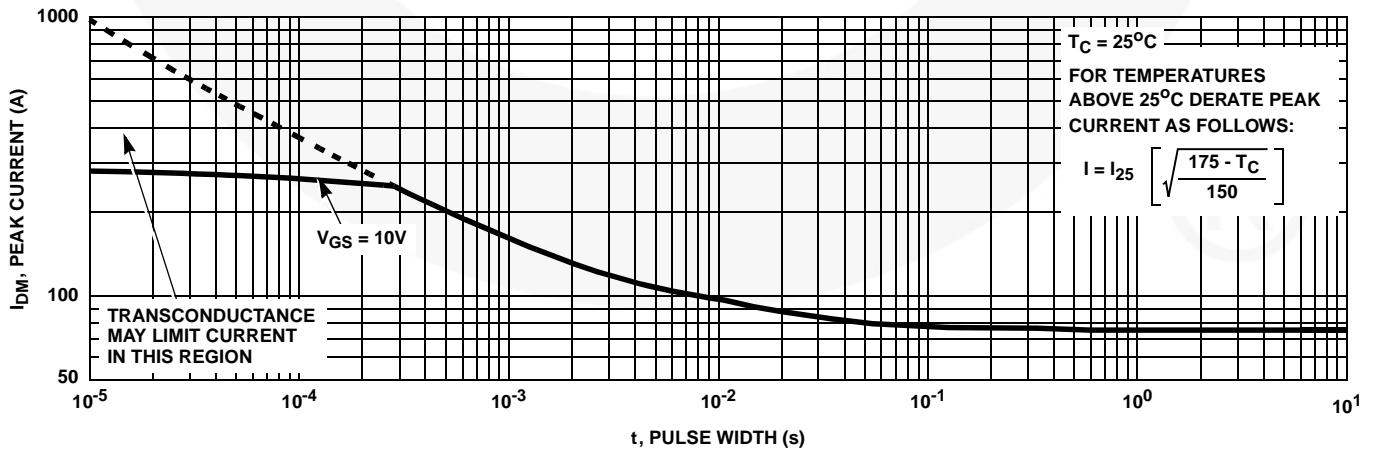
FIGURE 4. PEAK CURRENT CAPABILITY

Typical Performance Curves (Continued)
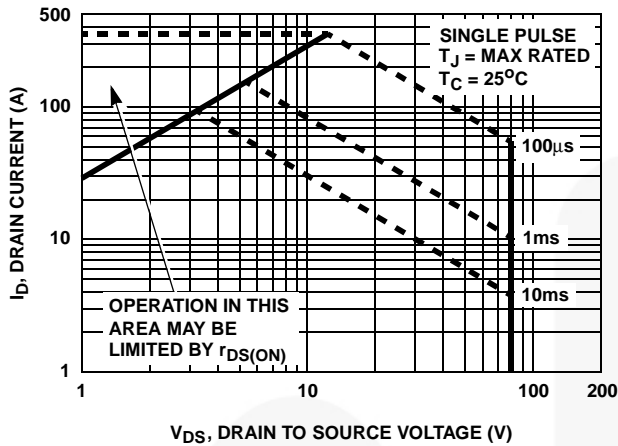
FIGURE 5. FORWARD BIAS SAFE OPERATING AREA
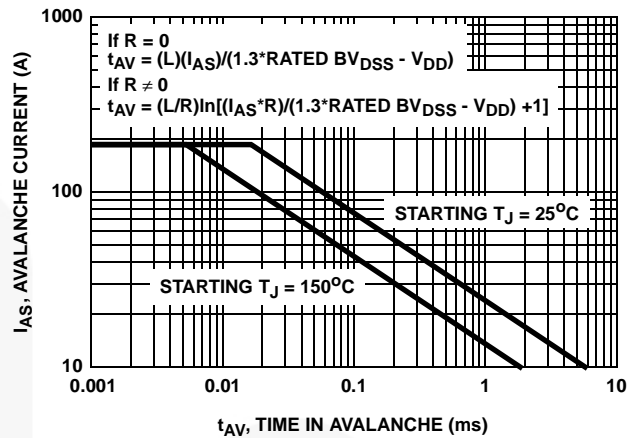
NOTE: Refer to Fairchild Application Notes AN9321 and AN9322.

FIGURE 6. UNCLAMPED INDUCTIVE SWITCHING
CAPABILITY
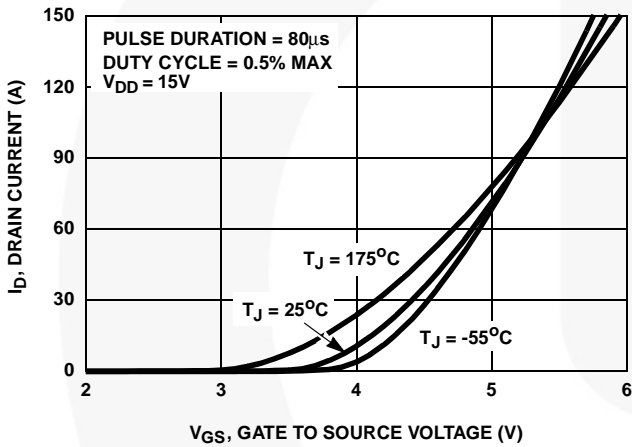
FIGURE 7. TRANSFER CHARACTERISTICS
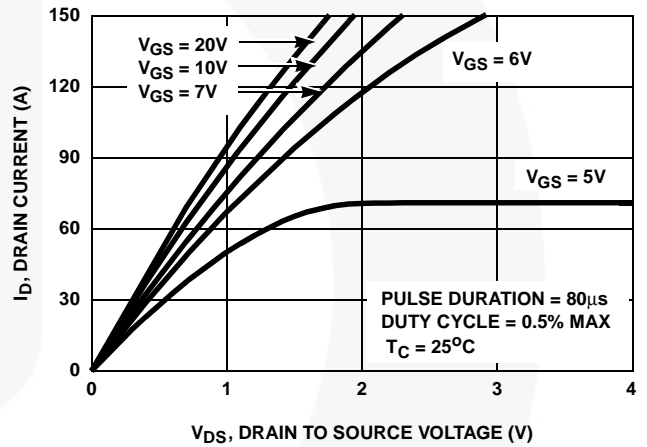
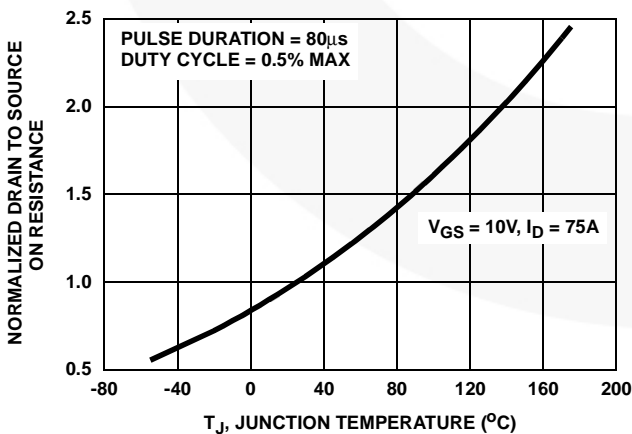FIGURE 8. SATURATION CHARACTERISTICS

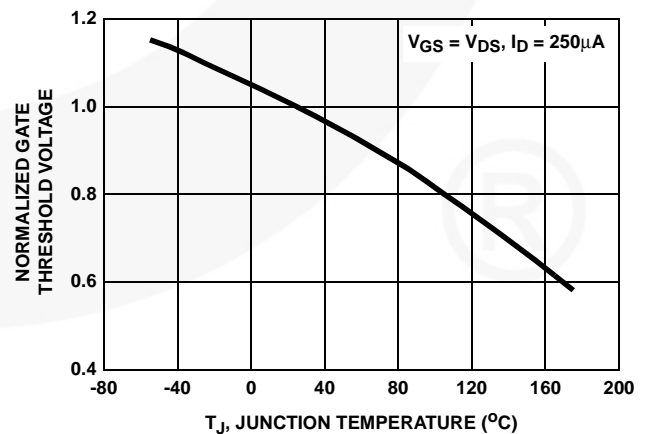FIGURE 9. NORMALIZED DRAIN TO SOURCE ON
RESISTANCE vs JUNCTION TEMPERATURE

FIGURE 10. NORMALIZED GATE THRESHOLD VOLTAGE vs
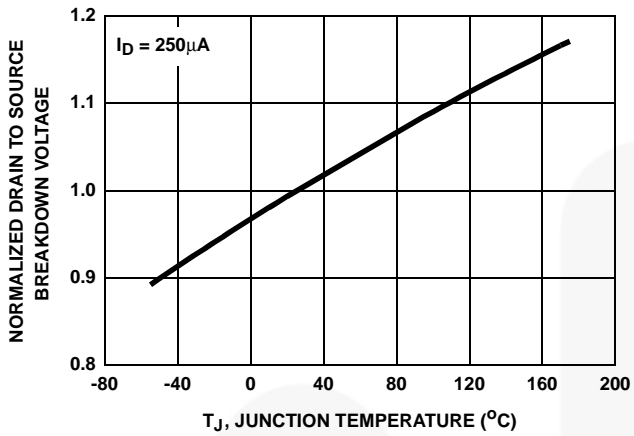JUNCTION TEMPERATURE

Typical Performance Curves (Continued)

**FIGURE 11. NORMALIZED DRAIN TO SOURCE BREAKDOWN
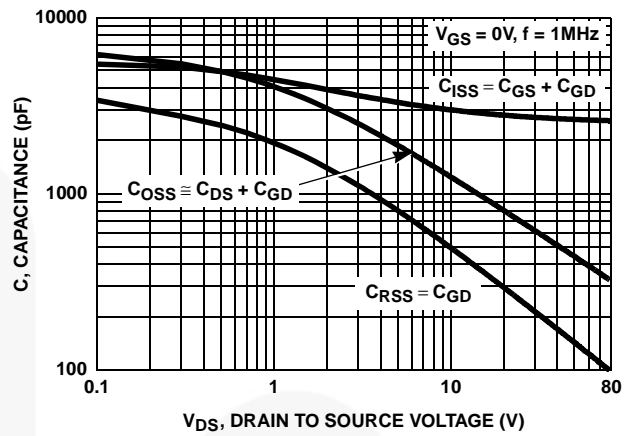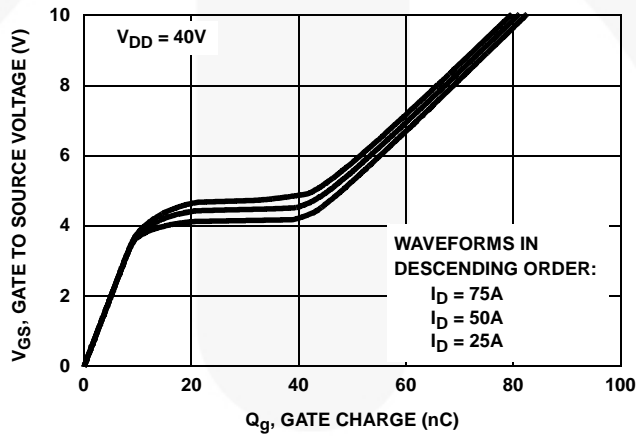VOLTAGE vs JUNCTION TEMPERATURE**

FIGURE 12. CAPACITANCE vs DRAIN TO SOURCE VOLTAGE

NOTE: Refer to Fairchild Application Notes AN7254 and AN7260.

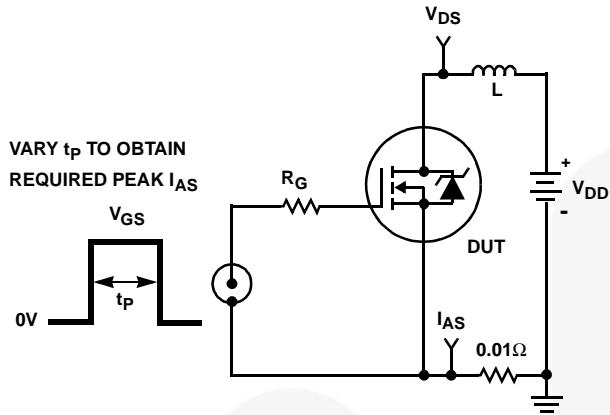**FIGURE 13. GATE CHARGE WAVEFORMS FOR CONSTANT GATE CURRENT**

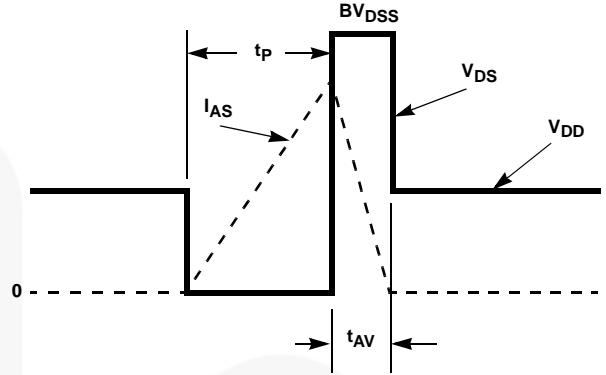## Test Circuits and Waveforms

FIGURE 14. UNCLAMPED ENERGY TEST CIRCUIT
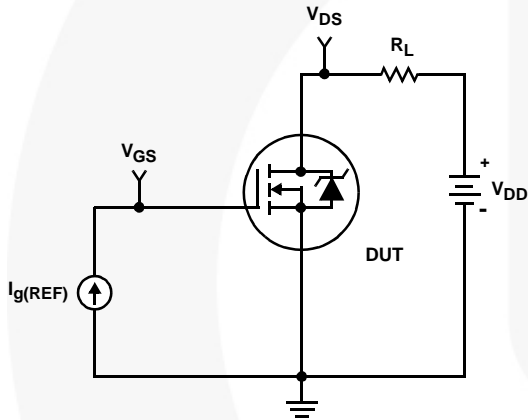
FIGURE 15. UNCLAMPED ENERGY WAVEFORMS
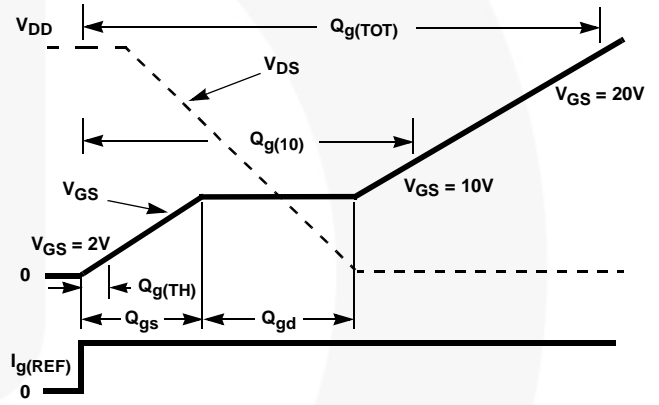
FIGURE 16. GATE CHARGE TEST CIRCUIT

FIGURE 17. GATE CHARGE WAVEFORMS

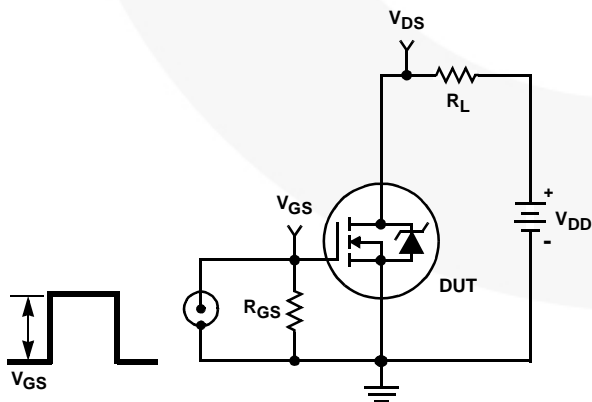**FIGURE 18. SWITCHING TIME TEST CIRCUIT**

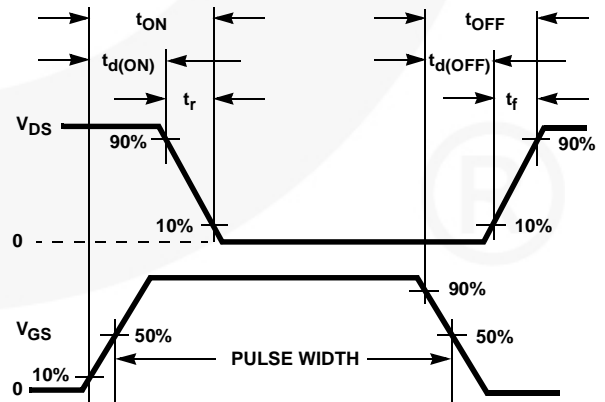**FIGURE 19. SWITCHING TIME WAVEFORM**

PSPICE Electrical Model

.SUBCKT HUF75542P3 2 1 3 ;   rev 15 Feb 2000

CA 12 8 4.4e-9
CB 15 14 4.2e-9
CIN 6 8 2.5e-9

DBODY 7 5 DBODYMOD
DBREAK 5 11 DBREAKMOD
DPLCAP 10 5 DPLCAPMOD

EBREAK 11 7 17 18 87.2
EDS 14 8 5 8 1
EGS 13 8 6 8 1
ESG 6 10 6 8 1
EVTHRES 6 21 19 8 1
EVTEMP 20 6 18 22 1

IT 8 17 1

LDRAIN 2 5 1.0e-9
LGATE 1 9 2.6e-9
LSOURCE 3 7 1.1e-9

MMED 16 6 8 8 MMEDMOD
MSTRO 16 6 8 8 MSTROMOD
MWEAK 16 21 8 8 MWEAKMOD

RBREAK 17 18 RBREAKMOD 1
RDRAIN 50 16 RDRAINMOD 5.5e-3
RGATE 9 20 1.0
RLDRAIN 2 5 10
RLGATE 1 9 26
RLSOURCE 3 7 11
RSLC1 5 51 RSLCMOD 1e-6
RSLC2 5 50 1e3
RSOURCE 8 7 RSOURCEMOD 3.3e-3
RVTHRES 22 8 RVTHRESMOD 1
RVTEMP 18 19 RVTEMPMOD 1

S1A 6 12 13 8 S1AMOD
S1B 13 12 13 8 S1BMOD
S2A 6 15 14 13 S2AMOD
S2B 13 15 14 13 S2BMOD

VBAT 22 19 DC 1

ESLC 51 50 VALUE={(V(5,51)/ABS(V(5,51)))*(PWR(V(5,51)/(1e-6*230),2.5))}

.MODEL DBODYMOD D (IS = 2.5e-12 RS = 2.85e-3 XTI = 5.5 TRS1 = 2e-3 TRS2 = 1e-6 CJO = 3.2e-9 TT = 5.5e-8 M = 0.6)
.MODEL DBREAKMOD D (RS = 2.9e- 1TRS1 = 1e- 3TRS2 = 1e-6)
.MODEL DPLCAPMOD D (CJO = 3.4e- 9IS = 1e-3 0M = 0.8 N = 10)
.MODEL MMEDMOD NMOS (VTO = 3.06 KP = 4.8 IS = 1e-30 N = 10 TOX = 1 L = 1u W = 1u RG = 1)
.MODEL MSTROMOD NMOS (VTO = 3.5 KP = 80 IS = 1e-30 N = 10 TOX = 1 L = 1u W = 1u)
.MODEL MWEAKMOD NMOS (VTO = 2.67 KP = 0.08 IS = 1e-30 N = 10 TOX = 1 L = 1u W = 1u RG = 10)
.MODEL RBREAKMOD RES (TC1 =1.3e- 3TC2 = -9e-7)
.MODEL RDRAINMOD RES (TC1 = 1.1e-2 TC2 = 2.5e-5)
.MODEL RSLCMOD RES (TC1 = 4.5e-3 TC2 = 1e-5)
.MODEL RSOURCEMOD RES (TC1 = 0 TC2 = 0)
.MODEL RVTHRESMOD RES (TC1 = -2.5e-3 TC2 = -1.1e-5)
.MODEL RVTEMPMOD RES (TC1 = -2.75e- 3TC2 = 0)

.MODEL S1AMOD VSWITCH (RON = 1e-5 ROFF = 0.1 VON = -6.0 VOFF= -4.5)
.MODEL S1BMOD VSWITCH (RON = 1e-5 ROFF = 0.1 VON = -4.5 VOFF= -6.0)
.MODEL S2AMOD VSWITCH (RON = 1e-5 ROFF = 0.1 VON = -0.5 VOFF= 0.5)
.MODEL S2BMOD VSWITCH (RON = 1e-5 ROFF = 0.1 VON = 0.5 VOFF= -0.5)

.ENDS

NOTE: For further discussion of the PSPICE model, consult **A New PSPICE Sub-Circuit for the Power MOSFET Featuring Global Temperature Options**; IEEE Power Electronics Specialist Conference Records, 1991, written by William J. Hepp and C. Frank Wheatley.
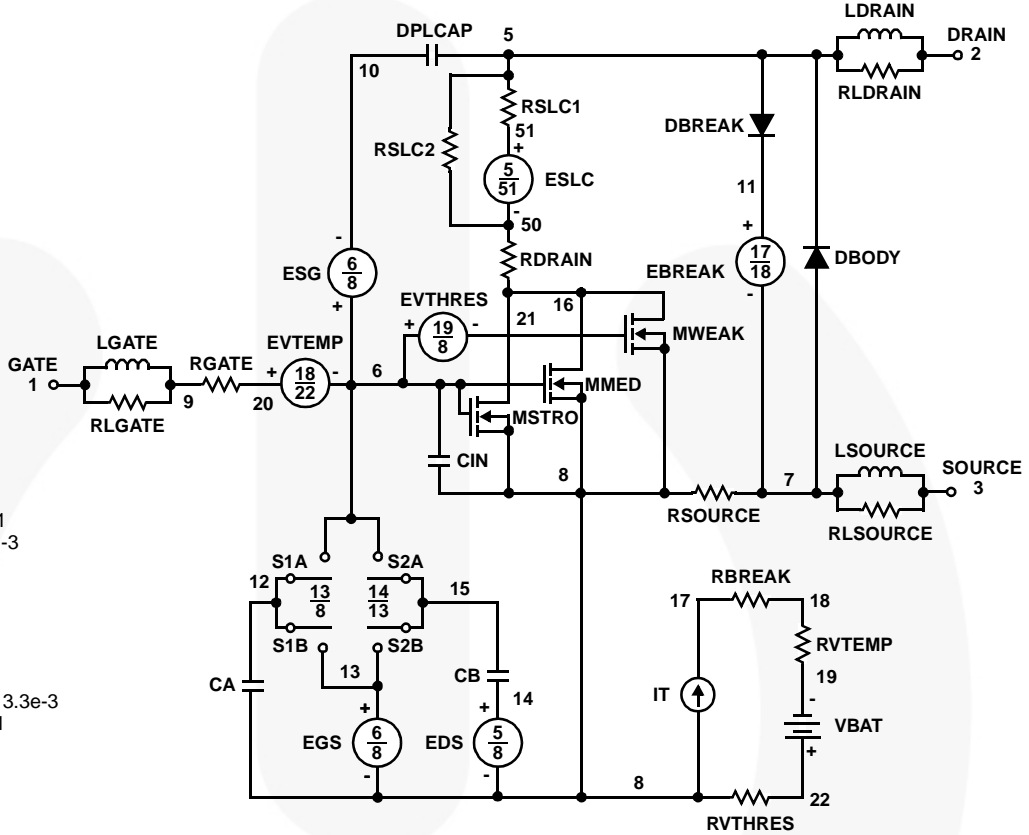
SABER Electrical Model

REV 15 Feb 00

```
template huf75542p3 n2,n1,n3
electrical n2,n1,n3
{
var i iscl
dp..model dbodymod =  (is = 2.5e-12, rs = 2.85e-3, xti = 5.5, trs1 = 2e-3, trs2 = 1e-6, cjo = 3.2e-9, tt = 5.5e-8, m = 0.6)
dp..model dbreakmod = (rs = 2.9e-1, trs1 = 1e-3, trs2 = 1e-6)
dp..model dplcapmod =  (cjo = 3.4e-9, is = 1e-30, m = 0.8, nl = 10)
m..model mmedmod = (type=_n, vto = 3.06, kp = 4.8, is = 1e-30, tox = 1)
m..model mstrongmod = (type=_n, vto = 3.5, kp = 80, is = 1e-30, tox = 1)
m..model mweakmod = (type=_n, vto = 2.67, kp = 0.08, is = 1e-30, tox = 1)
sw_vcsp..model s1amod =  (ron = 1e-5, roff = 0.1, von = -6.0, voff = -4.5)
sw_vcsp..model s1bmod =  (ron =1e-5, roff = 0.1, von = -4.5, voff = -6.0)
sw_vcsp..model s2amod =  (ron = 1e-5, roff = 0.1, von = -0.5, voff = 0.5)
sw_vcsp..model s2bmod =  (ron = 1e-5, roff = 0.1, von = 0.5, voff = -0.5)

c.ca n12 n8 = 4.4e-9
c.cb n15 n14 = 4.2e-9
c.cin n6 n8 = 2.5e-9
dp.dbody n7 n5 = model=dbodymod
dp.dbreak n5 n11 = model=dbreakmod
dp.dplcap n10 n5 = model=dplcapmod

i.it n8 n17 = 1

l.ldrain n2 n5 = 1e-9
l.lgate n1 n9 = 2.6e-9
l.lsource n3 n7 = 1.1e-9

m.mmed n16 n6 n8 n8 = model=mmedmod, l=1u, w=1u
m.mstrong n16 n6 n8 n8 = model=mstrongmod, l=1u, w=1u
m.mweak n16 n21 n8 n8 = model=mweakmod, l=1u, w=1u

res.rbreak n17 n18  = 1, tc1 = 1.3e-3, tc2 = -9e-7
res.rdrain n50 n16  = 5.5e-3, tc1 = 1.1e-2, tc2 = 2.5e-5
res.rgate n9 n20 = 1.0
res.rldrain n2 n5 = 10
res.rlgate n1 n9 = 26
res.rlsource n3 n7 = 11
res.rslc1 n5 n51 = 1e-6, tc1 = 4.5e-3, tc2 = 1e-5
res.rslc2 n5 n50 = 1e3
res.rsource n8 n7  = 3.3e-3, tc1 = 0, tc2 = 0
res.rvtemp n18 n19  = 1, tc1 = -2.75e-3, tc2 = 0
res.rvthres n22 n8  = 1, tc1 = -2.5e-3, tc2 = -1.1e-5

spe.ebreak n11 n7 n17 n18 = 87.2
spe.eds n14 n8 n5 n8 = 1
spe.egs n13 n8 n6 n8 = 1
spe.esg n6 n10 n6 n8 = 1
spe.evtemp n20 n6 n18 n22 = 1
spe.evthres n6 n21 n19 n8 = 1

sw_vcsp.s1a n6 n12 n13 n8 = model=s1amod
sw_vcsp.s1b n13 n12 n13 n8 = model=s1bmod
sw_vcsp.s2a n6 n15 n14 n13 = model=s2amod
sw_vcsp.s2b n13 n15 n14 n13 = model=s2bmod

v.vbat n22 n19 = dc=1

equations {
i (n51->n50) +=iscl
iscl: v(n51,n50) = ((v(n5,n51)/(1e-9+abs(v(n5,n51))))*((abs(v(n5,n51)*1e6/230))** 2.5))
}
}
```
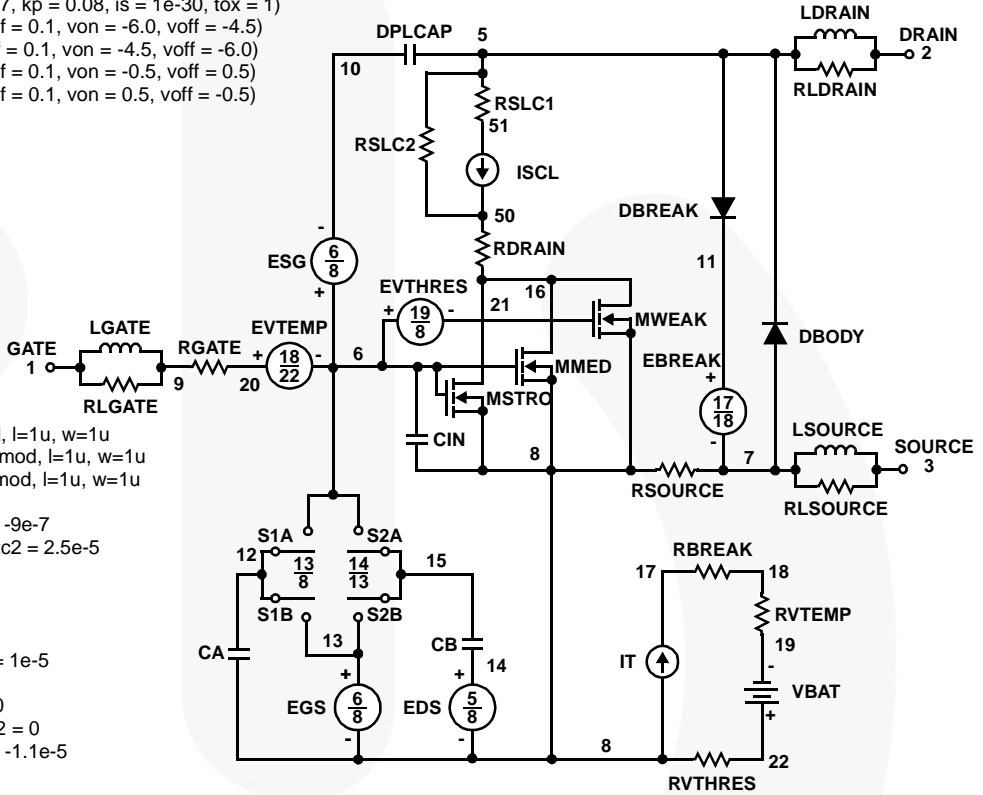
SPICE Thermal Model

REV 15 Feb 00

T75542

CTHERM1 th 6 4.1e-3
CTHERM2 6 5 5.5e-3
CTHERM3 5 4 8.6e-3
CTHERM4 4 3 1.5e-2
CTHERM5 3 2 1.6e-2
CTHERM6 2 tl 6.5e-2

RTHERM1 th 6 2.0e-4
RTHERM2 6 5 3.5e-3
RTHERM3 5 4 2.5e-2
RTHERM4 4 3 9.0e-2
RTHERM5 3 2 1.6e-1
RTHERM6 2 tl 2.3e-1

SABER Thermal Model

SABER thermal model t75542

template thermal_model th tl
thermal_c th, tl
{
ctherm.ctherm1 th 6 = 4.1e-3
ctherm.ctherm2 6 5 = 5.5e-3
ctherm.ctherm3 5 4 = 8.6e-3
ctherm.ctherm4 4 3 = 1.5e-2
ctherm.ctherm5 3 2 = 1.6e-2
ctherm.ctherm6 2 tl = 6.5e-2

rtherm.rtherm1 th 6 = 2.0e-4
rtherm.rtherm2 6 5 = 3.5e-3
rtherm.rtherm3 5 4 = 2.5e-2
rtherm.rtherm4 4 3 = 9.0e-2
rtherm.rtherm5 3 2 = 1.6e-1
rtherm.rtherm6 2 tl = 2.3e-1
}

FAIRCHILD
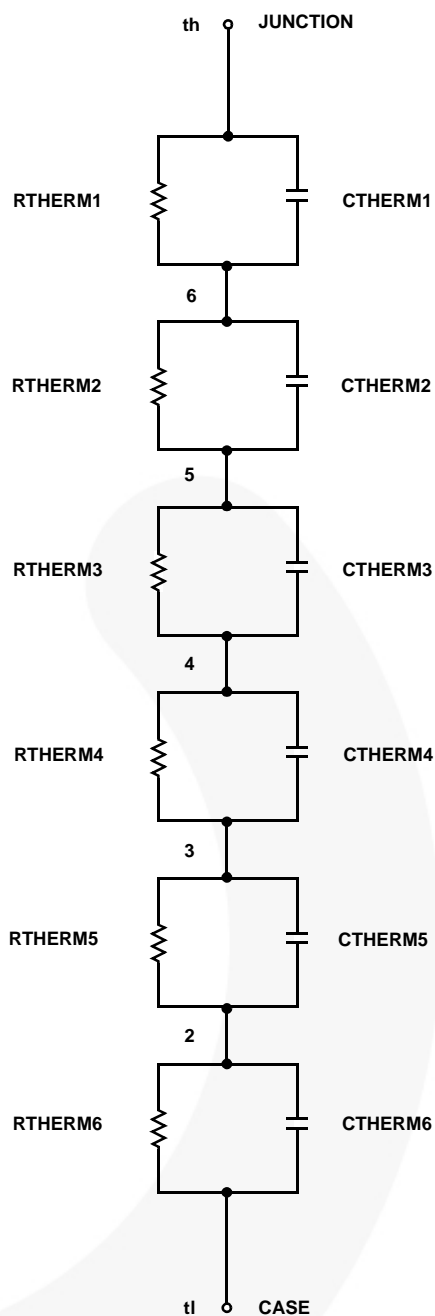
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CorePOWER™	Green FPS™ e-Series™	QFET®	TinyCalc™
CROSSVOLT™	G*max*™	QS™	TinyLogic®
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Current Transfer Logic™	IntelliMAX™	RapidConfigure™	TinyPower™
DEUXPEED®	ISOPLANAR™	™	TinyPWM™
Dual Cool™	Marking Small Speakers Sound Louder		TinyWire™
EcoSPARK®	and Better™	Saving our world, 1mW/W/kW at a time™	TranSiC™
EfficentMax™	MegaBuck™	SignalWise™	TriFault Detect™
ESBC™	MICROCOUPLER™	SmartMax™	TRUECURRENT®*
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®	MicroPak™	Solutions for Your Success™	
Fairchild®	MicroPak2™	SPM®	μ SerDes™
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FACT®	mWSaver®	SuperSOT™-3	UniFET™
FAST®	OptoHiT™	SuperSOT™-6	VCX™
FastvCore™	OPTOLOGIC®	SuperSOT™-8	VisualMax™
FETBench™	OPTOPLANAR®	SupreMOS®	VoltagePlus™
FPS™		SyncFET™	XS™

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As used here in:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body or (b) support or sustain life, and (c) whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury of the user.

2. A critical component in any component of a life support, device, or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

ANTI-COUNTERFEITING POLICY

Fairchild Semiconductor Corporation's Anti-Counterfeiting Policy. Fairchild's Anti-Counterfeiting Policy is also stated on our external website, www.Fairchildsemi.com, under Sales Support.

Counterfeiting of semiconductor parts is a growing problem in the industry. All manufactures of semiconductor products are experiencing counterfeiting of their parts. Customers who inadvertently purchase counterfeit parts experience many problems such as loss of brand reputation, substandard performance, failed application, and increased cost of production and manufacturing delays. Fairchild is taking strong measures to protect ourselves and our customers from the proliferation of counterfeit parts. Fairchild strongly encourages customers to purchase Fairchild parts either directly from Fairchild or from Authorized Fairchild Distributors who are listed by country on our web page cited above. Products customers buy either from Fairchild directly or from Authorized Fairchild Distributors are genuine parts, have full traceability, meet Fairchild's quality standards for handing and storage and provide access to Fairchild's full range of up-to-date technical and product information. Fairchild and our Authorized Distributors will stand behind all warranties and will appropriately address and warranty issues that may arise. Fairchild will not provide any warranty coverage or other assistance for parts bought from Unauthorized Sources. Fairchild is committed to combat this global problem and encourage our customers to do their part in stopping this practice by buying direct or from authorized distributors.

PRODUCT STATUS DEFINITIONS
Definition of Terms

Datasheet Identification	Product Status	Definition
Advance Information	Formative / In Design	Datasheet contains the design specifications for product development. Specifications may change in any manner without notice.
Preliminary	First Production	Datasheet contains preliminary data; supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve design.
No Identification Needed	Full Production	Datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve the design.
Obsolete	Not In Production	Datasheet contains specifications on a product that is discontinued by Fairchild Semiconductor. The datasheet is for reference information only.

Rev. I66

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