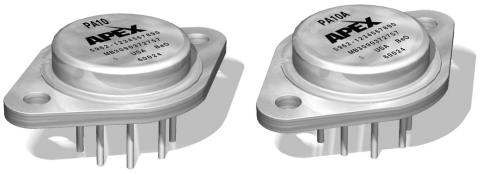
PA10 • PA10A

Power Operational Amplifier

RoHS COMPLIANT



FEATURES

- Gain Bandwidth Product — 4 MHz
- Temperature Range — –55 to +125°C (PA10A)
- Excellent Linearity — Class A/B Output
- Wide Supply Range — ±10V to ±50V
- High Output Current — ±5A Peak

APPLICATIONS

- Motor, Valve and Actuator Control
- Magnetic Deflection Circuits up to 4A
- Power Transducers up to 100 kHz
- Temperature Control up to 180W
- Programmable Power Supplies up to 90V
- Audio Amplifiers up to 60W RMS

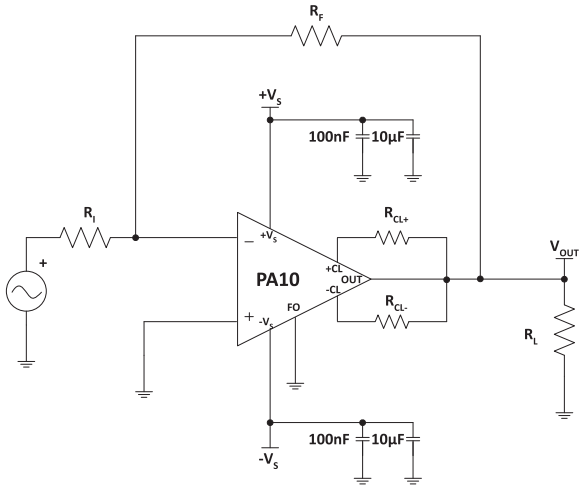
DESCRIPTION

The PA10 and PA10A are high voltage, high output current operational amplifiers designed to drive resistive, inductive and capacitive loads. For optimum linearity, the output stage is biased for class A/B operation. The safe operating area (SOA) can be observed for all operating conditions by selection of user programmable current limiting resistors. Both amplifiers are internally compensated for all gain settings. For continuous operation under load, a heatsink of proper rating is recommended.

This hybrid integrated circuit utilizes thick film (cermet) resistors, ceramic capacitors and semiconductor chips to maximize reliability, minimize size and give top performance. Ultrasonically bonded aluminum wires provide reliable interconnections at all operating temperatures. The 8-pin TO-3 package is hermetically sealed and electrically isolated. The use of compressible isolation washers voids the warranty.

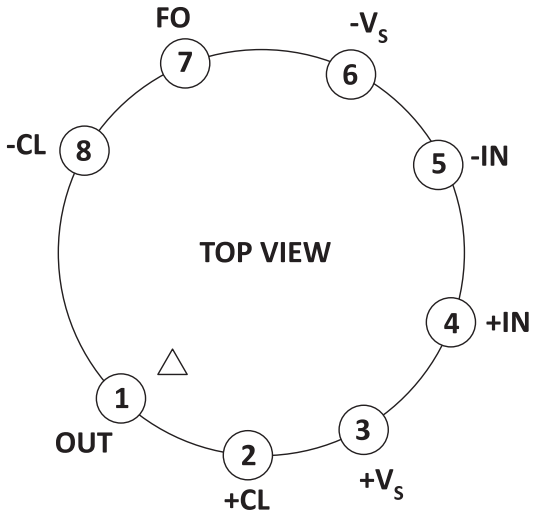
TYPICAL CONNECTION

Figure 1: Typical Connection



PINOUT AND DESCRIPTION TABLE

Figure 2: External Connections



Pin Number	Name	Description
1	OUT	The output. Connect this pin to load and to the feedback resistors.
2	+CL	Connect to the sourcing current limit resistor, and then the OUT pin. Output current flows out of this pin through R_{CL+}.
3	+Vs	The positive supply rail.
4	+IN	The non-inverting input.
5	-IN	The inverting input.
6	-Vs	The negative supply rail.
7	FO	The foldover current limit. Connect to ground if desired. See “Current Limiting” section.
8	-CL	Connect to the sinking current limit resistor, and then the OUT pin. Output current flows into this pin through R_{CL-}.

SPECIFICATIONS

The power supply voltage for all tests is ±40, unless otherwise noted as a test condition. Full temperature range specifications are guaranteed but not tested.

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Min	Max	Units
Supply Voltage, total	$+V_S$ to $-V_S$		100	V
Output Current, within SOA	I_O		5	A
Power Dissipation, internal	P_D		67	W
Input Voltage, differential	$V_{IN\ (Diff)}$		±37	V
Input Voltage, common mode	V_{cm}		$\pm V_S$	V_S
Temperature, pin solder, 10s max.			350	°C
Temperature, junction [1]	T_J		200	°C
Temperature Range, storage		-65	+150	°C
Operating Temperature Range, case	T_C	-55	+125	°C

1. Long term operation at the maximum junction temperature will result in reduced product life. Derate internal power dissipation to achieve high MTTF.

CAUTION The internal substrate contains beryllia (BeO). Do not break the seal. If accidentally broken, do not crush, machine, or subject to temperatures in excess of 850°C to avoid generating toxic fumes.

INPUT

Parameter	Test Conditions	PA10			PA10A			Units
		Min	Typ	Max	Min	Typ	Max	
Offset Voltage, initial	T_C = 25°C		±2	±6		±1	±4	mV
Offset Voltage vs. temperature	Full temp range		±10	±65		*	±40	µV/°C
Offset Voltage vs. supply	T_C = 25°C		±30	±200		*	*	µV/V
Offset Voltage vs. power	T_C = 25°C		±20			*		µV/W
Bias Current, initial	T_C = 25°C		12	30		10	20	nA
Bias Current vs. temperature	Full temp range		±50	±500		*	*	pA/°C
Bias Current vs. supply	T_C = 25°C		±0.10			*		pA/V
Offset Current, initial	T_C = 25°C		±12	±30		±5	±10	nA
Offset Current vs. temperature	Full temp range		±50			*		pA/°C
Input Impedance, DC	T_C = 25°C		200			*		MΩ
Input Capacitance	T_C = 25°C		3			*		pF
Common Mode Voltage Range [1]	Full temp range	$\pm V_S$–5	$\pm V_S$–3		*	*		V
Common Mode Rejection, DC [1]	Full temp range, $V_{CM} = \pm V_S$ –6V	74	100		*	*		dB

1. $+V_S$ and $–V_S$ denote the positive and negative supply rail respectively. Total V_S is measured from $+V_S$ to $–V_S$.

GAIN

Parameter	Test Conditions	PA10			PA10A			Units
		Min	Typ	Max	Min	Typ	Max	
Open Loop Gain @ 10 Hz	T_C = 25°C, 1 kΩ load		110			*		dB
Open Loop Gain @ 10 Hz	Full temp range, 15 Ω load	96	108		*	*		dB
Gain Bandwidth Product @ 1 MHz	T_C = 25°C, 15 Ω load		4			*		MHz
Power Bandwidth	T_C = 25°C, 15 Ω load	10	15		*	*		kHz
Phase Margin	Full temp range, 15 Ω load		35			*		°

OUTPUT

Parameter	Test Conditions	PA10			PA10A			Units
		Min	Typ	Max	Min	Typ	Max	
Voltage Swing [1]	T_C=25°C, I_O=5A	$\pm V_S - 8$	$\pm V_S - 5$		$\pm V_S - 6$	*		V
Voltage Swing [1]	Full temp range, I_O = 2A	$\pm V_S - 6$			*			V
Voltage Swing [1]	Full temp range, I_O = 80mA	$\pm V_S - 5$			*			V
Current, peak	T_C = 25°C	5			*			A
Settling Time to 0.1%	T_C=25°C, 2V step		2			*		µs
Slew Rate	T_C = 25°C	2	3		*	*		V/µs
Capacitive Load	Full temp range, A_V = 1			0.68			*	nF
Capacitive Load	Full temp range, A_V = 2.5			10			*	nF
Capacitive Load	Full temp range, A_V > 10			SOA			*	

1. $+V_S$ and $-V_S$ denote the positive and negative supply rail respectively. Total V_S is measured from $+V_S$ to $-V_S$.

POWER SUPPLY

Parameter	Test Conditions	PA10			PA10A			Units
		Min	Typ	Max	Min	Typ	Max	
Voltage	Full temp range	±10	±40	±45	*	*	±50	V
Current, quiescent	T_C = 25°C	8	15	30	*	*	*	mA

THERMAL

Parameter	Test Conditions	PA10			PA10A			Units
		Min	Typ	Max	Min	Typ	Max	
Resistance, AC, junction to case [1]	T_C=-55 to 125°C, F > 60 Hz		1.9	2.1		*	*	°C/W
Resistance, DC, junction to case	T_C = -55 to 125°C		2.4	2.6		*	*	°C/W
Resistance, junction to air	T_C= -55 to 125°C		30			*		°C/W
Temperature Range, case	Meets full range specs	-25		+85	-55		+125	°C

1. Rating applies if the output current alternates between both output transistors at a rate faster than 60 Hz.

Note: *The specification of PA10A is identical to the specification for PA10 in applicable column to the left.

TYPICAL PERFORMANCE GRAPHS

Figure 3: Power Derating

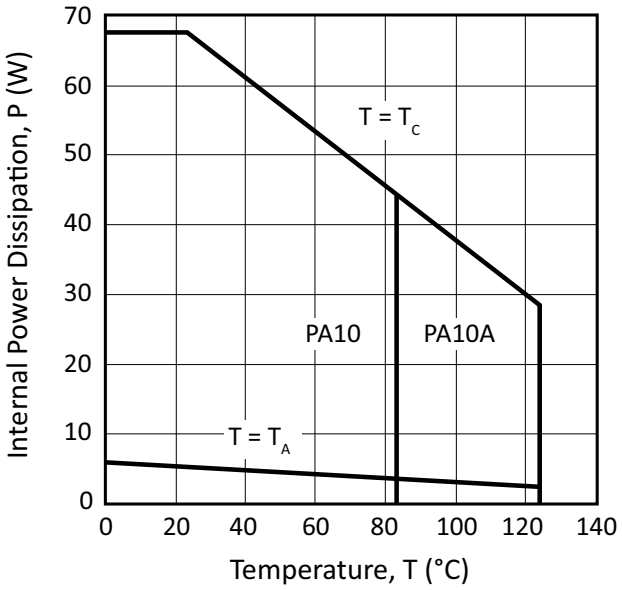


Figure 4: Bias Current

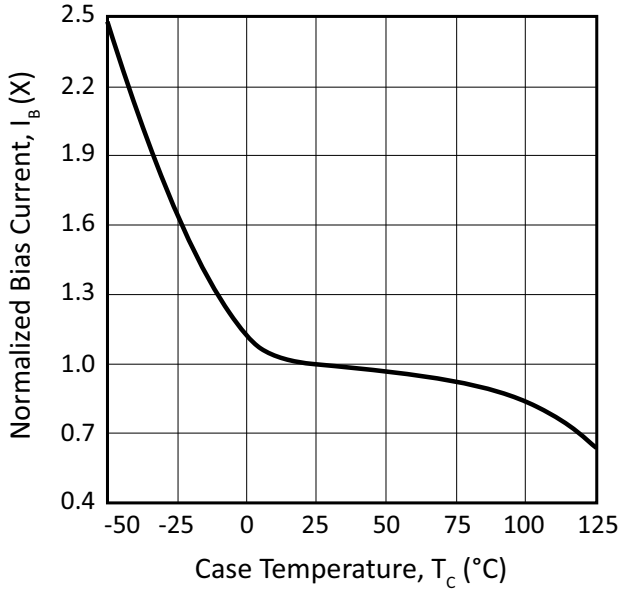


Figure 5: Small Signal Response

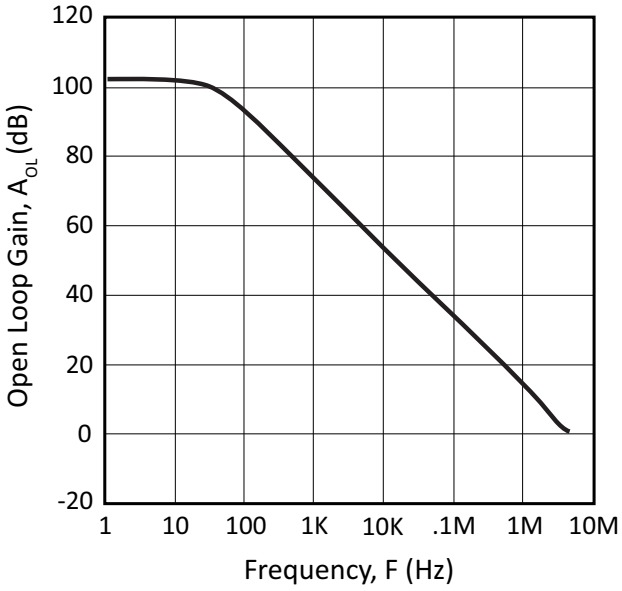


Figure 6: Phase Response

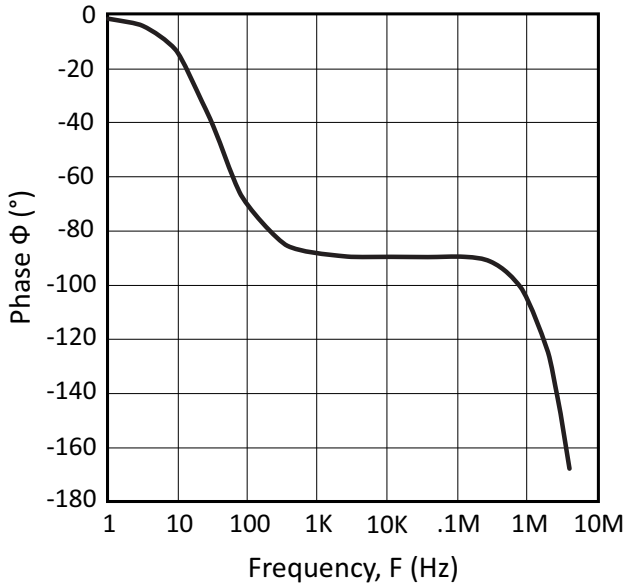


Figure 7: Current Limit

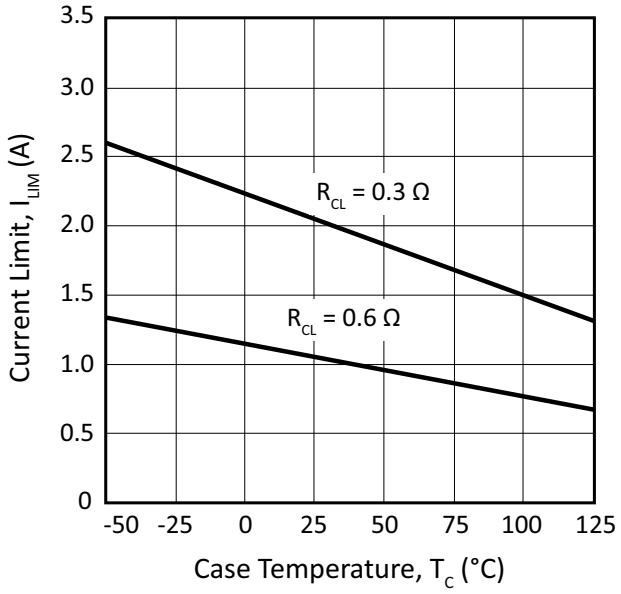


Figure 8: Power Response

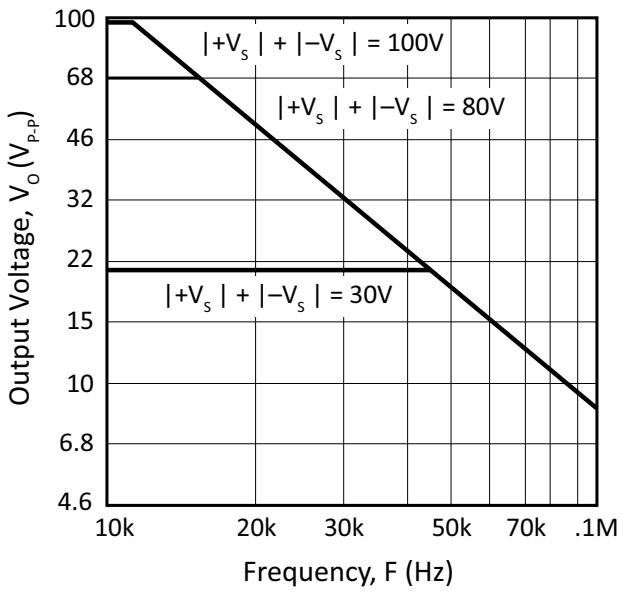


Figure 9: Common Mode Rejection

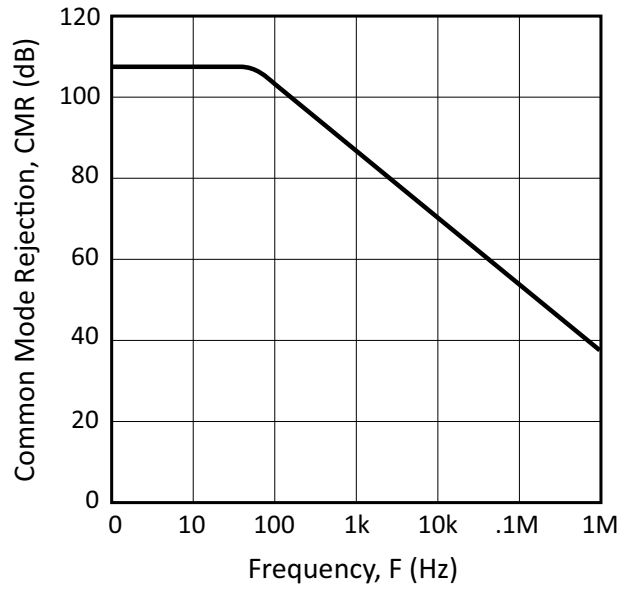


Figure 10: Pulse Response

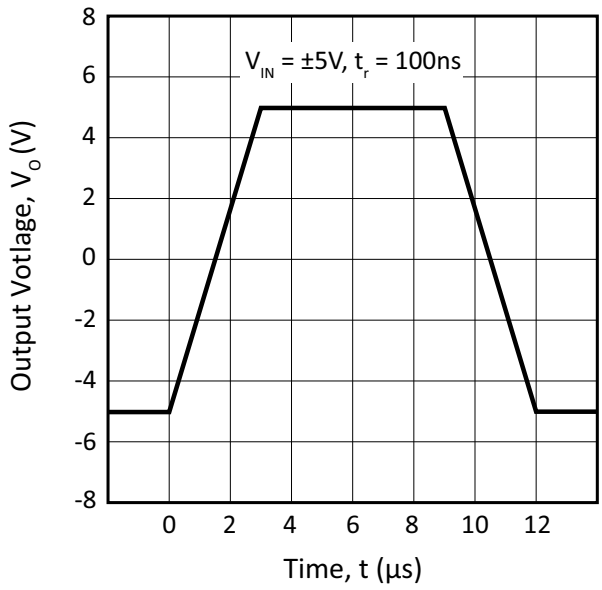


Figure 11: Input Noise

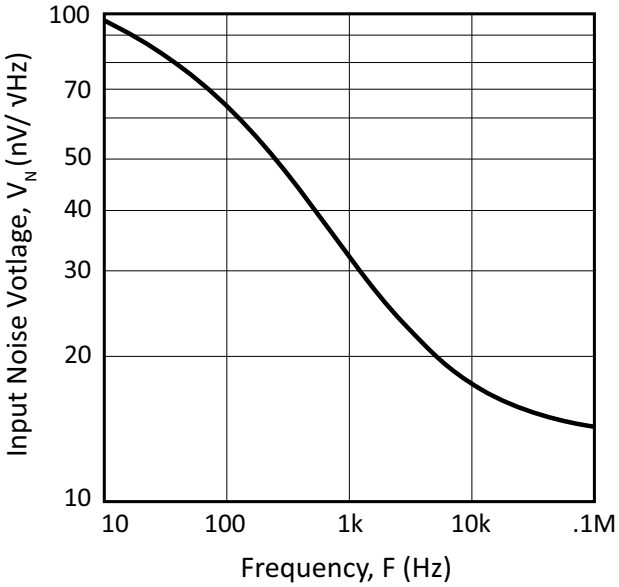


Figure 12: Harmonic Distortion

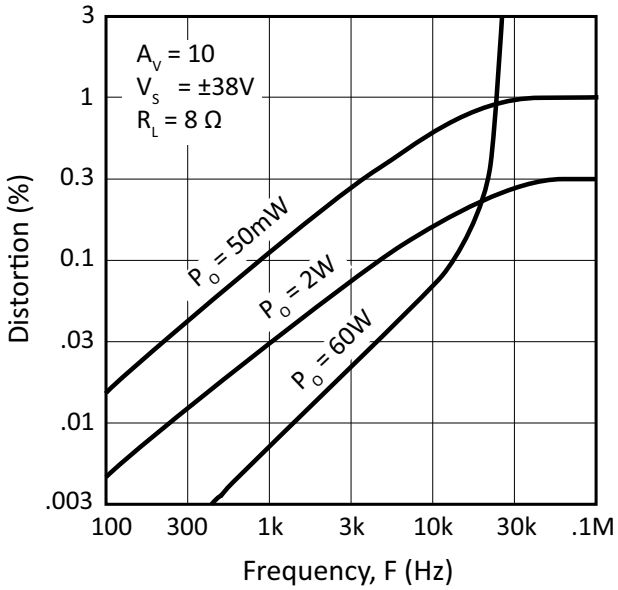


Figure 13: Quiescent Current

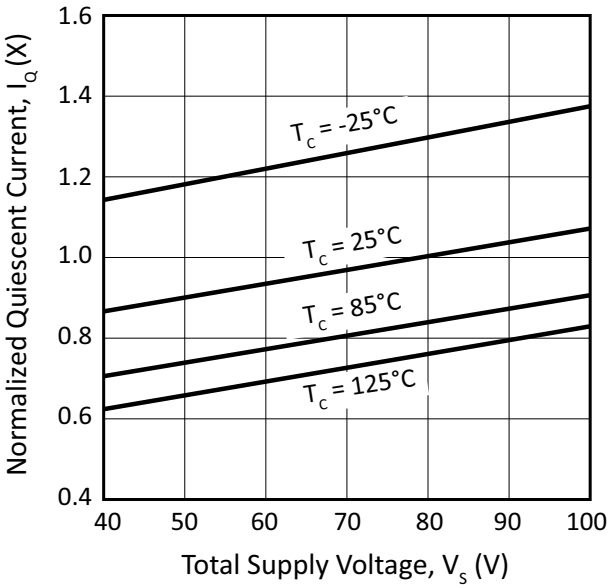
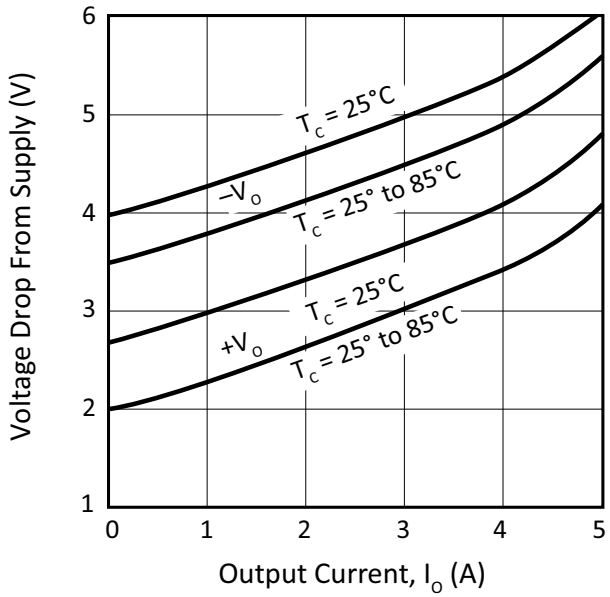


Figure 14: Output Voltage Swing



SAFE OPERATING AREA (SOA)

The output stage of most power amplifiers has three distinct limitations:

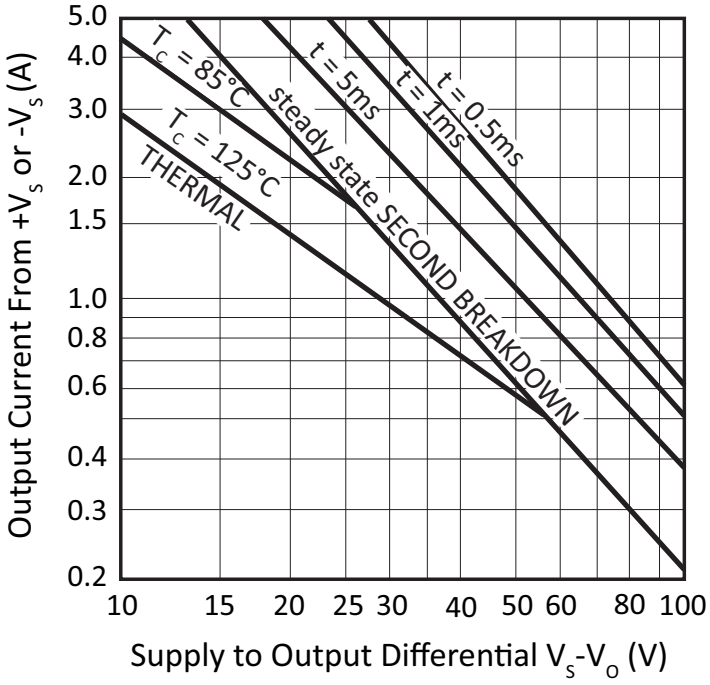
1. The current handling capability of the transistor geometry and the wire bonds.
2. The second breakdown effect which occurs whenever the simultaneous collector current and collector-emitter voltage exceeds specified limits.
3. The junction temperature of the output transistors.

The SOA curves combine the effect of these limits. For a given application, the direction and magnitude of the output current should be calculated or measured and checked against the SOA curves. This is simple for resistive loads but more complex for reactive and EMF generating loads.

1. For DC outputs, especially those resulting from fault conditions, check worst case stress levels against the SOA graph.
   Make sure the load line does not cross the 0.5ms limit and that excursions beyond any other second breakdown line do not exceed the time label, and have a duty cycle of no more than 10%.
   A Spice type analysis can be very useful in that a hardware setup often calls for instruments or amplifiers with wide common mode rejection ranges. Please refer to Application Notes, AN01 and AN22 for detailed information regarding SOA considerations.
2. The amplifier can handle any EMF generating or reactive load and short circuits to the supply rail or shorts to common if the current limits are set as follows at T_C = 85°C:

$\pm V_S$	Short to $\pm V_S$ C, L, or EMF Load	Short to Common
50V	0.21A	0.61A
40V	0.3A	0.87A
35V	0.36A	1.0A
30V	0.46A	1.4A
25V	0.61A	1.7A
20V	0.87A	2.2A
15V	1.4A	2.9A

Figure 15: SOA



GENERAL

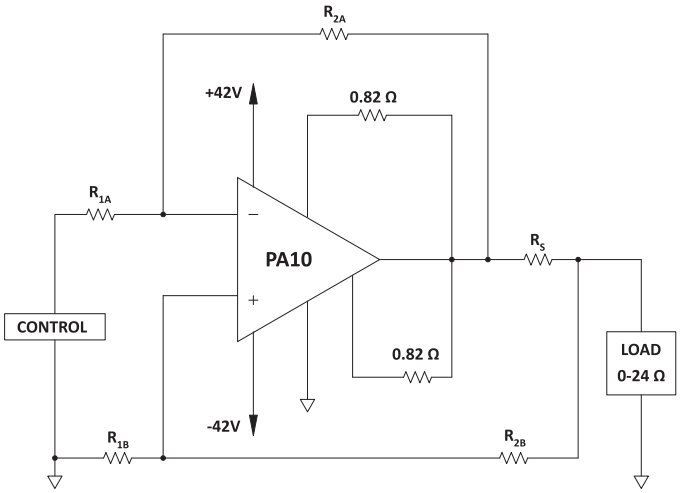
Please read Application Note 1 “General Operating Considerations” which covers stability, supplies, heat sinking, mounting, current limit, SOA interpretation, and specification interpretation. Visit www.apexanalog.com for Apex Microtechnology’s complete Application Notes library, Technical Seminar Workbook, and Evaluation Kits.

TYPICAL APPLICATION

DC and low distortion AC current waveforms are delivered to a grounded load by using matched resistors (A and B sections) and taking advantage of the high common mode rejection of the PA10.

Foldover current limit is used to modify current limits based on output voltage. When load resistance drops to 0, the current is limited based on output voltage. When load resistance drops to 0, the current limit is 0.79A resulting in an internal dissipation of 33.3 W. When output voltage increases to 36V, the current limit is 1.69A. Refer to Application Note 9 on foldover limiting for details.

Figure 16: Typical Application (Voltage-to-Current Conversion)



CURRENT LIMITING

Refer to Application Note 9, “Current Limiting”, for details of both fixed and foldover current limit operation. Beware that current limit should be thought of as a +/–20% function initially and varies about 2:1 over the range of –55°C to 125°C.

For fixed current limit, leave pin 7 open and use equations 1 and 2.

1.

$$R_{CL}(\Omega) = \frac{0.65V}{I_{CL}(A)}$$

2.

$$I_{CL}(A) = \frac{0.65V}{R_{CL}(\Omega)}$$

Where:

I_{CL} is the current limit in amperes.

R_{CL} is the current limit resistor in ohms.

For certain applications, foldover current limit adds a slope to the current limit which allows more power to be delivered to the load without violating the SOA. For maximum foldover slope, ground pin 7 and use equations 3 and 4.

3.

$$I_{CL}(A) = \frac{0.65V + (Vo \cdot 0.014)}{R_{CL}(\Omega)}$$

4.

$$R_{CL}(\Omega) = \frac{0.65V + (Vo \cdot 0.014)}{I_{CL}(A)}$$

Where:

Vo is the output voltage in volts.

Most designers start with either equation 1 to set R_{CL} for the desired current at 0v out, or with equation 4 to set R_{CL} at the maximum output voltage. Equation 3 should then be used to plot the resulting foldover limits on the SOA graph. If equation 3 results in a negative current limit, foldover slope must be reduced. This can happen when the output voltage is the opposite polarity of the supply conducting the current.

In applications where a reduced foldover slope is desired, this can be achieved by adding a resistor (R_{FO}) between pin 7 and ground. Use equations 4 and 5 with this new resistor in the circuit.

5.

$$I_{CL}(A) = \frac{0.65V + \frac{Vo \cdot 0.14}{10.14 + R_{FO}}}{R_{CL}(\Omega)}$$

6.

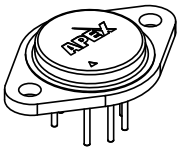
$$R_{CL}(\Omega) = \frac{0.65V + \frac{Vo \cdot 0.14}{10.14 + R_{FO}}}{I_{CL}(A)}$$

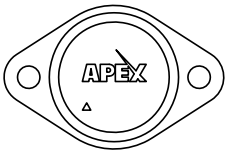
Where:

R_{FO} is in K ohms.

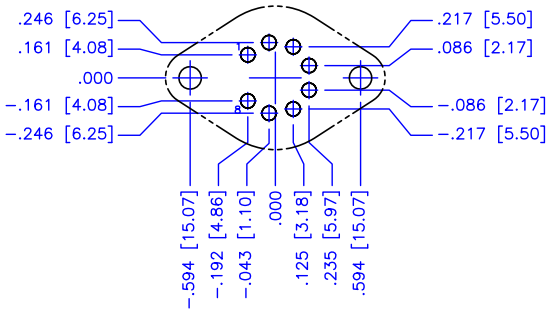
PACKAGE OPTIONS

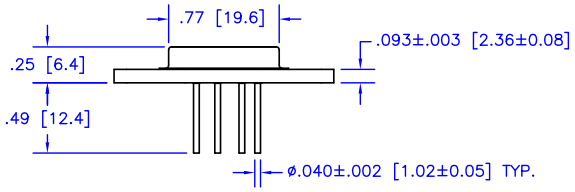
PACKAGE STYLE CE

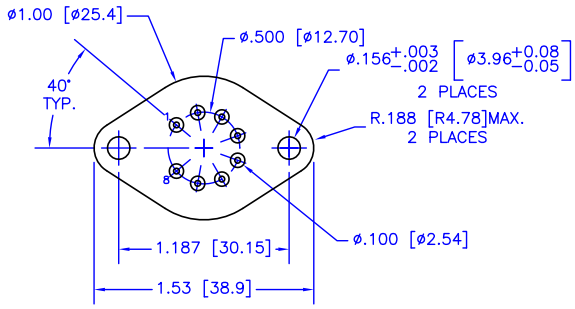




Ordinate dimensions for CAD layout







NOTES:

1. Dimensions are inches & [mm].
2. Triangle printed on lid denotes pin 1.
3. Header flatness within pin circle is .0005" TIR, max.
4. Header flatness between mounting holes is .0015" TIR, max.
5. Standard pin material: Solderable nickel–plated Alloy 52.
6. Header material: Nickel–plated cold–rolled steel.
7. Welded hermetic package seal
8. Isolation: 500 VDC any pin to case.
9. Package weight: .53 oz [15 g]

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