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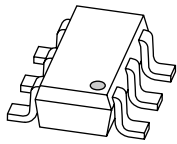
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Kind regards,

Team Nexperia



PBSS305ND

100 V, 3 A NPN low V_{CEsat} (BISS) transistor

Rev. 02 — 7 December 2007

Product data sheet

1. Product profile

1.1 General description

NPN low V_{CEsat} Breakthrough In Small Signal (BISS) transistor in a SOT457 (SC-74) small Surface-Mounted Device (SMD) plastic package.

PNP complement: PBSS305PD.

1.2 Features

- Low collector-emitter saturation voltage V_{CEsat}
- High collector current capability I_C and I_{CM}
- High collector current gain (h_{FE}) at high I_C
- High efficiency due to less heat generation
- Smaller required Printed-Circuit Board (PCB) area than for conventional transistors

1.3 Applications

- High-voltage DC-to-DC conversion
- High-voltage MOSFET gate driving
- High-voltage motor control
- High-voltage power switches (e.g. motors, fans)
- Thin Film Transistor (TFT) backlight inverter
- Automotive applications

1.4 Quick reference data

Table 1. Quick reference data

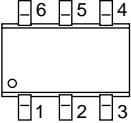
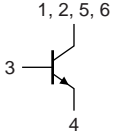
| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|-------------|--|----------------------------------|-----|-----|-----|------------|
| V_{CEO} | collector-emitter voltage | open base | - | - | 100 | V |
| I_C | collector current | | [1] | - | 3 | A |
| I_{CM} | peak collector current | single pulse; $t_p \leq 1$ ms | - | - | 4 | A |
| R_{CEsat} | collector-emitter saturation resistance | $I_C = 2$ A; $I_B = 200$ mA | [2] | 73 | 95 | m Ω |

[1] Device mounted on a ceramic PCB, Al_2O_3 , standard footprint.

[2] Pulse test: $t_p \leq 300$ μ s; $\delta \leq 0.02$.

2. Pinning information

Table 2. Pinning

| Pin | Description | Simplified outline | Symbol |
|-----|-------------|---|---|
| 1 | collector |  |  |
| 2 | collector | | |
| 3 | base | | |
| 4 | emitter | | |
| 5 | collector | | |
| 6 | collector | | |

3. Ordering information

Table 3. Ordering information

| Type number | Package | | |
|-------------|---------|--|---------|
| | Name | Description | Version |
| PBSS305ND | SC-74 | plastic surface-mounted package (TSOP6); 6 leads | SOT457 |

4. Marking

Table 4. Marking codes

| Type number | Marking code |
|-------------|--------------|
| PBSS305ND | AG |

5. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

| Symbol | Parameter | Conditions | Min | Max | Unit |
|-----------|---------------------------|----------------------------------|----------|------|------|
| V_{CBO} | collector-base voltage | open emitter | - | 100 | V |
| V_{CEO} | collector-emitter voltage | open base | - | 100 | V |
| V_{EBO} | emitter-base voltage | open collector | - | 5 | V |
| I_C | collector current | | [1] - | 1 | A |
| | | | [2] - | 3 | A |
| I_{CM} | peak collector current | single pulse; $t_p \leq 1$ ms | - | 4 | A |
| I_B | base current | | - | 0.8 | A |
| I_{BM} | peak base current | single pulse; $t_p \leq 1$ ms | - | 2 | A |
| P_{tot} | total power dissipation | $T_{amb} \leq 25$ °C | [1] - | 360 | mW |
| | | | [3] - | 600 | mW |
| | | | [4] - | 750 | mW |
| | | | [2] - | 1.1 | W |
| | | | [1][5] - | 2.5 | W |
| T_j | junction temperature | | - | 150 | °C |
| T_{amb} | ambient temperature | | -65 | +150 | °C |
| T_{stg} | storage temperature | | -65 | +150 | °C |

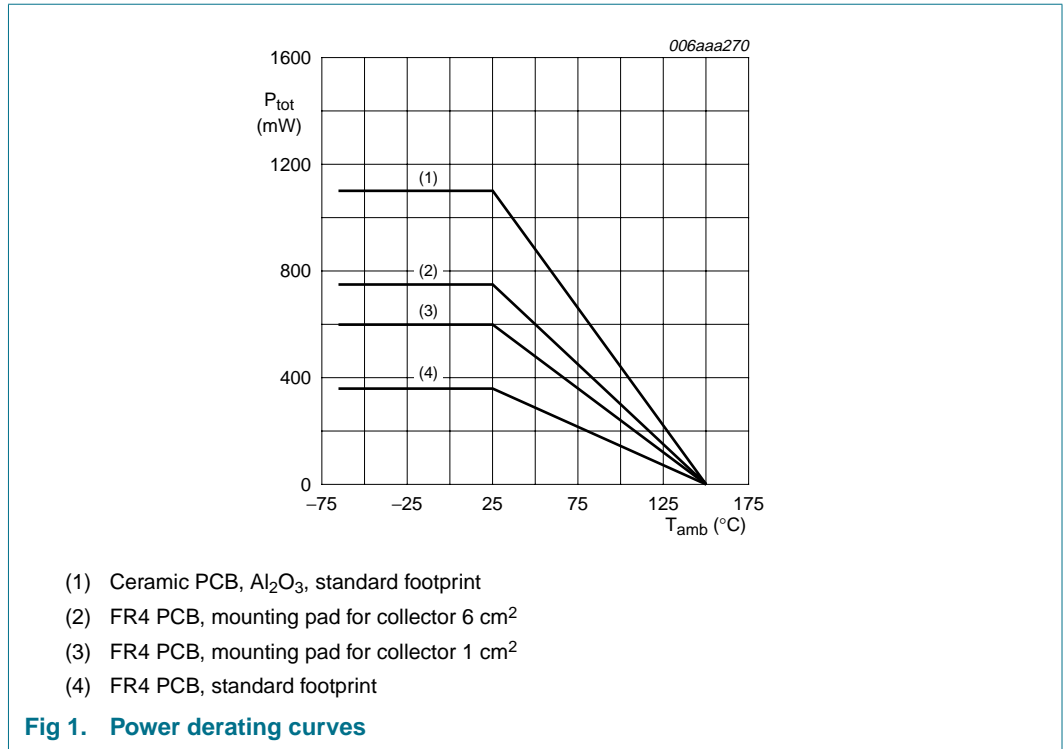
[1] Device mounted on an FR4 PCB, single-sided copper, tin-plated and standard footprint.

[2] Device mounted on a ceramic PCB, Al_2O_3 , standard footprint.

[3] Device mounted on an FR4 PCB, single-sided copper, tin-plated, mounting pad for collector 1 cm².

[4] Device mounted on an FR4 PCB, single-sided copper, tin-plated, mounting pad for collector 6 cm².

[5] Pulse test: $t_p \leq 10$ ms; $\delta \leq 10$ %.

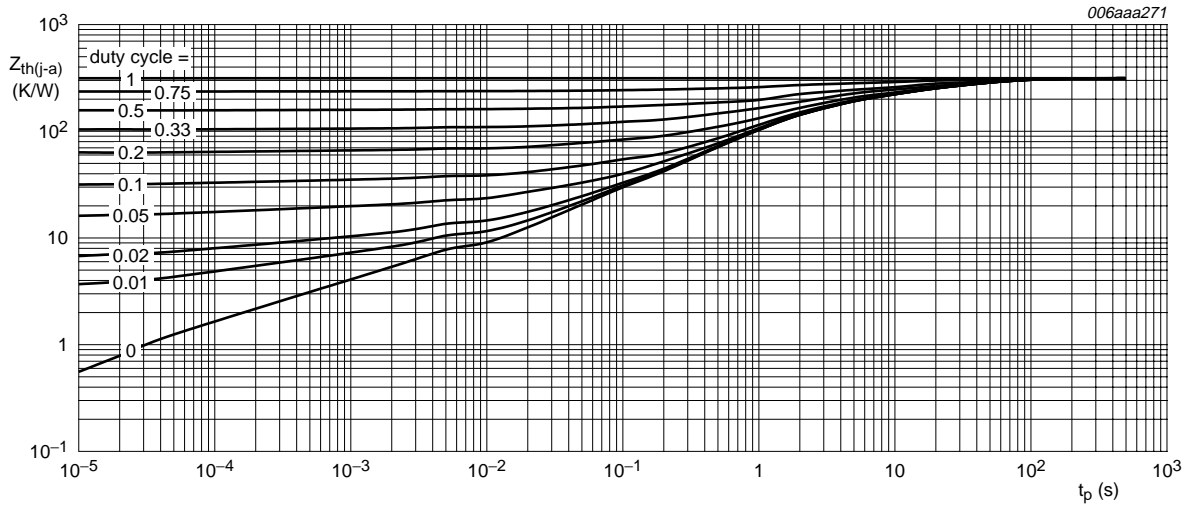


6. Thermal characteristics

Table 6. Thermal characteristics

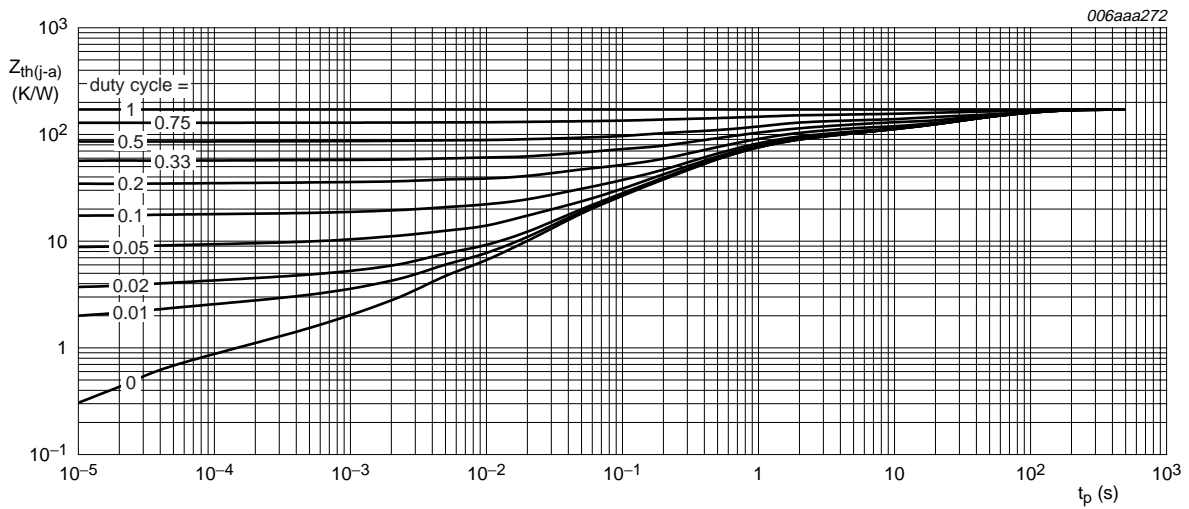
| Symbol | Parameter | Conditions | Min | Typ | Max | Unit | |
|-----------------------|--|-------------|--------|-----|-----|------|-----|
| R _{th(j-a)} | thermal resistance from junction to ambient | in free air | [1] | - | - | 350 | K/W |
| | | | [2] | - | - | 208 | K/W |
| | | | [3] | - | - | 167 | K/W |
| | | | [4] | - | - | 113 | K/W |
| | | | [1][5] | - | - | 50 | K/W |
| R _{th(j-sp)} | thermal resistance from junction to solder point | | - | - | 45 | K/W | |

- [1] Device mounted on an FR4 PCB, single-sided copper, tin-plated and standard footprint.
- [2] Device mounted on an FR4 PCB, single-sided copper, tin-plated, mounting pad for collector 1 cm².
- [3] Device mounted on an FR4 PCB, single-sided copper, tin-plated, mounting pad for collector 6 cm².
- [4] Device mounted on a ceramic PCB, Al₂O₃, standard footprint.
- [5] Pulse test: t_p ≤ 10 ms; δ ≤ 10 %.



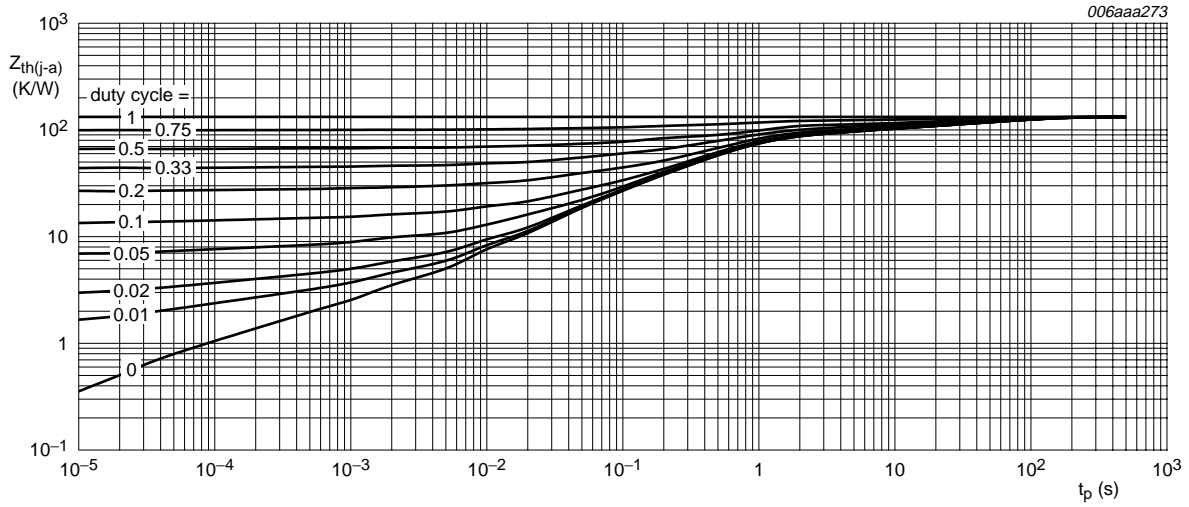
FR4 PCB, standard footprint

Fig 2. Transient thermal impedance from junction to ambient as a function of pulse duration; typical values



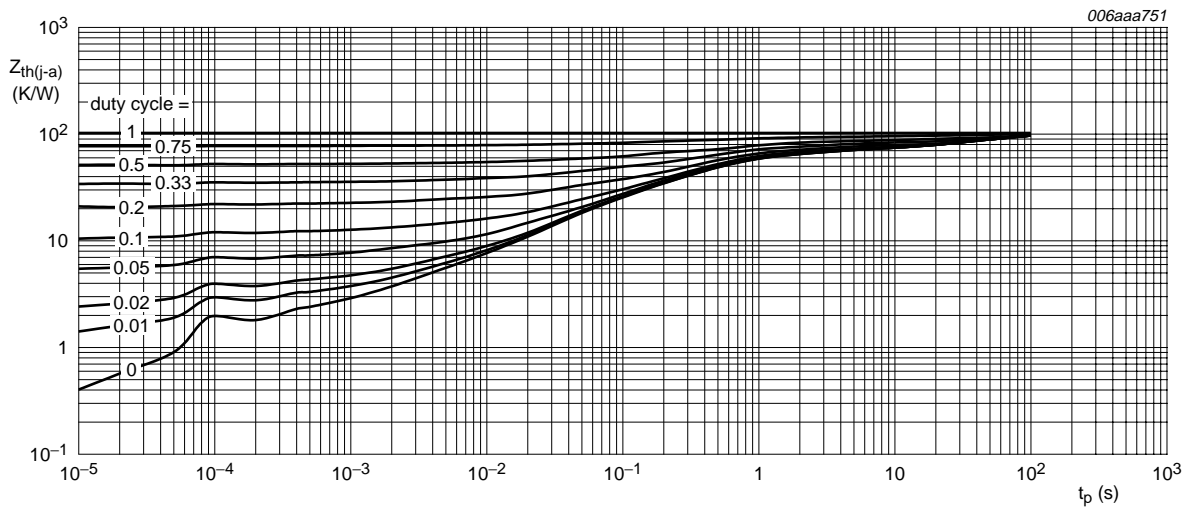
FR4 PCB, mounting pad for collector 1 cm²

Fig 3. Transient thermal impedance from junction to ambient as a function of pulse duration; typical values



FR4 PCB, mounting pad for collector 6 cm²

Fig 4. Transient thermal impedance from junction to ambient as a function of pulse duration; typical values



Ceramic PCB, Al₂O₃, standard footprint

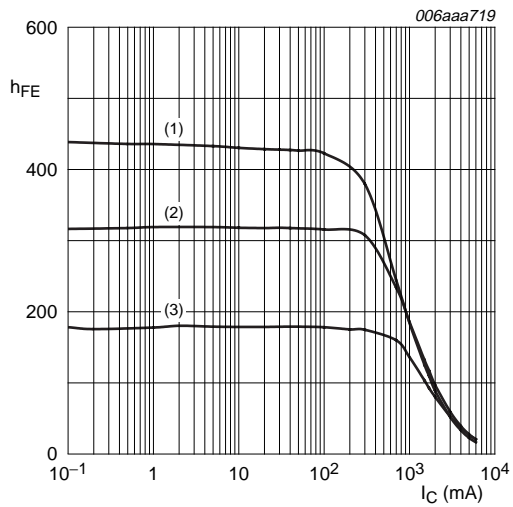
Fig 5. Transient thermal impedance from junction to ambient as a function of pulse duration; typical values

7. Characteristics

Table 7. Characteristics
 $T_{amb} = 25\text{ }^{\circ}\text{C}$ unless otherwise specified.

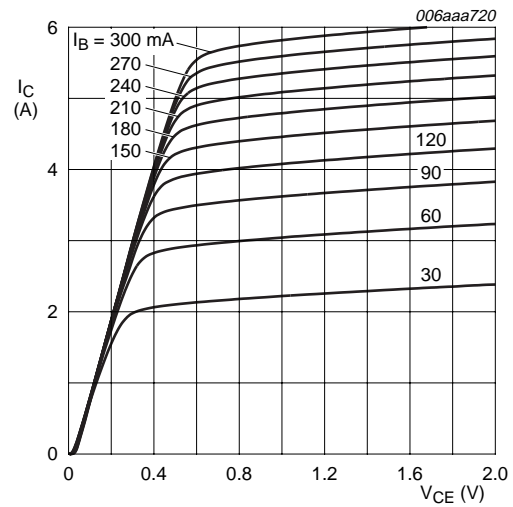
| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|-------------|---|---|---------|------|------|------------------|
| I_{CBO} | collector-base cut-off current | $V_{CB} = 100\text{ V}; I_E = 0\text{ A}$ | - | - | 100 | nA |
| | | $V_{CB} = 100\text{ V}; I_E = 0\text{ A}; T_j = 150\text{ }^{\circ}\text{C}$ | - | - | 50 | μA |
| I_{CES} | collector-emitter cut-off current | $V_{CE} = 80\text{ V}; V_{BE} = 0\text{ V}$ | - | - | 100 | nA |
| I_{EBO} | emitter-base cut-off current | $V_{EB} = 5\text{ V}; I_C = 0\text{ A}$ | - | - | 100 | nA |
| h_{FE} | DC current gain | $V_{CE} = 2\text{ V}; I_C = 0.5\text{ A}$ | 170 | 275 | - | |
| | | $V_{CE} = 2\text{ V}; I_C = 1\text{ A}$ | [1] 125 | 185 | - | |
| | | $V_{CE} = 2\text{ V}; I_C = 2\text{ A}$ | [1] 70 | 95 | - | |
| | | $V_{CE} = 2\text{ V}; I_C = 3\text{ A}$ | [1] 40 | 55 | - | |
| | | $V_{CE} = 2\text{ V}; I_C = 4\text{ A}$ | [1] 25 | 40 | - | |
| V_{CEsat} | collector-emitter saturation voltage | $I_C = 0.5\text{ A}; I_B = 50\text{ mA}$ | - | 45 | 60 | mV |
| | | $I_C = 1\text{ A}; I_B = 50\text{ mA}$ | - | 90 | 120 | mV |
| | | $I_C = 2\text{ A}; I_B = 200\text{ mA}$ | [1] - | 145 | 190 | mV |
| | | $I_C = 3\text{ A}; I_B = 150\text{ mA}$ | [1] - | 240 | 310 | mV |
| | | $I_C = 3\text{ A}; I_B = 300\text{ mA}$ | [1] - | 215 | 280 | mV |
| | | $I_C = 4\text{ A}; I_B = 400\text{ mA}$ | [1] - | 280 | 360 | mV |
| R_{CEsat} | collector-emitter saturation resistance | $I_C = 2\text{ A}; I_B = 200\text{ mA}$ | [1] - | 73 | 95 | $\text{m}\Omega$ |
| V_{BEsat} | base-emitter saturation voltage | $I_C = 0.5\text{ A}; I_B = 50\text{ mA}$ | - | 0.79 | 0.87 | V |
| | | $I_C = 1\text{ A}; I_B = 50\text{ mA}$ | - | 0.81 | 0.89 | V |
| | | $I_C = 1\text{ A}; I_B = 100\text{ mA}$ | [1] - | 0.83 | 0.92 | V |
| | | $I_C = 3\text{ A}; I_B = 150\text{ mA}$ | [1] - | 0.93 | 0.99 | V |
| | | $I_C = 3\text{ A}; I_B = 300\text{ mA}$ | [1] - | 0.95 | 1.02 | V |
| V_{BEon} | base-emitter turn-on voltage | $V_{CE} = 2\text{ V}; I_C = 2\text{ A}$ | - | 0.83 | 1 | V |
| t_d | delay time | $V_{CC} = 9.2\text{ V}; I_C = 2\text{ A}; I_{Bon} = 0.1\text{ A}; I_{Boff} = -0.1\text{ A}$ | - | 14 | - | ns |
| t_r | rise time | | - | 341 | - | ns |
| t_{on} | turn-on time | | - | 355 | - | ns |
| t_s | storage time | | - | 246 | - | ns |
| t_f | fall time | | - | 343 | - | ns |
| t_{off} | turn-off time | | - | 589 | - | ns |
| f_T | transition frequency | $V_{CE} = 10\text{ V}; I_C = 100\text{ mA}; f = 100\text{ MHz}$ | - | 140 | - | MHz |
| C_C | collector capacitance | $V_{CB} = 10\text{ V}; I_E = I_e = 0\text{ A}; f = 1\text{ MHz}$ | - | 16 | - | pF |

[1] Pulse test: $t_p \leq 300\text{ }\mu\text{s}; \delta \leq 0.02$.



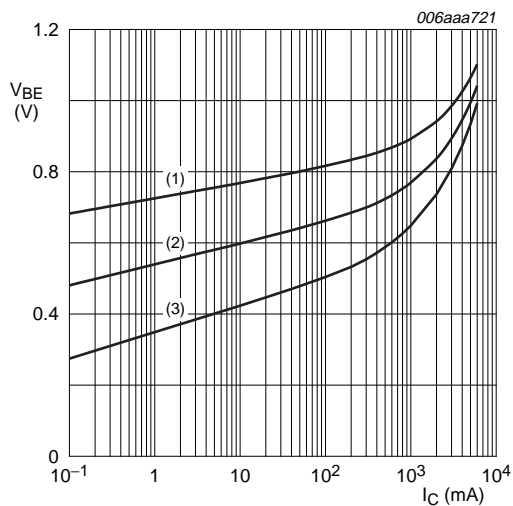
$V_{CE} = 2\text{ V}$
 (1) $T_{amb} = 100\text{ °C}$
 (2) $T_{amb} = 25\text{ °C}$
 (3) $T_{amb} = -55\text{ °C}$

Fig 6. DC current gain as a function of collector current; typical values



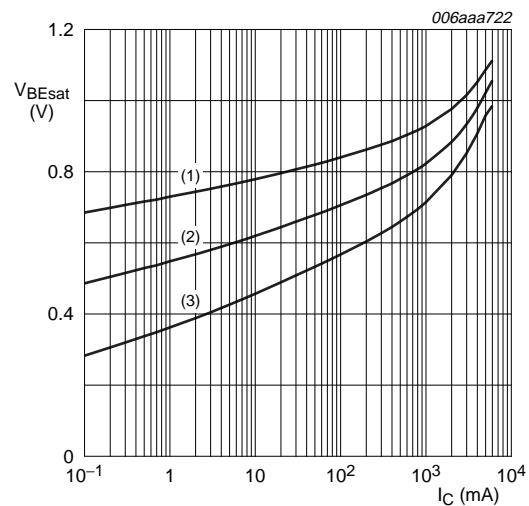
$T_{amb} = 25\text{ °C}$

Fig 7. Collector current as a function of collector-emitter voltage; typical values



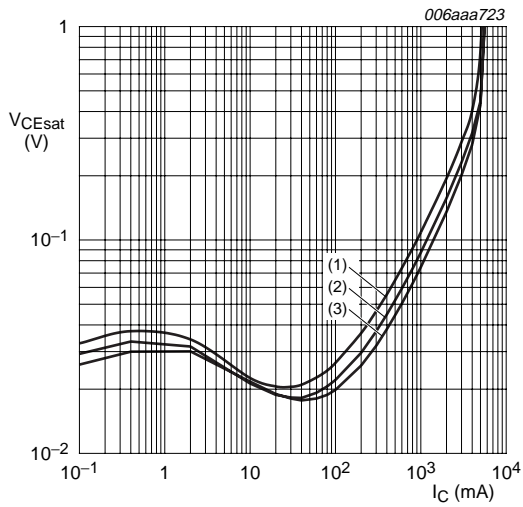
$V_{CE} = 2\text{ V}$
 (1) $T_{amb} = -55\text{ °C}$
 (2) $T_{amb} = 25\text{ °C}$
 (3) $T_{amb} = 100\text{ °C}$

Fig 8. Base-emitter voltage as a function of collector current; typical values



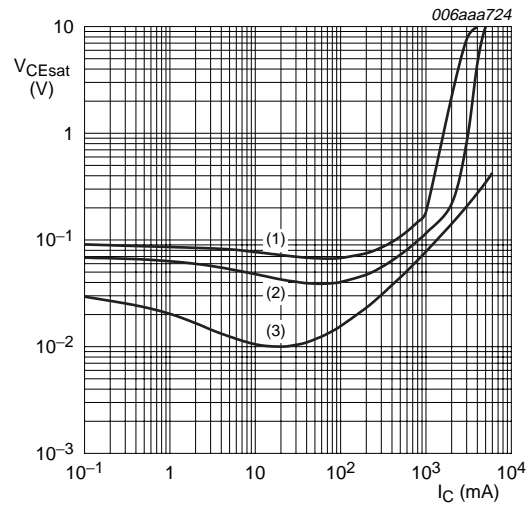
$I_C/I_B = 20$
 (1) $T_{amb} = -55\text{ °C}$
 (2) $T_{amb} = 25\text{ °C}$
 (3) $T_{amb} = 100\text{ °C}$

Fig 9. Base-emitter saturation voltage as a function of collector current; typical values



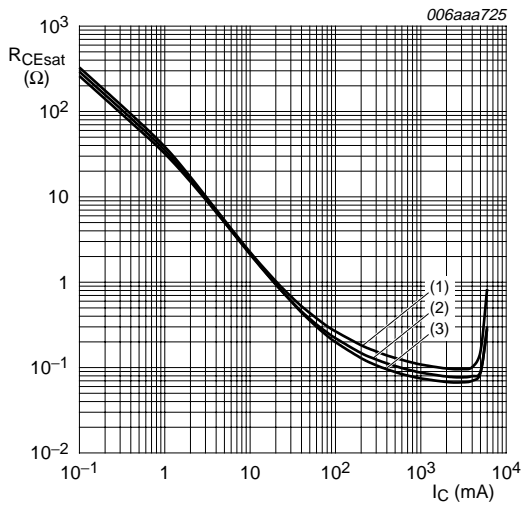
$I_C/I_B = 20$
 (1) $T_{amb} = 100\text{ °C}$
 (2) $T_{amb} = 25\text{ °C}$
 (3) $T_{amb} = -55\text{ °C}$

Fig 10. Collector-emitter saturation voltage as a function of collector current; typical values



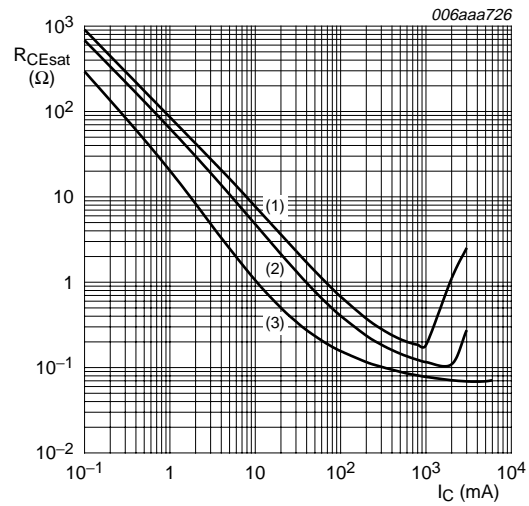
$T_{amb} = 25\text{ °C}$
 (1) $I_C/I_B = 100$
 (2) $I_C/I_B = 50$
 (3) $I_C/I_B = 10$

Fig 11. Collector-emitter saturation voltage as a function of collector current; typical values



$I_C/I_B = 20$
 (1) $T_{amb} = 100\text{ °C}$
 (2) $T_{amb} = 25\text{ °C}$
 (3) $T_{amb} = -55\text{ °C}$

Fig 12. Collector-emitter saturation resistance as a function of collector current; typical values



$T_{amb} = 25\text{ °C}$
 (1) $I_C/I_B = 100$
 (2) $I_C/I_B = 50$
 (3) $I_C/I_B = 10$

Fig 13. Collector-emitter saturation resistance as a function of collector current; typical values

8. Test information

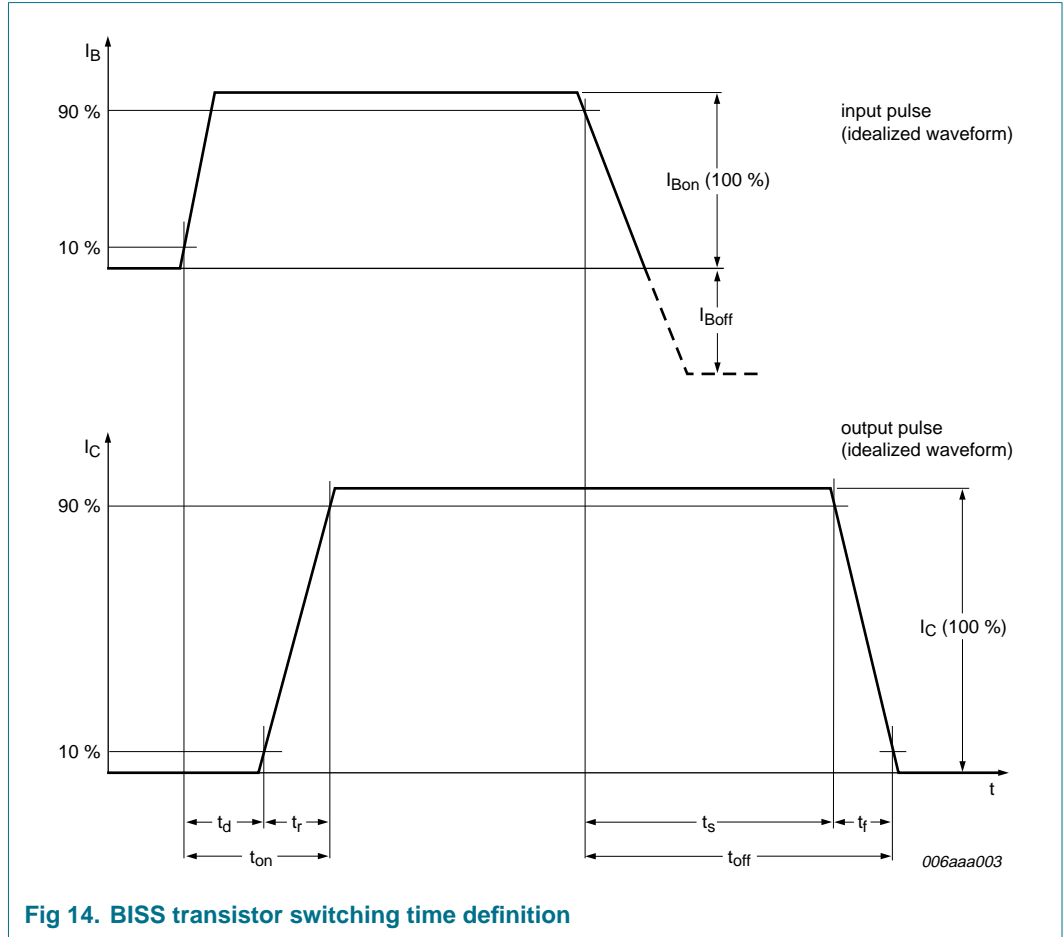


Fig 14. BISS transistor switching time definition

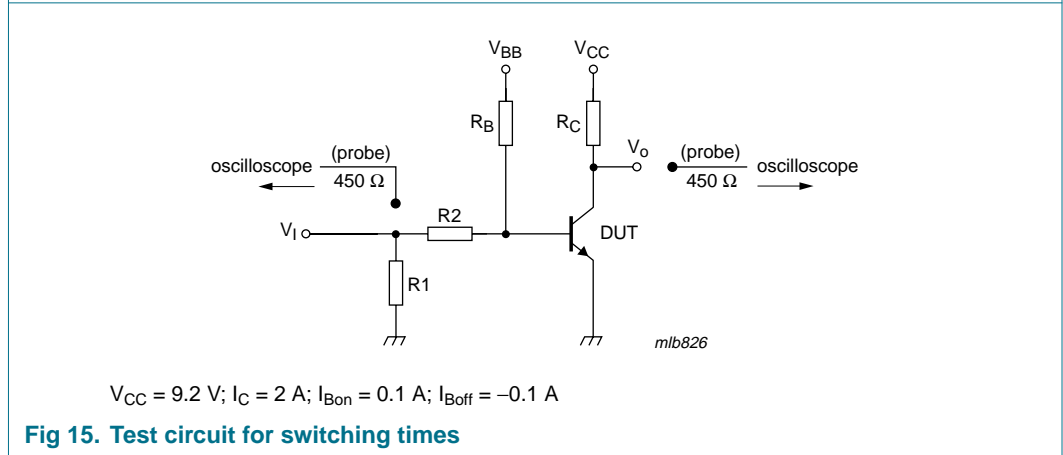
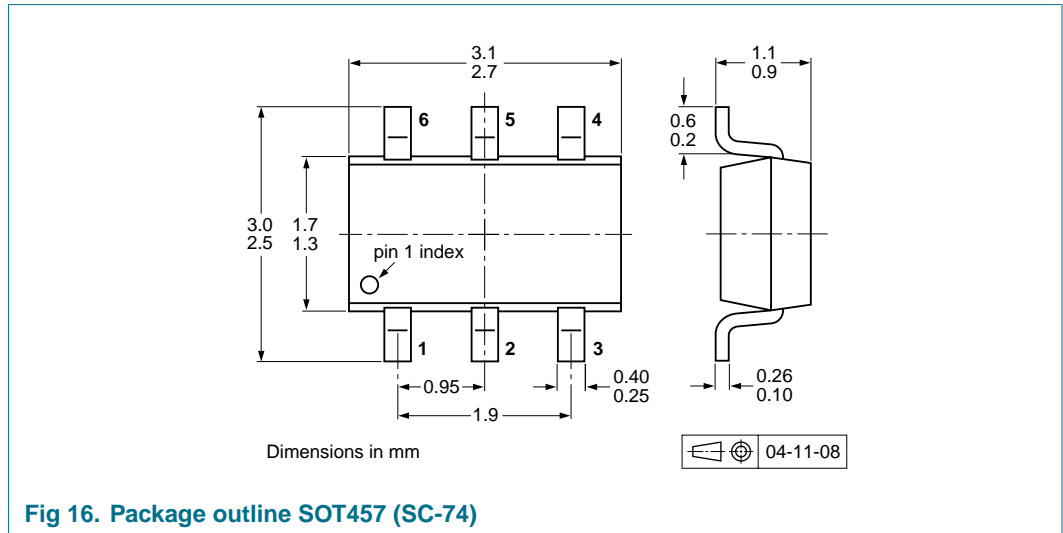


Fig 15. Test circuit for switching times

9. Package outline



10. Packing information

Table 8. Packing methods

The indicated -xxx are the last three digits of the 12NC ordering code.^[1]

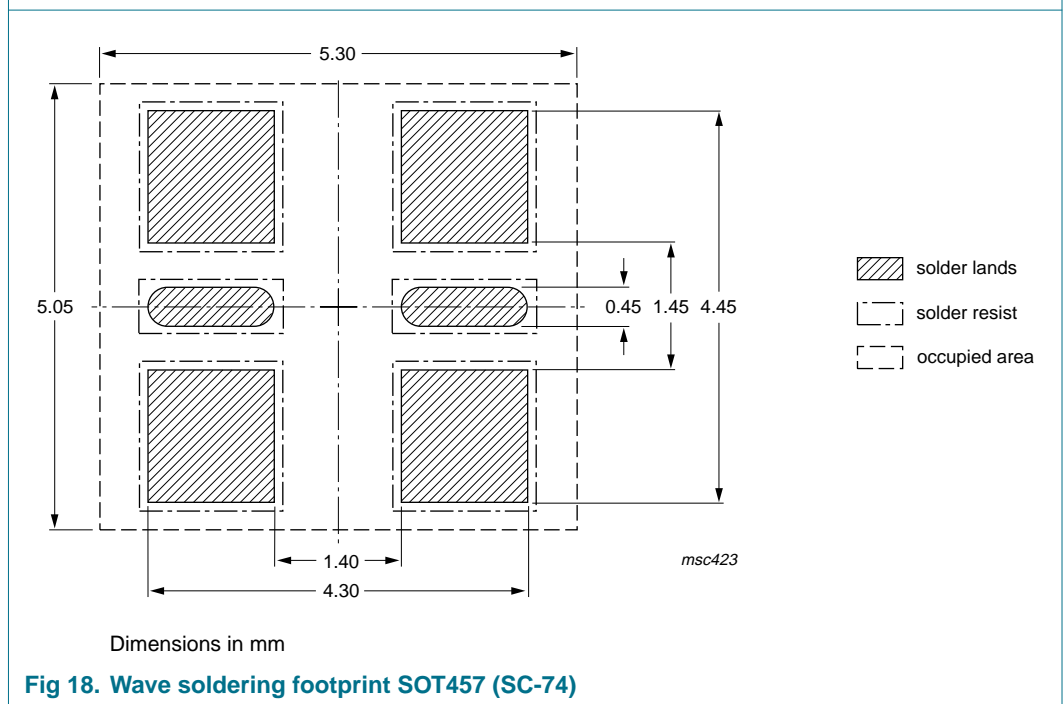
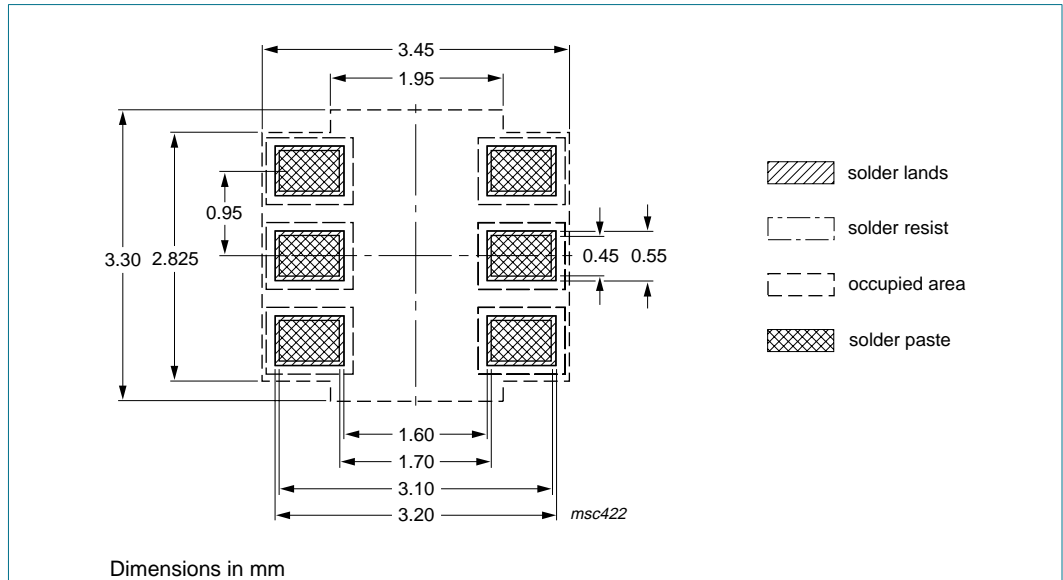
| Type number | Package | Description | Packing quantity | |
|-------------|---------|--|------------------|-------|
| | | | 3000 | 10000 |
| PBSS305ND | SOT457 | 4 mm pitch, 8 mm tape and reel; T1 [2] | -115 | -135 |
| | | 4 mm pitch, 8 mm tape and reel; T2 [3] | -125 | -165 |

[1] For further information and the availability of packing methods, see [Section 14](#).

[2] T1: normal taping

[3] T2: reverse taping

11. Soldering



12. Revision history

Table 9. Revision history

| Document ID | Release date | Data sheet status | Change notice | Supersedes |
|----------------|--------------|--|---------------|-------------|
| PBSS305ND_2 | 20071207 | Product data sheet | - | PBSS305ND_1 |
| Modifications: | | <ul style="list-style-type: none">• The format of this data sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors.• Legal texts have been adapted to the new company name where appropriate.• Table 6: typing error for maximum value on 6 cm² footprint amended• Section 13 "Legal information": updated | | |
| PBSS305ND_1 | 20060410 | Product data sheet | - | - |

13. Legal information

13.1 Data sheet status

| Document status ^{[1][2]} | Product status ^[3] | Definition |
|-----------------------------------|-------------------------------|---|
| Objective [short] data sheet | Development | This document contains data from the objective specification for product development. |
| Preliminary [short] data sheet | Qualification | This document contains data from the preliminary specification. |
| Product [short] data sheet | Production | This document contains the product specification. |

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL <http://www.nxp.com>.

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15. Contents

| | | |
|-----------|--|-----------|
| 1 | Product profile | 1 |
| 1.1 | General description | 1 |
| 1.2 | Features | 1 |
| 1.3 | Applications | 1 |
| 1.4 | Quick reference data | 1 |
| 2 | Pinning information | 2 |
| 3 | Ordering information | 2 |
| 4 | Marking | 2 |
| 5 | Limiting values | 3 |
| 6 | Thermal characteristics | 4 |
| 7 | Characteristics | 7 |
| 8 | Test information | 10 |
| 9 | Package outline | 11 |
| 10 | Packing information | 11 |
| 11 | Soldering | 12 |
| 12 | Revision history | 13 |
| 13 | Legal information | 14 |
| 13.1 | Data sheet status | 14 |
| 13.2 | Definitions | 14 |
| 13.3 | Disclaimers | 14 |
| 13.4 | Trademarks | 14 |
| 14 | Contact information | 14 |
| 15 | Contents | 15 |

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