PIC16(L)F1574/5/8/9

PIC16(L)F1574/5/8/9 Family
Silicon Errata and Data Sheet Clarification

The PIC16(L)F1574/5/8/9 family devices that you have received conform functionally to the current Device Data Sheet (DS40001782**B**), except for the anomalies described in this document.

The silicon issues discussed in the following pages are for silicon revisions with the Device and Revision IDs listed in Table 1 The silicon issues are summarized in Table 2.

The errata described in this document will be addressed in future revisions of the PIC16(L)F1574/5/8/9 silicon.

Note:	This document summarizes all silicon errata issues from all revisions of silicon, previous as well as current. Only the issues indicated in the last column of Table 2 apply to the current silicon revision (**A1**).

Data Sheet clarifications and corrections start on page 4, following the discussion of silicon issues.

The silicon revision level can be identified using the current version of MPLAB® IDE and Microchip's programmers, debuggers, and emulation tools, which are available at the Microchip corporate web site (www.microchip.com).

For example, to identify the silicon revision level using MPLAB IDE in conjunction with a hardware debugger:

1. Using the appropriate interface, connect the device to the hardware debugger.
2. Open an MPLAB IDE project.
3. Configure the MPLAB IDE project for the appropriate device and hardware debugger.
4. Based on the version of MPLAB IDE you are using, do one of the following:
   a) For MPLAB IDE 8, select *Programmer > Reconnect*.
   b) For MPLAB X IDE, select *Window > Dashboard* and click the **Refresh Debug Tool Status** icon ( ).
5. Depending on the development tool used, the part number *and* Device Revision ID value appear in the **Output** window.

Note:	If you are unable to extract the silicon revision level, please contact your local Microchip sales office for assistance.

The DEVREV values for the various PIC16(L)F1574/5/8/9 silicon revisions are shown in Table 1.

TABLE 1: SILICON DEVREV VALUES

Part Number	Device ID(1)	Revision ID for Silicon Revision(2)
		A1
PIC16F1574	3000h	2001h
PIC16F1575	3001h	2001h
PIC16F1578	3002h	2001h
PIC16F1579	3003h	2001h
PIC16LF1574	3004h	2001h
PIC16LF1575	3005h	2001h
PIC16LF1578	3006h	2001h
PIC16LF1579	3007h	2001h

Note 1: The Device IDs (DEVID and DEVREV) are located at the last two implemented addresses of configuration memory space. They are shown in hexadecimal in the format "DEVID DEVREV".

2: Refer to the *"PIC16(L)F157X Memory Programming Specification"* (DS40001766) for detailed information on Device and Revision IDs for your specific device.

TABLE 2: SILICON ISSUE SUMMARY

Module	Feature	Item Number	Issue Summary	Affected Revisions(1)
				A1
Enhanced Universal Synchronous Receiver Transmitter (EUSART)	Transmit mode	1.1	Possible duplicate byte transmitted.	X
16-Bit Pulse-Width Modulation (PWM)	Continuous Run Slave Offset	2.1	Anomalous behavior.	X

Note 1: Only those issues indicated in the last column apply to the current silicon revision.

Silicon Errata Issues

Note:	This document summarizes all silicon errata issues from all revisions of silicon, previous as well as current. Only the issues indicated by the shaded column in the Affected Silicon Revisions tables apply to the current silicon revision (**A1**).

1. Module: Enhanced Universal Synchronous Receiver Transmitter (EUSART)

1.1 Transmit Mode

Under certain conditions, a byte written to the TXREG register can be transmitted twice. This happens when a byte is written to TXREG just as the TSR register becomes empty. This new byte is immediately transferred to the TSR register, but also remains in the TXREG register until the completion of the current instruction cycle. If the new byte in the TSR register is transmitted before this instruction cycle has completed, the duplicate in the TXREG register will subsequently be transferred to the TSR register on the following instruction clock cycle and transmitted.

Work around

When transmitting bytes, it is common practice to check the TXIF bit before writing to the TXREG register. To avoid the issue of duplicate bytes being transmitted, a NOP should be placed before the write to the TXREG register. This changes the timing so that the issue does not occur. The TRMT bit can also be checked in addition to or instead of the TXIF bit to determine if TXREG can be written without causing a duplicate-byte transmission. If the transmit interrupt is enabled then, inside the ISR, testing the TRMT bit will avoid transmission of a duplicate byte.

Affected Silicon Revisions

A1							
X							

2. Module: 16-Bit Pulse-Width Modulation (PWM)

2.1 Continuous Run Slave Offset Mode Anomaly

The 16-bit PWM in Continuous Run Slave mode (PWMxOFTCON<6:5>=11) may get stuck in anomalous behavior. The behavior is that the slave PWM output will toggle when the master PWM matches the master PWM offset value, then toggle again on the next master offset match event. The slave PWM output will then remain steady for the number of master periods equal to the slave PWM period value, after which the sequence repeats. The slave PWM may occasionally start to operate as described by either writing the slave PWMxOFTCON register or enabling the slave PWM from an Idle state.

Work around

None.

Affected Silicon Revisions

A1							
X							

Data Sheet Clarifications

The following typographic corrections and clarifications are to be noted for the latest version of the device data sheet (DS40001782**B**).

Note:	Corrections are shown in **bold**. Where possible, the original bold text formatting has been removed for clarity.

None.

APPENDIX A: DOCUMENT REVISION HISTORY

Rev A Document (2/2015)

Initial release of this document.

Rev B Document (9/2015)

Added Module 1 and 2: EUSART and 16-bit PWM.

Note the following details of the code protection feature on Microchip devices:

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