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November 2014

# FSA8108
# Audio Jack Detection Solution Featuring Volume Up/Down & Send/End Detection

## Features

- Detection:
  - Accessory Plug-In
  - Send / End Key Press
  - Volume Up/Down Key Press
- $V_{DD}$ 2.7 to 4.5 V
- $V_{IO}$ 1.6 V to $V_{DD}$
- THD (MIC) 0.01% Typical
- LDO Output for MIC Bias Voltage: 2.4 V
- ESD (IEC 61000-4-2) 15 kV Air Gap
- Detects 3- or 4-Pole Audio Accessories
- Removes Audio Jack Pop-and-Click Caused by MIC Bias

## Applications

- Cellular Phones, Smart Phones
- MP3 and PMP (Portable Media Player)

## Description

The FSA8108 is an audio jack detection switch for 3- or 4-pole accessories that detects the audio plug connection. The FSA8108 detects volume up/down or send/end key presses. An LDO provides DC bias to microphone and remote key circuit in the accessory. For system flexibility, the FSA8108 features an $I^2C$ port with registers to allow programmability of AC timing specifications.

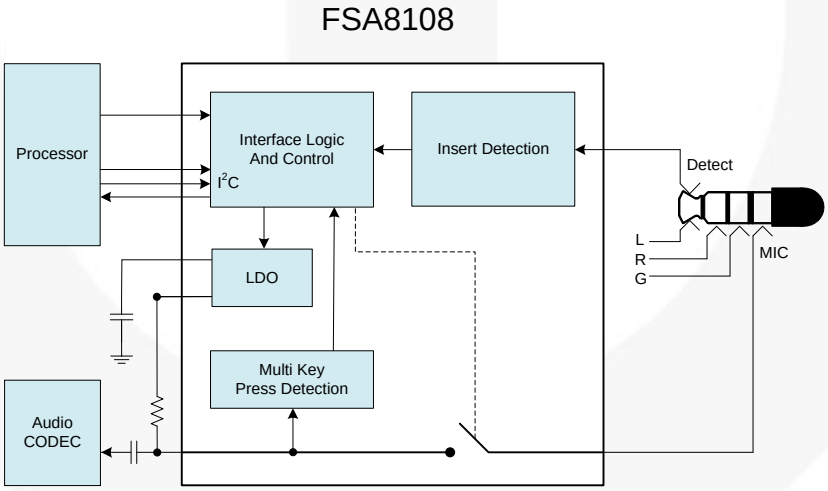



**Figure 1. Typical Application Diagram**

## Ordering Information

| Part Number | Operating Temperature Range | Top Mark | Package |
|---|---|---|---|
| FSA8108BUCX(1) | -40 to +85°C | G6 | 12-Ball, 3 x 4 Array, 0.4 mm Pitch, 250 µm Ball, Wafer-Level Chip-Scale Package |

**Note:**
1. Includes backside lamination.

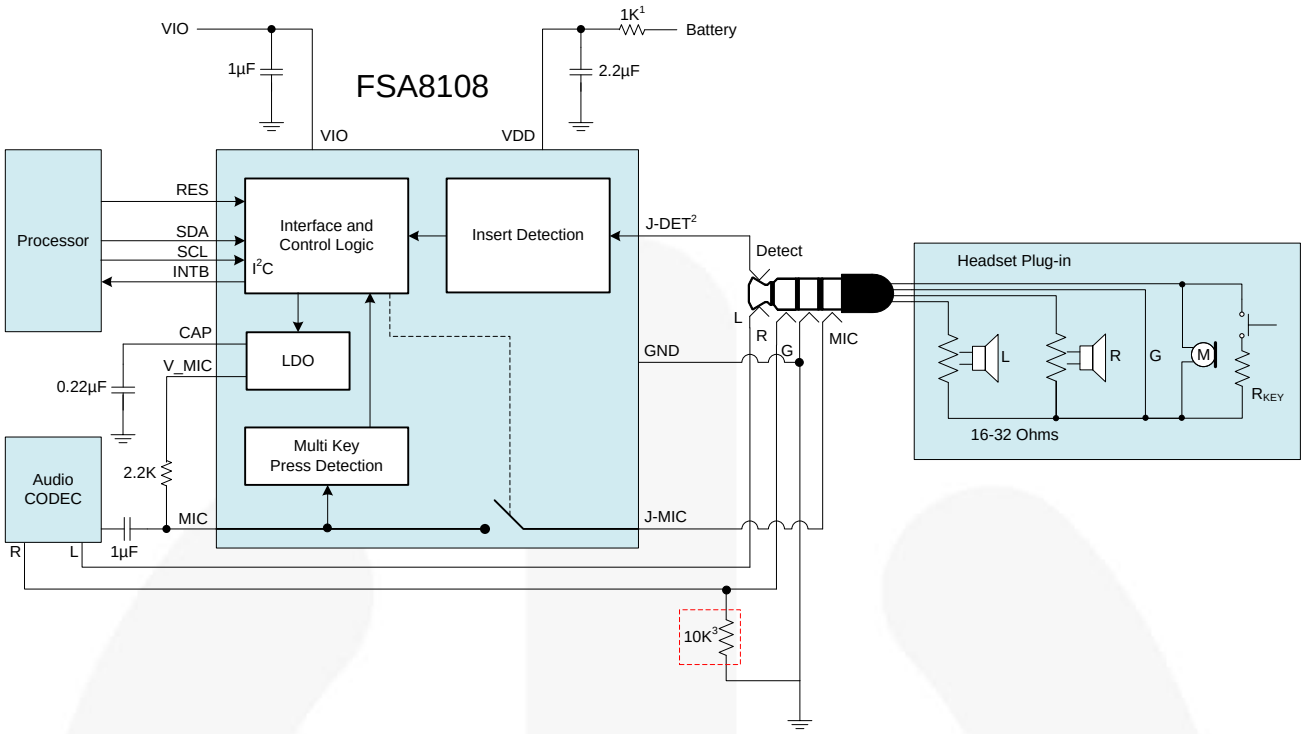



**Figure 2. Typical Application Diagram**

**Notes:**

2. A 1 kΩ resistor with a 2.2 µF capacitor is recommended for direct battery connection. This filter helps stabilize power rail events not associated with the FSA8039A. If power is supplied from a stable source, such as from a PMIC or LDO, a single 1 µF capacitor is recommended.
3. The J-DET is shorted to the left (L) audio channel when the headset or accessory plug is inserted into most audio jacks. Any external circuitry attached to the J-DET pin could affect audio performance in the 20-20 kHz range on the left channel.
4. The optional 10 kΩ resistor on the left channel is used to assist in detection of high-impedance accessories. This resistor has negligible impact on audio fidelity.

## Pin Configuration

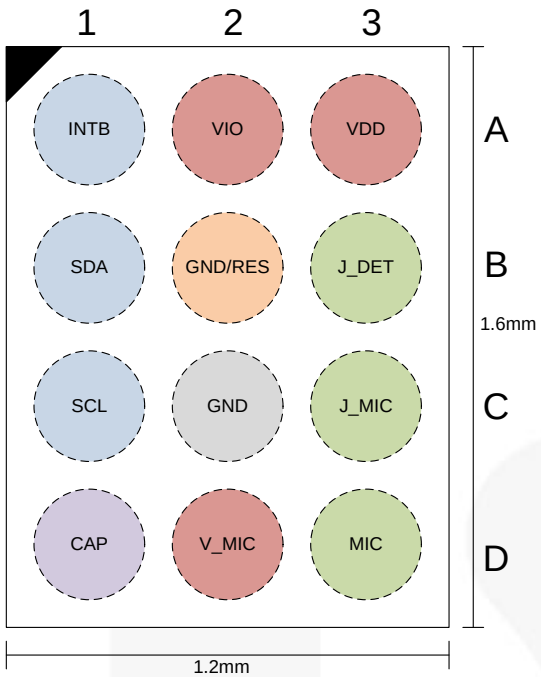



**Figure 3. Pin Assignments**

## Pin Definitions

| Name | PIN | Type | Description |
|---|---|---|---|
| INTB | A1 | Output | Interrupt. Low is interrupt asserted. |
| SDA | B1 | Data | $I^2C$ data |
| SCL | C1 | Data | $I^2C$ input clock |
| CAP | D1 | Output | Internal LDO output. A capacitor to ground is required. |
| VIO | A2 | Power | Baseband I/O supply voltage |
| RES | B2 | Input | Device reset control. Active high reset. Connect to GND if unused. |
| GND | C2 | GND | Ground |
| V_MIC | D2 | Power | LDO output to supply MIC bias voltage (2.4 V) |
| VDD | A3 | Power | Core supply voltage |
| J_DET | B3 | I/O | Input from a pin of the audio jack socket; plug insert/removal detection pin. |
| J_MIC | C3 | I/O | Microphone switch path that connects to the audio jack. |
| MIC | D3 | I/O | Microphone switch path that goes to the microphone input of the codec. |

# Application Information

## Music Mode

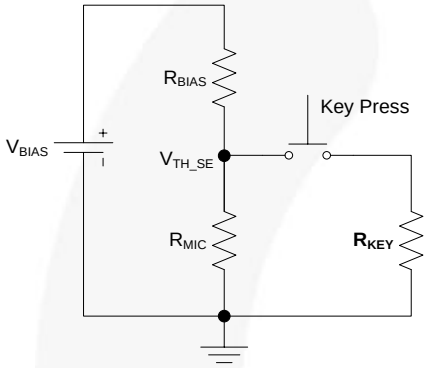
When a 4-pole headset is inserted into the audio jack and a music/listening application is used, the MIC bias is normally enabled for headset button press detection (i.e. mute, volume change, etc.). This consumes power due to a constant path from the MIC bias resistor and microphone in the headset to GND. Fairchild has developed a Music Mode to enable the MIC switch periodically to monitor for a pressed button. This results in a power savings for battery-sensitive devices, such as cell phones or MP3 players. The FSA8108 enters Music Mode when the Music Mode Enable bit in CONTROL(0Ch) is set and a plug is inserted,. Music Mode reduces MIC bias current by approximately 80% with the default Music Mode timing (09h) register value.

## LDO Operation

The integrated microphone bias LDO is set to 2.4 V. The LDO can be used to bias a microphone accessory and is enabled / disabled by the $I^2C$ register bit LDO ENABLE in the CONTROL register(0Ch). This LDO requires a 0.22 µF decoupling capacitor on the output. The decoupling capacitor should be placed close to the LDO pin.

## Headset Key-Press Operation

The headset key-press comparator threshold is a function of the MIC bias voltage, MIC bias resistor, and the MIC impedance. All of these variables must be considered when calculating the key-press resistor value. 0 is an example of how to calculate the key-press resistor value.




$$R_{VOL\ UP\ KEY\ MIN} = \frac{1}{\left(\frac{V_{BIAS\_MAX}-V_{TH\_KEY\_MIN}}{V_{TH\_KEY\_MIN}}\right)\frac{1}{R_{BIAS}} - \frac{1}{R_{MIC}}} = 132\Omega$$

$$R_{VOL\ UP\ KEY\ MAX} = \frac{1}{\left(\frac{V_{BIAS\_MIN}-V_{TH\_KEY\_MAX}}{V_{TH\_KEY\_MAX}}\right)\frac{1}{R_{BIAS}} - \frac{1}{R_{MIC}}} = 286\Omega$$

**Volume up Resistor**
**$V_{BIAS}$, LDO ±5%, 2.28V – 2.25V**
**$R_{BIAS}$=2.2kΩ**
**$R_{MIC}$=2kΩ**
**$V_{TH\_KEY}$ ,Min:120mV default +12%, 0.134V**
**Max: 250mV default-7%, 0233V**

**Figure 4. Example Key-Press Resistor Calculations and Values**

## Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

| Symbol | Parameter | | Min. | Max. | Unit |
|---|---|---|---|---|---|
| $V_{DD}$, $V_{IO}$ | Supply Voltage from Battery | | -0.5 | 6.0 | V |
| $V_{SW}$ | Switch I/O Voltage | | -0.5 | $V_{CC}$+0.5 | V |
| $I_{V\_MIC}$ | V_MIC LDO Supply Current | | | 15 | mA |
| $I_{IK}$ | Input Clamp Diode Current | | -50 | | mA |
| $I_{SW}$ | Switch I/O Current | | | 50 | mA |
| $T_{STG}$ | Storage Temperature Range | | -65 | +150 | °C |
| $T_J$ | Maximum Junction Temperature | | | +150 | °C |
| $T_L$ | Lead Temperature (Soldering, 10 Seconds) | | | +260 | °C |
| ESD | IEC 61000-4-2 System ESD | Air Gap | | 15 | kV |
| | | Contact | | 8 | |
| | Human Body Model, JEDEC JESD22-A114 | J_DET vs. GND, J_MIC vs. GND, VDD vs. GND, VIO vs. GND | | 11 | |
| | | All Pins | | 4 | |
| | Charged Device Model, JEDEC JESD22-C101 | All Pins | | 2 | |

## Recommended Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. Fairchild does not recommend exceeding them or designing to Absolute Maximum Ratings.

| Symbol | Parameter | Min. | Max. | Unit |
|---|---|---|---|---|
| $V_{DD}$ | Supply Voltage | 2.7 | 4.5 | V |
| $V_{IO}$ | I/O Supply Voltage | 1.6 | $V_{DD}$ | V |
| $T_A$ | Operating Temperature | -40 | +85 | ºC |
| $V_{IN}$ | MIC Switch Input Voltage Range | 0 | $V_{DD}$ | V |
| $V_{Audio}$ | Audio Voltage Range on J_DET Pin | -1 | 1 | V |
| $f_{Audio}$ | Audio Frequency on J_DET Pin | 20 | 20000 | Hz |
| $J\_DET_{RL}$ | Resistance on Audio Accessory Left Channel to generate Attach | | 500 | kΩ |

## DC Electrical Characteristics

All typical values are at $T_A$=25°C unless otherwise specified.

| Symbol | Parameter | $V_{DD}$ (V) | Condition | $T_A$=-40 to +85°C | | | Unit |
|---|---|---|---|---|---|---|---|
| | | | | Min. | Typ. | Max. | |
| **MIC Switch** | | | | | | | |
| $R_{ON}$ | MIC Switch On Resistance | 3.8 | $I_{OUT}$=24 mA, $V_{IN}$=2.0 V | | 0.8 | 2.5 | Ω |
| $R_{FLAT}$ | On Resistance Flatness | 3.8 | $I_{OUT}$=24 mA, $V_{IN}$=1 V to $V_{DD}$ | | 0.7 | | Ω |
| $C_{ON(MIC)}$ | MIC Switch On Capacitance | 3.8 | f=1 MHz, $V_{IN}$=100 mV, 50 $mV_{PP}$ | | 16 | | pF |
| $C_{OFF(MIC)}$ | MIC Switch Off Capacitance | 3.8 | f=1 MHz, $V_{IN}$=100 mV, 50 $mV_{PP}$ | | 30 | | pF |
| **J-DET** | | | | | | | |
| $J\_DET_{HYS}$ | Hysteresis of J_DET | | | | 200 | | mV |
| **Parallel I/O Control Signals** | | | | | | | |
| | | | | | | | |
| $V_{IL}$ | Low-Level Input Voltage | | | | | 0.3 • $V_{IO}$ | V |
| $V_{IH}$ | High-Level Input Voltage | | | 0.7 • $V_{IO}$ | | $V_{IO}$ | V |
| **$I^2C$ Controller DC Characteristics Fast Mode (400 kHz)** | | | | | | | |
| $V_{IL}$ | Low-Level Input Voltage | | | -0.5 | | 0.3 $V_{IO}$ | V |
| $V_{IH}$ | High-Level Input Voltage | | | 0.7 $V_{IO}$ | | | V |
| $V_{HYS}$ | Hysteresis of Schmitt Trigger Inputs | | $V_{IO}$>2 V | | | 0.05 $V_{IO}$ | V |
| | | | $V_{IO}$<2 V | | | 0.1 $V_{IO}$ | |
| $V_{OL1}$ | Output Voltage (Open-Drain) | | $V_{IO}$>2 V, 3 mA | 0 | | 0.4 | V |
| | | | $V_{IO}$<2 V, 3 mA | | | 0.2 $V_{IO}$ | V |
| $I_{I2C}$ | Input Current of SDA and SCL Pins, Input Voltage 0.26 V to 2.34 V | | | -10 | | 10 | µA |
| $C_I$ | Capacitance for Each I/O Pin[5] | | | | | 10 | pF |
| **Current Consumption** | | | | | | | |
| $I_{OZ}$ | Off Leakage Current | 4.5 | MIC and J_MIC Port $V_{IN}$ = 4.4 V | | | 1.5 | µA |
| $I_{IN}$ | Input Leakage Current | 0 to 4.5 | Inputs 0 to 4.4 V | | 1 | | µA |
| $I_{DD-SLNA}$ | Sleep Mode Current with No Accessory | 2.7 to 4.5 | J_DET=1 | | 1.5 | | µA |
| $I_{DD-SLWA}$ | Current After Detection With Accessory (Normal Mode) | 2.7 to 4.5 | J_DET=0 | | 35 | | µA |
| $I_{DD-MUSIC\ MODE}$ | Music Mode | 2.7 to 4.5 | $I^2C$ Default Settings | | 25 | | µA |
| $I_{DD\_LDO}$ | Current to Operating LDO, Not Including Output Current | 2.7 to 4.5 | LDO Powered | | 110 | | µA |
| $I_{DD-SLWA\ +\ LDO}$ | Current After Detection With Accessory (Normal Mode) with LDO Current | 2.7 to 4.5 | J_DET=0 | | 145 | | µA |
| $I_{DD\_Music\ Mode\ +\ LDO}$ | Music Mode with LDO | 2.7 to 4.5 | $I^2C$ Default Settings | | 135 | | µA |

*Continued on the following page…*

## DC Electrical Characteristics

All typical values are at $T_A$=25°C unless otherwise specified.

| Symbol | Parameter | $V_{DD}$ (V) | Condition | $T_A$=-40 to +85°C | | | Unit |
|---|---|---|---|---|---|---|---|
| | | | | Min. | Typ. | Max. | |
| **MIC_V LDO Outputs** | | | | | | | |
| MIC_$V_{VOUT}$ | Output Voltage | 2.7 to 4.5 | | -5% | 2.4 | +5% | V |
| MIC_$V_{IOUT}$ | Maximum Output Current | 2.7 to 4.5 | | 10 | | | mA |
| **Comparator Thresholds for Headset Key Pad (Default Voltage Reference)** | | | | | | | |
| $V_{COMP1}$ | Comparator Threshold for Send/End Sensing for NO Headset | 2.7 to 4.5 | $I^2C$ Default Setting, $V_{MIC}$=2.4 V, $R_{MIC}$=2.2 kΩ | -12% | 120 | +12% | mV |
| $V_{COMP2}$ | Comparator Threshold for Send/End Sensing for NC Headset | 2.7 to 4.5 | $I^2C$ Default Setting, $V_{MIC}$=2.4 V, $R_{MIC}$=2.2 kΩ | -5% | 2300 | +5% | mV |
| $V_{COMP3}$ | Comparator Threshold for Volume_Up Sensing | 2.7 to 4.5 | $I^2C$ Default Setting, $V_{MIC}$=2.4 V, $R_{MIC}$=2.2 kΩ | -7% | 250 | +7% | mV |
| $V_{COMP4}$ | Comparator Threshold for Volume_Down Sensing | 2.7 to 4.5 | $I^2C$ Default Setting, $V_{MIC}$=2.4 V, $R_{MIC}$=2.2 kΩ | -7% | 690 | +7% | mV |

**Note:**

5. Not production tested.

## AC Electrical Characteristics

All typical values are at $T_A$=25°C unless otherwise specified; all other values are at the recommended $T_A$ and $T_J$ temperatures. Not production tested.

| Symbol | Parameter | $V_{DD}$ (V) | Condition | $T_A$=-40 to +85°C | | | Unit |
|---|---|---|---|---|---|---|---|
| | | | | Min. | Typ. | Max. | |
| **MIC Switch** | | | | | | | |
| THD | Total Harmonic Distortion | 3.8 | $R_T$=600 Ω, $V_{SW}$=0.5 $V_{PP}$, f=20 Hz to 20 kHz, $V_{IN}$=2.0 V | | 0.01 | | % |
| $O_{IRR}$ | Off Isolation | 3.8 | f=20 kHz, $R_S$=600 Ω, $C_L$=0 pF, $R_T$=600 Ω | | 80 | | dB |
| **Parallel I/O (Default Timing)** | | | | | | | |
| $t_{ON}$ | Switch Turn-On Time | 3.8 | $R_L$=10 kΩ, $C_L$=10 pF | | 100 | | µs |
| $t_{OFF}$ | Switch Turn-Off Time | 3.8 | $R_L$=10 kΩ, $C_L$=10 pF | | 10 | | ns |
| $t_{DET-IN}$ | Debounce Time after J_DET Changes from HIGH to LOW | 2.7 to 4.5 | $I^2C$ Default Setting | | 500 | | ms |
| $t_{DET-REM}$ | Debounce Time after J_DET Changes from Low to HIGH | 2.7 to 4.5 | $I^2C$ Default Setting | | 30 | | µs |
| $t_{DET-MIC}$ | Detection Time of Audio Jack GND and MIC Terminals | 2.7 to 4.5 | $I^2C$ Default Setting | | 50 | | ms |
| $t_{ESD\_DE}$ | Debounce Time for ESD Event on J_DET (Double-Check J_DET Status) | 2.7 to 4.5 | $I^2C$ Default Setting | | 1 | | ms |
| $t_{POLL}$ | ON Time of MIC Switch for Sensing SEND/END Key Press in MP3 Mode | 2.7 to 4.5 | $I^2C$ Default Setting | | 15 | | ms |
| $t_{WAIT}$ | OFF Time of MIC Switch for Sensing SEND/END Key Press in MP3 Mode | 2.7 to 4.5 | $I^2C$ Default Setting | | 150 | | ms |
| $t_{KBK}$ | Debounce Time for Sensing SEND/END Key Press/Release | 2.7 to 4.5 | $I^2C$ Default Setting | | 45 | | ms |
| $t_{KEY-LONG}$ | Minimum Time for Long Key Press | 2.7 to 4.5 | $I^2C$ Default Setting | | 900 | | ms |
| $t_{KEY-Double}$ | Maximum Time between Key Presses for Double-Key Press | 2.7 to 4.5 | $I^2C$ Default Setting | | 1000 | | ms |
| $t_{RES\_DE}$ | Debounce Time for Reset Control | 2.7 to 4.5 | | | 15 | | µs |
| **Power Supply Noise Immunity** | | | | | | | |
| $PSRR_{SW}$ | Power Supply Rejection Ratio for Switch | 3.8 | Power Supply Noise 300 $mV_{PP}$, Measured 10/90%, f=217 Hz | | 95 | | dB |
| $PSRR_{LDO}$ | Power Supply Rejection Ratio for LDO | 3.8 | Power Supply Noise 300 $mV_{PP}$, Measured 10/90%, f=217 Hz, $C_{EXT}$=1 µF | | 100 | | dB |

## I²C Specifications (Fast Mode)

| Symbol | Parameter | Min. | Max. | Unit |
|---|---|---|---|---|
| $f_{SCL}$ | SCL Clock Frequency | 0 | 400 | kHz |
| $t_{HD;STA}$ | Hold Time (Repeated) START Condition | 0.6 | | µs |
| $t_{LOW}$ | LOW Period of SCL Clock | 1.3 | | µs |
| $t_{HIGH}$ | HIGH Period of SCL Clock | 0.6 | | µs |
| $t_{SU;STA}$ | Set-up Time for Repeated START Condition | 0.6 | | µs |
| $t_{HD;DAT}$ | Data Hold Time | 0 | 0.9 | µs |
| $t_{SU;DAT}$ | Data Set-up Time(6) | 100 | | ns |
| $t_r$ | Rise Time of SDA and SCL Signals(6,7) | 20+0.1$C_b$ | 300 | ns |
| $t_f$ | Fall Time of SDA and SCL Signals(6,7) | 20+0.1$C_b$ | 300 | ns |
| $t_{SU;STO}$ | Set-up Time for STOP Condition | 0.6 | | µs |
| $t_{BUF}$ | BUS-Free Time between STOP and START Conditions | 1.3 | | µs |
| $t_{SP}$ | Pulse Width of Spikes that Must Be Suppressed by the Input Filter | 0 | 50 | ns |

**Notes:**

6. A Fast-Mode I²C-Bus® device can be used in a Standard-Mode I²C-Bus system; but the requirement $t_{SU;DAT} \geq 250$ ns must be met. This is automatically the case if the device does not stretch the LOW period of the I2C_SCL signal. If the device does stretch the LOW period of the I2C_SCL signal, it must output the next data bit to the I2C_SDA line $t_{r\_max} + t_{SU;DAT} = 1000 + 250 = 1250$ ns (according to the Standard-Mode I²C Bus specification) before the I2C_SCL line is released.
7. $C_b$ equals the total capacitance of one BUS line in pF. If mixed with high-speed devices, faster fall times are allowed according to the I²C specification.

## I²C Timing

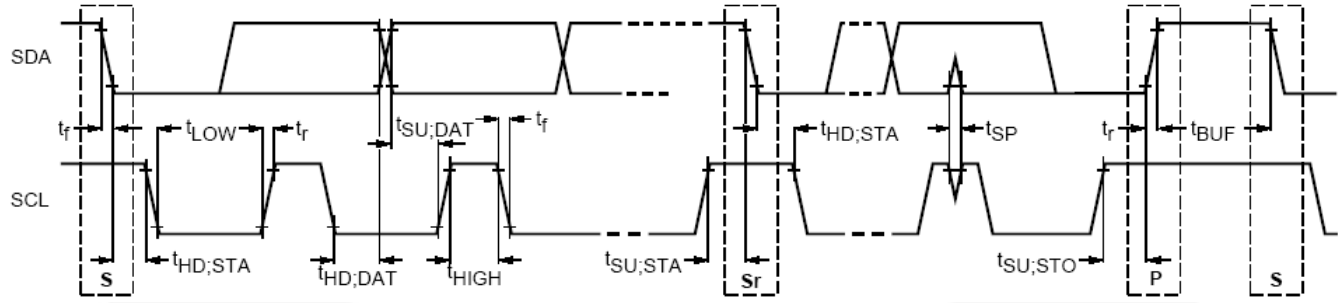



**Figure 5. Definition of Timing for Full-Speed Mode Devices on the I²C Bus**

| Name | Size(Bits) | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|---|
| Slave Address | 8 | 0 | 1 | 0 | 0 | 0 | 1 | 1 | Read/White |

**Figure 6. I²C Slave Address**

**Table 1. Register Definitions**

| Address | Register | Type | Reset Values | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 |
|---|---|---|---|---|---|---|---|---|---|---|---|
| 01H | Device ID | R | 00000000 | Version ID | | | | Reserved | | | |
| 02H | Interrupt 1 | R | 00000000 | Reserved | | Send/End Long Key Press | Send/End Double Key Press | Send/End Key Press | Plug Disconnect | 4-Pole Plug Connect | 3-Pole Plug Connect |
| 03H | Interrupt 2 | R | 00000000 | Reserved | | Volume Down Long Key release | Volume Down Long Key Press | Volume Down Key Press | Volume Up Long Key release | Volume Up Long Key Press | Volume Up Key Press |
| 04H | Interrupt Mask 1 | R/W | 00000000 | Reserved | | Send/End Long Key Press Mask | Send/End Double Key Press Mask | Send/End Key Press Mask | Plug Disconnect Mask | 4-Pole Plug Connect Mask | 3-Pole Plug Connect Mask |
| 05H | Interrupt Mask 2 | R/W | 00000000 | Reserved | | Volume Down Long Key release Mask | Volume Down Long Key Press Mask | Volume Down Key Press Mask | Volume Up Long Key Release Mask | Volume Up Long Key Press Mask | Volume Up Key Press Mask |
| 06H | Global Multiplier | R/W | 00000100 | Reserved | | | | | Global Multiplier Number | | |
| 07H | J_DET Timing | R/W | 10000010 | Insert ($t_{DET-IN}$) | | | | Removal ($t_{DET-REM}$) Global Multiplier Does not apply | | | |
| 08H | Key Press Timing | R/W | 01111000 | Double Key Press Timing ($t_{KEY-Double}$) | | | | Long Key Press Timing ($t_{KEY-LONG}$) | | | |
| 09H | Music Mode Timing | R/W | 00101000 | Key Press Polling Time ($t_{POLL}$) | | | | Key Press Waiting Time ($t_{WAIT}$) | | | |
| 0AH | Detection Timing | R/W | 01010101 | Key Press timing for volume up and volume down ($t_{Key\_Press}$) | | | | Detection Time ($t_{DET-MIC}$) | | | |
| 0BH | Debounce Timing | R/W | 10011000 | Debounce for ESD Event on J_DET ($t_{ESD\_DE}$) | | | | Key Press Debounce Timing ($t_{KBK}$) | | | |
| 0CH | Control | R/W | 01001000 | Stuck S/E On/Off | All Key as Send/End On/Off | Double Key Press On/Off | Long Key Press On/Off | Music Mode | Jack Det On/Off | 3/ 4-Pole Det On/Off | LDO Output On/Off |
| 0DH | Detection Thresholds | R/W | 11101010 | Comparator 2 (Send/End Key - Normally Closed) | | | | Comparator 1 (Send/End Key - Normally Open) | | | |
| 0EH | Detection Thresholds | R/W | 01111001 | Comparator 4 (Volume Down) | | | | Comparator 3 (Volume Down) | | | |
| 0FH | Reset Control | R/W | 00000000 | Reserved | | | | | | Jack Removal Reset | Global Reset |
| 10H | Reserved | R/W | Reserved | Reserved | | | | | | | |

**Notes:**

8. Write “0” to undefined register bits.
9. Values read from undefined register bits are not defined and are invalid.
10. Blocks in green color mean setting change is implemented upon next use.
11. Blocks in blue color mean setting change is implemented after jack removal.

**Table 2. I²C Control**

Reserved Register bit read out as 0
Address: 01H
Reset Value: 00000000
Type: Read

| Device ID | | | Default | 00000000 |
|---|---|---|---|---|
| **Bit #** | **Name** | **Size** | **Function** | |
| 0:3 | Reserved | 4 | Do Not Use | |
| 4:7 | Version ID | 4 | 0000 = Version 0.0 | |
| | | | 0001 = Version 0.1 | |

**Table 3. Interrupt 1**

Address: 02H
Reset Value: 00000000
Type: Read/Clear

| Interrupt 1 | | | Default | 00000000 |
|---|---|---|---|---|
| **Bit #** | **Name** | **Size** | **Function** | |
| 0 | 3-Pole Plug Connect | 1 | 0: No Headset Connected | |
| | | | 1: 3-Pole Headset Connected | |
| 1 | 4-Pole Plug Connect | 1 | 0: No Headset Connected | |
| | | | 1: 4-Pole Headset Connected | |
| 2 | Plug Disconnect | 1 | 0: No Update | |
| | | | 1: Headset Disconnected | |
| 3 | Send/End Key Press | 1 | 0: Send/End Key Not Pressed | |
| | | | 1: Send/End Key Pressed | |
| 4 | Send/End Double Key Press | 1 | 0: Send/End Double Key Not Pressed | |
| | | | 1: Send/End Double Key Pressed | |
| 5 | Send/End Long Key Press | 1 | 0: Send/End Long Key not Pressed | |
| | | | 1: Send/End Long Key Pressed | |
| 6:7 | Reserved | 2 | Do Not Use | |

**Table 4. Interrupt 2**

Address: 03H
Reset Value: 00000000
Type: Read/Clear

| Interrupt 2 | | | Default | 00000000 |
|---|---|---|---|---|
| **Bit #** | **Name** | **Size** | **Function** | |
| 0 | Volume Up Key Press | 1 | 0: Volume Up key not pressed | |
| | | | 1: Volume Up key pressed | |
| 1 | Volume Up Key Long Press | 1 | 0: Volume Up Long key not pressed | |
| | | | 1: Volume Up Long key pressed | |
| 2 | Volume Up Key Long Release | 1 | 0: Volume Up Long key not released | |
| | | | 1: Volume Up Long key released | |
| 3 | Volume Down Key Press | 1 | 0: Volume Down key not pressed | |
| | | | 1: Volume Down Key Press | |
| 4 | Volume Down Long Key Press | 1 | 0: Volume Down Long Key Not Pressed | |
| | | | 1: Volume Down Long Key Pressed | |
| 5 | Volume Down Long Key Release | 1 | 0: Volume Down Key Not Released | |
| | | | 1: Volume Down Key Released | |
| 6:7 | Reserved | 2 | Do Not Use | |

**Table 5. Interrupt Mask 1**

Address: 04H
Reset Value: 00000000
Type: Read/Write

| Interrupt Mask 1 | | | Default | 00000000 |
|---|---|---|---|---|
| **Bit #** | **Name** | **Size** | **Function** | |
| 0 | 3-Pole Plug Connect | 1 | 0: Do Not Mask 3-Pole Plug Connect Interrupt | |
| | | | 1: Mask 3-Pole Plug Connect Interrupt | |
| 1 | 4-Pole Plug Connect | 1 | 0: Do Not Mask 4-Pole Plug Connect Interrupt | |
| | | | 1: Mask 4-Pole Plug Connect Interrupt | |
| 2 | Plug Disconnect | 1 | 0: Do Not Mask Plug Disconnect Interrupt | |
| | | | 1: Mask Plug Disconnect Interrupt | |
| 3 | Send/End Key Press | 1 | 0: Do Not Mask Send/End Key Press Interrupt | |
| | | | 1: Mask Send/End Key Press Interrupt | |
| 4 | Send/End Double Key Press | 1 | 0: Do Not Mask Send/End Key Double Press Interrupt | |
| | | | 1: Mask Send/End Key Double Key Press Interrupt | |
| 5 | Send/End Long Key Press | 1 | 0: Do Not Mask Send/End Long Key Press Interrupt | |
| | | | 1: Mask Send/End Long Key Press Interrupt | |
| 6:7 | Reserved | 2 | Do Not Use | |

**Table 6. Interrupt Mask 2**

Address: 05H
Reset Value: 00000000
Type: Read/Write

| Interrupt Mask 2 | | | Default | 00000000 |
|---|---|---|---|---|
| **Bit #** | **Name** | **Size** | **Function** | |
| 0 | Volume Up Key Press | 1 | 0: Do Not Mask Volume Up Key Press Interrupt | |
| | | | 1: Mask Volume Up Key Press Interrupt | |
| 1 | Volume Up Key Long Press | 1 | 0: Do Not Mask Volume Up Long Key Press Interrupt | |
| | | | 1: Mask Volume Up Long Key Press Interrupt | |
| 2 | Volume Up Key Long Release | 1 | 0: Do Not Mask Volume Up Long Key Release Interrupt | |
| | | | 1: Mask Volume Up Long Key Release Interrupt | |
| 3 | Volume Down Key Press | 1 | 0: Do Not Mask Volume Down Key Press Interrupt | |
| | | | 1: Mask Volume Down Key Press Interrupt | |
| 4 | Volume Down Long Key Press | 1 | 0: Do Not Mask Volume Down Long Key Press Interrupt | |
| | | | 1: Mask Volume Down Long Key Press Interrupt | |
| 5 | Volume Down Long Key Release | 1 | 0: Do Not Mask Volume Down key Release Interrupt | |
| | | | 1: Mask Volume Down key released Interrupt | |
| 6:7 | Reserved | 2 | Do Not Use | |

**Table 7. Global Multiplier Number**

Address: 06H
Reset Value: 00000100
Type: Read/Write

| Global Multiplier Number | | | | | | | | Default | 00000100 |
|---|---|---|---|---|---|---|---|---|---|
| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | Function | |
| Reserved | | | | | 0 | 0 | 0 | 1/16 | |
| Reserved | | | | | 0 | 0 | 1 | 1/8 | |
| Reserved | | | | | 0 | 1 | 0 | 1/4 | |
| Reserved | | | | | 0 | 1 | 1 | 1/2 | |
| Reserved | | | | | 1 | 0 | 0 | 1 | |
| Reserved | | | | | 1 | 0 | 1 | 2 | |
| Reserved | | | | | 1 | 1 | 0 | 4 | |
| Reserved | | | | | 1 | 1 | 1 | 8 | |

**Table 8. J_DET Timing**

Address: 07H
Reset Value: 10000010
Type: Read/Write

| J_DET Timing | | | | | | | | | | Default | 10000010 |
|---|---|---|---|---|---|---|---|---|---|---|---|
| Insert ($t_{DET\_IN}$) | | | | | | Removal ($t_{DET\_REM}$) (Global Multiplier Does Not Apply) | | | | | |
| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Function | | Bit 3 | Bit 2 | Bit 1 | Bit 0 | Function | |
| 0 | 0 | 0 | 0 | 100 | ms | 0 | 0 | 0 | 0 | 10 | µs |
| 0 | 0 | 0 | 1 | 150 | | 0 | 0 | 0 | 1 | 20 | |
| 0 | 0 | 1 | 0 | 200 | | 0 | 0 | 1 | 0 | 30 | |
| 0 | 0 | 1 | 1 | 250 | | 0 | 0 | 1 | 1 | 40 | |
| 0 | 1 | 0 | 0 | 300 | | 0 | 1 | 0 | 0 | 50 | |
| 0 | 1 | 0 | 1 | 350 | | 0 | 1 | 0 | 1 | 60 | |
| 0 | 1 | 1 | 0 | 400 | | 0 | 1 | 1 | 0 | 70 | |
| 0 | 1 | 1 | 1 | 450 | | 0 | 1 | 1 | 1 | 80 | |
| 1 | 0 | 0 | 0 | 500 | | 1 | 0 | 0 | 0 | 90 | |
| 1 | 0 | 0 | 1 | 550 | | 1 | 0 | 0 | 1 | 100 | |
| 1 | 0 | 1 | 0 | 600 | | 1 | 0 | 1 | 0 | 110 | |
| 1 | 0 | 1 | 1 | 650 | | 1 | 0 | 1 | 1 | 120 | |
| 1 | 1 | 0 | 0 | 700 | | 1 | 1 | 0 | 0 | 130 | |
| 1 | 1 | 0 | 1 | 750 | | 1 | 1 | 0 | 1 | 140 | |
| 1 | 1 | 1 | 0 | 800 | | 1 | 1 | 1 | 0 | 140 | |
| 1 | 1 | 1 | 1 | 850 | | 1 | 1 | 1 | 1 | 140 | |

**Table 9. Key Press Timing**

Address: 08H

Reset Value: 01111000

Type: Read/Write

| Key Press Timing | | | | | | | | | | Default | 00101000 |
|---|---|---|---|---|---|---|---|---|---|---|---|
| Double Key Press ($t_{DOUBLE}$) | | | | | | Long Key Press ($t_{LONG}$) | | | | | |
| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Function | | Bit 3 | Bit 2 | Bit 1 | Bit 0 | Function | |
| 0 | 0 | 0 | 0 | 100 | ms | 0 | 0 | 0 | 0 | 500 | ms |
| 0 | 0 | 0 | 1 | 200 | | 0 | 0 | 0 | 1 | 550 | |
| 0 | 0 | 1 | 0 | 300 | | 0 | 0 | 1 | 0 | 600 | |
| 0 | 0 | 1 | 1 | 400 | | 0 | 0 | 1 | 1 | 650 | |
| 0 | 1 | 0 | 0 | 500 | | 0 | 1 | 0 | 0 | 700 | |
| 0 | 1 | 0 | 1 | 600 | | 0 | 1 | 0 | 1 | 750 | |
| 0 | 1 | 1 | 0 | 800 | | 0 | 1 | 1 | 0 | 800 | |
| 0 | 1 | 1 | 1 | 1000 | | 0 | 1 | 1 | 1 | 850 | |
| 1 | 0 | 0 | 0 | 1100 | | 1 | 0 | 0 | 0 | 900 | |
| 1 | 0 | 0 | 1 | 1200 | | 1 | 0 | 0 | 1 | 1000 | |
| 1 | 0 | 1 | 0 | 1300 | | 1 | 0 | 1 | 0 | 1100 | |
| 1 | 0 | 1 | 1 | 1400 | | 1 | 0 | 1 | 1 | 1200 | |
| 1 | 1 | 0 | 0 | 1500 | | 1 | 1 | 0 | 0 | 1300 | |
| 1 | 1 | 0 | 1 | 1600 | | 1 | 1 | 0 | 1 | 1400 | |
| 1 | 1 | 1 | 0 | 1800 | | 1 | 1 | 1 | 0 | 1500 | |
| 1 | 1 | 1 | 1 | 2000 | | 1 | 1 | 1 | 1 | 2000 | |

**Table 10. Music Mode Timing**

Address: 09H

Reset Value: 01011000

Type: Read/Write

| Music Mode Timing | | | | | | | | | | Default | 01011000 |
|---|---|---|---|---|---|---|---|---|---|---|---|
| Key Press Polling Time ($t_{POLL}$) | | | | | | Key Press Waiting Time ($t_{WAIT}$) | | | | | |
| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Function | | Bit 3 | Bit 2 | Bit 1 | Bit 0 | Function | |
| 0 | 0 | 0 | 0 | 5 | ms | 0 | 0 | 0 | 0 | 5 | ms |
| 0 | 0 | 0 | 1 | 10 | | 0 | 0 | 0 | 1 | 10 | |
| 0 | 0 | 1 | 0 | 15 | | 0 | 0 | 1 | 0 | 15 | |
| 0 | 0 | 1 | 1 | 20 | | 0 | 0 | 1 | 1 | 20 | |
| 0 | 1 | 0 | 0 | 25 | | 0 | 1 | 0 | 0 | 25 | |
| 0 | 1 | 0 | 1 | 30 | | 0 | 1 | 0 | 1 | 30 | |
| 0 | 1 | 1 | 0 | 35 | | 0 | 1 | 1 | 0 | 50 | |
| 0 | 1 | 1 | 1 | 40 | | 0 | 1 | 1 | 1 | 100 | |
| 1 | 0 | 0 | 0 | 45 | | 1 | 0 | 0 | 0 | 150 | |
| 1 | 0 | 0 | 1 | 50 | | 1 | 0 | 0 | 1 | 200 | |
| 1 | 0 | 1 | 0 | 60 | | 1 | 0 | 1 | 0 | 250 | |
| 1 | 0 | 1 | 1 | 70 | | 1 | 0 | 1 | 1 | 300 | |
| 1 | 1 | 0 | 0 | 80 | | 1 | 1 | 0 | 0 | 350 | |
| 1 | 1 | 0 | 1 | 90 | | 1 | 1 | 0 | 1 | 400 | |
| 1 | 1 | 1 | 0 | 100 | | 1 | 1 | 1 | 0 | 450 | |
| 1 | 1 | 1 | 1 | 150 | | 1 | 1 | 1 | 1 | 500 | |

**Table 11. Detection Timing**

Address: 0AH

Reset Value: 01010101

Type: Read/Write

| Detection Timing | | | | | | | | | | Default | 01010101 |
|---|---|---|---|---|---|---|---|---|---|---|---|
| Key Press Timing for Volume Up and Volume Down ($t_{KEY}$) | | | | | | Detection Time ($t_{DET\_MIC}$) | | | | | |
| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Function | | Bit 3 | Bit 2 | Bit 1 | Bit 0 | Function | |
| 0 | 0 | 0 | 0 | 50 | ms | 0 | 0 | 0 | 0 | **5** | ms |
| 0 | 0 | 0 | 1 | 100 | | 0 | 0 | 0 | 1 | **10** | |
| 0 | 0 | 1 | 0 | 150 | | 0 | 0 | 1 | 0 | **15** | |
| 0 | 0 | 1 | 1 | 200 | | 0 | 0 | 1 | 1 | **20** | |
| 0 | 1 | 0 | 0 | 250 | | 0 | 1 | 0 | 0 | **25** | |
| 0 | 1 | 0 | 1 | 300 | | 0 | 1 | 0 | 1 | **50** | |
| 0 | 1 | 1 | 0 | 350 | | 0 | 1 | 1 | 0 | **75** | |
| 0 | 1 | 1 | 1 | 400 | | 0 | 1 | 1 | 1 | **100** | |
| 1 | 0 | 0 | 0 | 450 | | 1 | 0 | 0 | 0 | **150** | |
| 1 | 0 | 0 | 1 | 500 | | 1 | 0 | 0 | 1 | **200** | |
| 1 | 0 | 1 | 0 | 550 | | 1 | 0 | 1 | 0 | **250** | |
| 1 | 0 | 1 | 1 | 600 | | 1 | 0 | 1 | 1 | **300** | |
| 1 | 1 | 0 | 0 | 650 | | 1 | 1 | 0 | 0 | **350** | |
| 1 | 1 | 0 | 1 | 700 | | 1 | 1 | 0 | 1 | **400** | |
| 1 | 1 | 1 | 0 | 750 | | 1 | 1 | 1 | 0 | **450** | |
| 1 | 1 | 1 | 1 | 800 | | 1 | 1 | 1 | 1 | **500** | |

**Table 12. Key Press Debounce Timing**

Address: 0BH

Reset Value: 10011000

Type: Read/Write

| Key Press Debounce Timing | | | | | | | | | | Default | 10011000 |
|---|---|---|---|---|---|---|---|---|---|---|---|
| Debounce Timing for ESD Event on J_DET (Global Multiplier Does Not Apply) | | | | | | Key Press Debounce Timing | | | | | |
| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Function | | Bit 3 | Bit 2 | Bit 1 | Bit 0 | Function | |
| 0 | 0 | 0 | 0 | 100 | µs | 0 | 0 | 0 | 0 | 5 | ms |
| 0 | 0 | 0 | 1 | 200 | | 0 | 0 | 0 | 1 | 10 | |
| 0 | 0 | 1 | 0 | 300 | | 0 | 0 | 1 | 0 | 15 | |
| 0 | 0 | 1 | 1 | 400 | | 0 | 0 | 1 | 1 | 20 | |
| 0 | 1 | 0 | 0 | 500 | | 0 | 1 | 0 | 0 | 25 | |
| 0 | 1 | 0 | 1 | 600 | | 0 | 1 | 0 | 1 | 30 | |
| 0 | 1 | 1 | 0 | 700 | | 0 | 1 | 1 | 0 | 35 | |
| 0 | 1 | 1 | 1 | 800 | | 0 | 1 | 1 | 1 | 40 | |
| 1 | 0 | 0 | 0 | 900 | | 1 | 0 | 0 | 0 | 45 | |
| 1 | 0 | 0 | 1 | 1000 | | 1 | 0 | 0 | 1 | 50 | |
| 1 | 0 | 1 | 0 | 1200 | | 1 | 0 | 1 | 0 | 55 | |
| 1 | 0 | 1 | 1 | 1400 | | 1 | 0 | 1 | 1 | 60 | |
| 1 | 1 | 0 | 0 | 1600 | | 1 | 1 | 0 | 0 | 65 | |
| 1 | 1 | 0 | 1 | 1800 | | 1 | 1 | 0 | 1 | 70 | |
| 1 | 1 | 1 | 0 | 2000 | | 1 | 1 | 1 | 0 | 75 | |
| 1 | 1 | 1 | 1 | 5000 | | 1 | 1 | 1 | 1 | 80 | |

**Table 13. Control 1**

Address: 0CH

Reset Value: 01001000

Type: Read/Write

| Control 1 | | | Default | 01001000 |
|---|---|---|---|---|
| **Bit #** | **Name** | **Size** | **Function** | |
| 0 | LDO Output | 1 | 0: LDO Output On | |
| | | | 1: LDO Output Off | |
| 1 | MIC Detection | 1 | 0: MIC Detection On | |
| | | | 1: MIC Detection Off | |
| 2 | Jack detection | 1 | 0: Jack Detection On | |
| | | | 1: Jack Detection Off | |
| 3 | Music Mode | 1 | 0: Music Mode On | |
| | | | 1: Music Mode Off | |
| 4 | Long Key Press Function | 1 | 0: Long Key Press Function On | |
| | | | 1: Long Key Press Function Off | |
| 5 | Double Key Press Function | 1 | 0: Double Key Press Function On | |
| | | | 1: Double Key Press Function Off | |
| 6 | All Key as Send/End Function | 1 | 0: All Key as Send/End Function On | |
| | | | 1: All Key as Send/End Function Off | |
| 7 | Stuck S/E Function | 1 | 0: Stuck Send/End Function On | |
| | | | 1: Stuck Send/End Function OFF | |

**Table 14. Detection Thresholds 1**

Address: 0DH

Reset Value: 11101010

Type: Read/Write

| Detection Thresholds 1 | | | | | | | | | | Default | 11101010 |
|---|---|---|---|---|---|---|---|---|---|---|---|
| Normally Closed S/E Key | | | | | | Normally Open S/E Key Maximum/Volume up Key Minimum | | | | | |
| **Bit 7** | **Bit 6** | **Bit 5** | **Bit 4** | **Function** | | **Bit 3** | **Bit 2** | **Bit 1** | **Bit 0** | **Function** | |
| 0 | 0 | 0 | 0 | 1000 | mV | 0 | 0 | 0 | 0 | 20 | mV |
| 0 | 0 | 0 | 1 | 1100 | | 0 | 0 | 0 | 1 | 30 | |
| 0 | 0 | 1 | 0 | 1200 | | 0 | 0 | 1 | 0 | 40 | |
| 0 | 0 | 1 | 1 | 1300 | | 0 | 0 | 1 | 1 | 50 | |
| 0 | 1 | 0 | 0 | 1400 | | 0 | 1 | 0 | 0 | 60 | |
| 0 | 1 | 0 | 1 | 1500 | | 0 | 1 | 0 | 1 | 70 | |
| 0 | 1 | 1 | 0 | 1600 | | 0 | 1 | 1 | 0 | 80 | |
| 0 | 1 | 1 | 1 | 1650 | | 0 | 1 | 1 | 1 | 90 | |
| 1 | 0 | 0 | 0 | 1700 | | 1 | 0 | 0 | 0 | 100 | |
| 1 | 0 | 0 | 1 | 1750 | | 1 | 0 | 0 | 1 | 110 | |
| 1 | 0 | 1 | 0 | 1800 | | 1 | 0 | 1 | 0 | **120** | |
| 1 | 0 | 1 | 1 | 1900 | | 1 | 0 | 1 | 1 | 130 | |
| 1 | 1 | 0 | 0 | 2000 | | 1 | 1 | 0 | 0 | 140 | |
| 1 | 1 | 0 | 1 | 2200 | | 1 | 1 | 0 | 1 | 150 | |
| 1 | 1 | 1 | 0 | **2300** | | 1 | 1 | 1 | 0 | 160 | |
| 1 | 1 | 1 | 1 | 2400 | | 1 | 1 | 1 | 1 | 170 | |

**Table 15. Detection Thresholds 2**

Address: 0EH

Reset Value: 01110111

Type: Read/Write

| Detection Thresholds 2 | | | | | | | | | | Default | 01111001 |
|---|---|---|---|---|---|---|---|---|---|---|---|
| Volume Down Key Maximum | | | | | | Volume Up Key Maximum/Volume Down Key Minimum | | | | | |
| Bit 7 | Bit 6 | Bit 5 | Bit 4 | Function | | Bit 3 | Bit 2 | Bit 1 | Bit 0 | Function | |
| 0 | 0 | 0 | 0 | 270 | mV | 0 | 0 | 0 | 0 | 110 | mV |
| 0 | 0 | 0 | 1 | 330 | | 0 | 0 | 0 | 1 | 125 | |
| 0 | 0 | 1 | 0 | 390 | | 0 | 0 | 1 | 0 | 145 | |
| 0 | 0 | 1 | 1 | 450 | | 0 | 0 | 1 | 1 | 160 | |
| 0 | 1 | 0 | 0 | 510 | | 0 | 1 | 0 | 0 | 175 | |
| 0 | 1 | 0 | 1 | 570 | | 0 | 1 | 0 | 1 | 190 | |
| 0 | 1 | 1 | 0 | 630 | | 0 | 1 | 1 | 0 | 205 | |
| 0 | 1 | 1 | 1 | **690** | | 0 | 1 | 1 | 1 | 220 | |
| 1 | 0 | 0 | 0 | 750 | | 1 | 0 | 0 | 0 | 235 | |
| 1 | 0 | 0 | 1 | 810 | | 1 | 0 | 0 | 1 | **250** | |
| 1 | 0 | 1 | 0 | 870 | | 1 | 0 | 1 | 0 | 265 | |
| 1 | 0 | 1 | 1 | 930 | | 1 | 0 | 1 | 1 | 280 | |
| 1 | 1 | 0 | 0 | 990 | | 1 | 1 | 0 | 0 | 295 | |
| 1 | 1 | 0 | 1 | 1050 | | 1 | 1 | 0 | 1 | 310 | |
| 1 | 1 | 1 | 0 | 1120 | | 1 | 1 | 1 | 0 | 325 | |
| 1 | 1 | 1 | 1 | 1190 | | 1 | 1 | 1 | 1 | 340 | |

**Table 16. Reset Control**

Address: 0FH

Reset Value: 00000000

Type: Read/Write

| Reset Control | | | Default | 00000000 |
|---|---|---|---|---|
| Bit # | Name | Size | Function | |
| 0 | Global Reset | 1 | 0: No Change | |
| | | | 1: Reset Device Reset to all I2C into default values (timing, comparator threshold ) | |
| 1 | Jack Removal Reset | 1 | 0: No Change | |
| | | | 1: Clear I2C register related to Jack Removal process (interrupt) | |
| 2:7 | Reserved | 5 | Do Not Use | |

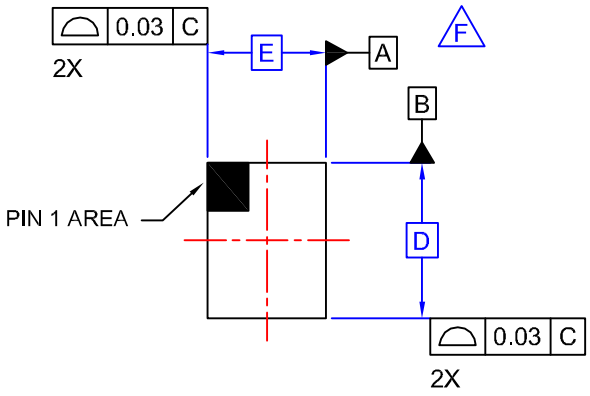
## Nominal Values

| Bump Pitch | Overall Package Height | Silicon Thickness | Solder Bump Height | Solder Bump Diameter |
|---|---|---|---|---|
| 0.4 mm | 0.586 mm | 0.378 mm | 0.208 mm | 0.260 mm |

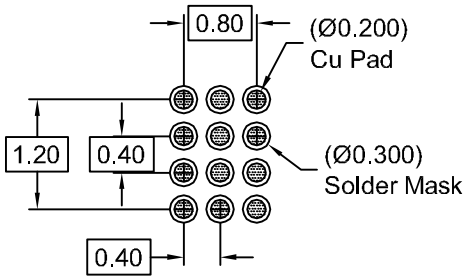
## Package Specific Dimensions

| D | E | X | Y |
|---|---|---|---|
| 1.56 mm | 1.16 mm | 0.18 mm | 0.18 mm |

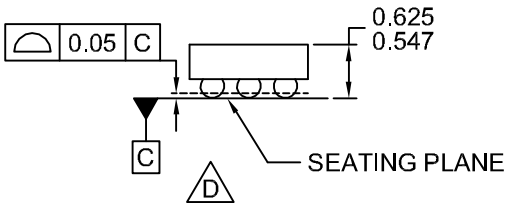
| REVISIONS | | | |
|---|---|---|---|
| REV | DESCRIPTION | DATE | APP'D / SITE |
| 1 | Initial drawing release. | 8-19-09 | L. England / FSME |

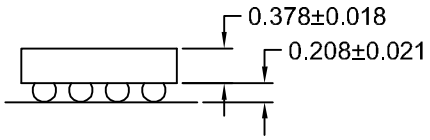



TOP VIEW

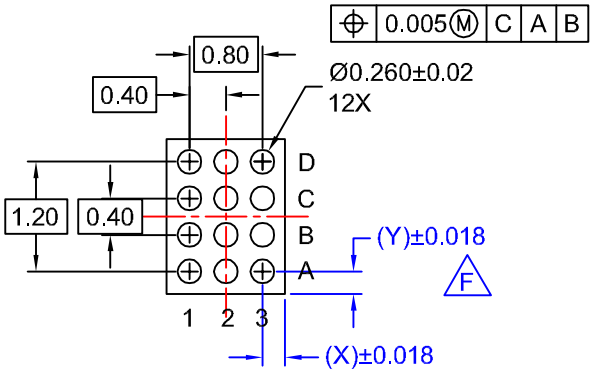



RECOMMENDED LAND PATTERN
(NSMD PAD TYPE)




SIDE VIEWS




BOTTOM VIEW

## NOTES:

A. NO JEDEC REGISTRATION APPLIES.

B. DIMENSIONS ARE IN MILLIMETERS.

C. DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994.

D. DATUM C IS DEFINED BY THE SPHERICAL CROWNS OF THE BALLS.

E. PACKAGE NOMINAL HEIGHT IS 586 MICRONS ±39 MICRONS (547-625 MICRONS).

F. FOR DIMENSIONS D, E, X, AND Y SEE PRODUCT DATASHEET.

G. DRAWING FILENAME: MKT-UC012ACrev1.

| APPROVALS | DATE |
|---|---|
| DRAWN L. England | 8-19-09 |
| DFTG. CHK. S. Martin | 8-19-09 |
| ENGR. CHK. | |
| | |

FAIRCHILD SEMICONDUCTOR™

12BALL WLCSP, 3X4 ARRAY
0.4MM PITCH, 250UM BALL

PROJECTION INCH [MM]

| SCALE | SIZE | DRAWING NUMBER | REV |
|---|---|---|---|
| N/A | N/A | MKT-UC012AC | 1 |

DO NOT SCALE DRAWING | SHEET 1 of 1

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