SAM D5x/E5x Family Silicon Errata and Data Sheet Clarification

SAM D5x/E5x Family Errata

The SAM D5x/E5x family of devices that you have received conform functionally to the current Device Data Sheet (DS60001507**B**), except for the anomalies described in this document.

The silicon issues discussed in the following pages are for silicon revisions with the Device and Revision IDs listed in Table 1. SAM D5x/E5x Family Silicon Device Identification. The silicon issues are summarized in the Table of Contents following this section.

The errata described in this document will be addressed in future revisions of the SAM D5x/E5x family silicon.

Note: This document summarizes all silicon errata issues from all revisions of silicon, previous as well as current.

Table 1. SAM D5x/E5x Family Silicon Device Identification

Part Number	Device Identification (DID[31:0])	Revision ID (DID.REVISION[3:0])
		A
ATSAME54P19A	0x6184xx01	0x0
ATSAME54P20A	0x6184xx00	
ATSAME54N19A	0x6184xx03	
ATSAME54N20A	0x6184xx02	
ATSAME53N20A	0x6183xx02	
ATSAME53N19A	0x6183xx03	
ATSAME53J18A	0x6183xx06	
ATSAME53J19A	0x6183xx05	
ATSAME53J20A	0x6183xx04	
ATSAME51N19A	0x6181xx01	
ATSAME51N20A	0x6181xx00	
ATSAME51J18A	0x6181xx03	
ATSAME51J19A	0x6181xx02	
ATSAME51J20A	0x6181xx04	
ATSAMD51P20A	0x6006xx00	
ATSAMD51P19A	0x6006xx01	
ATSAMD51N19A	0x6006xx03	
ATSAMD51N20A	0x6006xx02	
ATSAMD51J18A	0x6006xx06	
ATSAMD51J19A	0x6006xx05	
ATSAMD51J20A	0x6006xx04	
ATSAMD51G18A	0x6006xx08	
ATSAMD51G19A	0x6006xx07	

Data Sheet clarifications and corrections (if applicable) are located in the section Data Sheet Clarifications, following the discussion of silicon issues.

Note: Refer to the **"Device Service Unit"** chapter in the current device data sheet (DS60001507**B**) for a detailed information on Device Identification and Revision IDs for your specific device.

Table of Contents

1. Silicon Errata Summary

Table 1-1. Errata Summary

Module	Feature	Item Number	Issue Summary	Affected Revisions
				A
Analog -to-Digital Converter(ADC)	ADC SYNCBUSY.SWTRIG	2.1.1	The ADC SYNCBUSY.SWTRIG gets stuck to '1' after wake-up from Standby Sleep mode.	X
Analog -to-Digital Converter(ADC)	ADC TUE/INL/DNL	2.1.2	The ADC TUE/INL/DNL performance is not guaranteed in the following scenarios: • Sampling frequency is above 500 ksps • ADC VREF is different from VDDANA	X
Analog -to-Digital Converter(ADC)	Reference Buffer Offset Compensation	2.1.3	ADC converted data could be erroneous when using the Reference Buffer (REFCTRL.REFSEL =INTREF, INTVCC0, INTVCC1, VREFA or VREB) and when Reference Buffer Offset Compensation is enabled (REFCTRL.REFCOMP = 1).	X
Analog Comparator (AC)	AC Hysteresis	2.2.1	Enabling Hysteresis (COMPCTRLn.HYSTEN = 0x1) changes the threshold voltage (VTH-), which could result in unexpected behavior of the Analog Comparator.	X
Configurable Custom Logic (CCL)	Enable Protected Registers	2.3.1	The SEQCTRLx and LUCTRLx registers are enable-protected by the CTRL.ENABLE bit, whereas they should be enable-protected by the LUTCTRLx.ENABLE bits.	X
Configurable Custom Logic (CCL)	Sequential Logic	2.3.2	LUT output is corrupted after enabling CCL when sequential logic is used.	X

Module	Feature	Item Number	Issue Summary	Affected Revisions
				A
Controller Area Network (CAN)	CAN Edge Filtering	2.4.1	When edge filtering is activated (CCCR.EFBI = 1) and when the end of the integration phase coincides with a falling edge at the Rx input pin, it may occur that the CAN synchronizes itself incorrectly and does not correctly receive the first bit of the frame. In this case, the CRC will detect the first bit that was received incorrectly, it will rate the received FD frame as faulty, and an error frame will be send.	X
Controller Area Network (CAN)	Dominant Bit of Intermission	2.4.2	When NBTP.NTSEG2 is configured to zero (Phase_Seg2(N) = 1), and when there is a pending transmission request, a dominant third bit of Intermission may cause the CAN to wrongly transmit the first identifier bit dominant instead of recessive, even if this bit was configured as '1' in the Tx Buffer Element of the CAN module.	X
Clock Failure Detector (CFD)	CFD with XOSC/ XOSC32K Oscillator	2.5.1	When the CFD is enabled for the XOSC/XOSC32K oscillator and the oscillator input signal is stuck at 1, the clock failure detection works correctly but the switch to the safe clock will fail.	X
Device	Reverse Current in VDDIOB Domain	2.6.1	For the device with 100-pin, 120-pin, and 128-pin counts, when VDDIOB is supplied with the voltage less than VDDIO - 0.7V, reverse current in VDDIOB cluster is observed.	X
Device	Internal Pull-up on the RESET Pin	2.6.2	The internal pull-up of the RESET pin is not functional.	X
Device	Detection of a Debugger Probe	2.6.3	The detection of a debugger probe could fail if the "BOD33 Disable" fuse is cleared (i.e., BOD33 is enabled).	X
Device	VBAT Mode	2.6.4	VBAT mode is not functional.	X

Module	Feature	Item Number	Issue Summary	Affected Revisions
				A
Device	Internal Reference	2.6.5	When the internal reference is used with the DAC and ADC, their outputs become non-linear when the operating temperature is less than 0°C.	X
Device	Device Operation for Temperature < -20°C	2.6.6	If the operating temperature is less than -20°C, the device does not start.	X
Device Service Unit	CRC32	2.7.1	DSU CRC32 will not complete when targeting NVM memory space while the NVM cache is disabled.	X
48 MHz Digital Frequency-Locked Loop (DFLL48M)	COARSE or FINE Calibration Values During the Locking Sequence	2.8.1	If the DFLL48M reaches the maximum or minimum COARSE or FINE calibration values during the locking sequence, an out of bounds interrupt will be generated.	X
48 MHz Digital Frequency-Locked Loop (DFLL48M)	STATUS.DFLLRDY Bit in Close Loop Mode	2.8.2	In Close Loop mode, the STATUS.DFLLRDY bit does not rise before lock fine occurs. Therefore, the information about DFLL ready to start Close Loop mode is not available.	X
48 MHz Digital Frequency-Locked Loop (DFLL48M)	DFLLVAL.FINE Value When DFLL48M Re-enabled	2.8.3	If the DFLL is disabled and then re-enabled, the DFLLVAL.FINE value is ignored by the DFLL module, which will then start its lock fine process at another frequency.	X
Digital-to-Analog Converter (DAC)	Differential Mode the Smoothing of the Output Signal	2.9.1	In Differential mode the smoothing of the output signal is not fully functional.	X
Digital-to-Analog Converter (DAC)	VDDANA as the DAC Reference	2.9.2	The selection of VDDANA as the DAC reference in DAC.CTRLB.REFSEL is non-functional.	X
Digital-to-Analog Converter (DAC)	DAC on Negative Input AIN3	2.9.3	No analog compare will be done on Comparator 1 (AC1) when using the DAC on negative input AIN3.	X

Module	Feature	Item Number	Issue Summary	Affected Revisions
				A
Digital-to-Analog Converter (DAC)	Interpolation Mode	2.9.4	If the Interpolation mode is enabled (with filter integrated to the DAC), the last data from the filter is missing, hence the DAC final output value does not correspond to the DAC input value.	X
Direct Memory Access Controller (DMAC)	Linked Descriptors	2.10.1	When at least one channel using linked descriptors is already active, a channel Fetch Error (FERR) could occur on enabling a channel with no linked descriptor or the second descriptor (index 1) of the channel being enabled could be fetched by one of the already active channels using linked descriptors.	X
Ethernet MAC (GMAC)	Ethernet Functionality in 64-pin Packages	2.11.1	Ethernet functionality in 64-pin packages is not available.	X
External Interrupt Controller (EIC)	Edge Detection	2.12.1	When enabling EIC, SYNCBUSY.ENABLE is released before EIC is fully enabled. Edge detection can be done only after three cycles of the selected GCLK (GCLK_EIC or CLK_ULP32K).	X
External Interrupt Controller (EIC)	Asynchronous Edge Detection	2.12.2	When the asynchronous edge detection is enabled and the system is in Standby mode, only the first edge will be detected. The following edges are ignored until the system wakes up.	X
Fractional Digital Phase-Locked Loop (FDPLL)	Low-Frequency Input Clock on FDPLLn	2.13.1	When using a low-frequency input clock (≤400kHz) on FDPLLn, several FDPLL unlocks could occur while the output frequency is stable.	X
Fractional Digital Phase-Locked Loop (FDPLL)	FDPLL Ratio in DPLLnRATIO	2.13.2	When changing the FDPLL ratio in DPLLnRATIO register on-the-fly, STATUS.DPLLnLDRTO will not beset when the ratio update will be completed.	X

Module	Feature	Item Number	Issue Summary	Affected Revisions
				A
Non-Volatile Memory Controller (NVMCTRL)	NVM Read Corruption	2.14.1	NVM reads could be corrupted when mixing NVM reads with Page Buffer writes.	X
Peripheral Access Controller (PAC)	PAC Protection Error in FREQM	2.15.1	FREQM reads on the Control B register (FREQM.CTRLB) generate a PAC protection error.	X
	PAC Protection Error in CCL	2.15.2	Writing the Software Reset bit in the Control A register (CTRLASWRST) will trigger a PAC protection error.	X
I/O Pin Controller (PORT)	PORT Read/Write Attempts on Non-Implemented Registers	2.16.1	PORT read/write attempts on non-implemented registers, including addresses beyond the last implemented register group (PA, PB,...), do not generate a PAC protection error.	X
I/O Pin Controller (PORT)	PORT Pull-Up/Pull-Down Resistor	2.16.2	The pull-down on PA24/PA25 are activated during power-up and when Sleep mode is OFF. On all other pins, except those in the VSWOUT cluster, the pull-up is activated during power-up and when Sleep mode is OFF.	X
Real-Time Counter (RTC)	Write Corruption	2.17.1	A 8-bit or 16-bit write access for a 32-bit register, or 8-bit write access for a 16-bit register can fail for the following registers: • The COUNT register in COUNT32 mode • The COUNT register in COUNT16 mode • The CLOCK register in CLOCK mode	X
Serial Communication Interface (SERCOM)	SERCOM-USART: USART Auto-Baud Mode	2.18.1	In USART Auto-Baud mode, missing stop bits are not recognized as inconsistent sync (ISF) or framing (FERR) errors. SAM D5x/E5x Family Silicon Errata Issues	X

Module	Feature	Item Number	Issue Summary	Affected Revisions
				A
Serial Communication Interface (SERCOM)	SERCOM-USART: Collision Detection	2.18.2	In USART operating mode with Collision Detection enabled (CTRLB.COLDEN=1), the SERCOM will not abort the current transfer as expected if a collision is detected and if the SERCOM APB Clock is lower than the SERCOM Generic Clock.	X
Serial Communication Interface (SERCOM)	SERCOM-USART: Debug Mode	2.18.3	In USART operating mode, if DBGCTRL.DBGSTOP=1, data transmission is not halted after entering Debug mode.	X
Serial Communication Interface (SERCOM)	SERCOM-USART: 32-bit Extension Mode	2.18.4	When 32-bit Extension mode is enabled and data to be sent is not in multiples of 4 bytes (which means the length counter must be enabled), additional bytes will be sent over the line.	X
Serial Communication Interface (SERCOM)	SERCOM-UART: TXINV and RXINV Bits	2.18.5	The TXINV and RXINV bits in the CTRLA register have inverted functionality.	X
Serial Communication Interface (SERCOM)	SERCOM-I^2C: SDAHOLD Timing	2.18.6	SDAHOLD timing of the SERCOM-I^2C does not match the value shown in the current device data sheet.	X
Serial Communication Interface (SERCOM)	Repeated Start in High-Speed Master Write Operation	2.18.7	For High-Speed Master Write operations, writing CTRLB.CMD = 0x1 issues a STOP command instead of a Repeated Start making repeated start not possible in that mode.	X
Serial Communication Interface (SERCOM)	Repeated Start in High-Speed Master Read Operation	2.18.8	For High-Speed Master Read operations, sending a NACK (CTRLB.CMD = 0x2) forces a STOP to be issued making repeated start not possible in that mode.	X

Module	Feature	Item Number	Issue Summary	Affected Revisions
				A
Serial Communication Interface (SERCOM)	STATUS.CLKHOLD Bit in Master and Slave Modes	2.18.9	The STATUS.CLKHOLD bit in master and slave modes can be written whereas it is a read-only status bit.	X
Serial Communication Interface (SERCOM)	SERCOM-I^{2}C: I^{2}C in Slave Mode	2.18.10	In I^{2}C mode, LENERR, SEXTOUT, LOWTOUT, COLL and BUSERR bits are not cleared when INTFLAG.AMATCH is cleared.	X
Serial Communication Interface (SERCOM)	SERCOM-I^{2}C: Slave Mode with DMA	2.18.11	In I^{2}C Slave Transmitter mode, at the reception of a NACK, if there is still data to be sent in the DMA buffer, the DMA will push a data to the DATA register.	X
Serial Communication Interface (SERCOM)	SERCOM-I^{2}C: I^{2}C Slave in DATA32B Mode	2.18.12	When SERCOM is configured as an I^{2}C slave in 32-bit Data Mode (DATA32B=1) and the I^{2}C master reads from the I^{2}C slave (slave transmitter) and outputs its NACK (indicating no more data is needed), the I^{2}C slave still receives a DRDY interrupt.	X
Serial Communication Interface (SERCOM)	SERCOM-I^{2}C: 10-bit Addressing Mode	2.18.13	10-bit addressing in I^{2}C Slave mode is not functional.	X
Serial Communication Interface (SERCOM)	SERCOM-I^{2}C: Repeated Start	2.18.14	When the Quick command is enabled (CTRLB.QCEN=1), software can issue a repeated Start by writing either CTRLB.CMD or ADDR.ADDR bit fields.	X
Serial Communication Interface (SERCOM)	SERCOM-SPI: Data Preload	2.18.15	In SPI Slave mode and with Slave Data Preload Enabled (CTRLB.PLOADEN=1), the first data sent from the slave will be a dummy byte if the master cannot keep the Slave Select (SS) line low until the end of transmission.	X

Module	Feature	Item Number	Issue Summary	Affected Revisions
				A
Supply Controller (SUPC)	Buck Converter Mode	2.19.1	Digital Phase-Locked Loop (FDPLL200Mx2) and Digital Frequency-Locked Loop (DFLL48M) PLL's cannot be used with main voltage regulator in Buck converter mode.	X
Timer/Counter (TC)	PERBUF/CCBUFx Register	2.20.1	When clearing the STATUS.PERBUFV/ STATUS.CCBUFx flag, the SYNCBUSY flag is released before the PERBUF/CCBUFx register is restored to its appropriate value.	X
Timer/Counter for Control Applications (TCC)	TCC with EVSYS in SYNC/RESYNC Mode	2.21.1	TCC peripheral is not compatible with an EVSYS channel in SYNC or RESYNC mode.	X
Timer/Counter for Control Applications (TCC)	Dithering Mode with External Retrigger Events	2.21.2	Using TCC in Dithering mode with external retrigger events can lead to an unexpected stretch of right aligned pulses, or shrink of left-aligned pulses.	X

2. Silicon Errata Issues

The following issues apply to the SAM D5x/E5x Family of devices.

2.1 Analog-to-Digital Converter (ADC)

2.1.1 ADC SYNCBUSY.SWTRIG

The ADC SYNCBUSY.SWTRIG gets stuck to '1' after wake-up from Standby Sleep mode.

Workaround

Ignore the ADC SYNCBUSY.SWTRIG status when waking up from Sleep mode.

Affected Silicon Revisions

A							
X							

2.1.2 ADC TUE/INL/DNL Performance

The ADC TUE/INL/DNL performance is not guaranteed in the following scenarios:

- Sampling frequency is above 500 ksps AND
- ADC V_{REF} is different from VDDANA

Workaround

None.

Affected Silicon Revisions

A							
X							

2.1.3 Reference Buffer Offset Compensation

ADC converted data could be erroneous when using the Reference Buffer (REFCTRL.REFSEL = INTREF, INTVCC0, INTVCC1, VREFA or VREB) and when Reference Buffer Offset Compensation is enabled (REFCTRL.REFCOMP = 1).

Workaround

The first five conversions must be ignored. All further ADC module conversions are accurate.

Affected Silicon Revisions

A							
X							

2.2 Analog Comparator (AC)

2.2.1 AC Hysteresis

Enabling Hysteresis (COMPCTRLn.HYSTEN = 0x1) changes the threshold voltage (VTH-), which could result in unexpected behavior of the Analog Comparator.

Workaround
None.

Affected Silicon Revisions

A							
X							

2.3 Configurable Custom Logic (CCL)

2.3.1 Enable Protected Registers

The SEQCTRLx and LUCTRLx registers are enable-protected by the CTRL.ENABLE bit, whereas they should be enable-protected by the LUTCTRLx.ENABLE bits.

Workaround
None.

Affected Silicon Revisions

A							
X							

2.3.2 Sequential Logic Reference

LUT Output is corrupted after enabling CCL when sequential logic is used.

Workaround
Write the CTRL register twice when enabling the CCL.

Affected Silicon Revisions

A							
X							

2.4 Controller Area Network (CAN)

2.4.1 CAN Edge Filtering

When edge filtering is activated (CCCR.EFBI = 1) and when the end of the integration phase coincides with a falling edge at the Rx input pin, it may occur that the CAN synchronizes itself incorrectly and does

not correctly receive the first bit of the frame. In this case, the CRC will detect the first bit that was received incorrectly, it will rate the received FD frame as faulty, and an error frame will be send.

The issue only occurs when there is a falling edge at the Rx input pin (CAN_RX) within the last time quantum (tq) before the end of the integration phase. The last time quantum of the integration phase is at the sample point of the 11th recessive bit of the integration phase. When edge filtering is enabled, the bit timing logic of the CAN sees the Rx input signal delayed by the edge filtering. When the integration phase ends, edge filtering is automatically disabled. This affects the reset of the FD CRC registers at the beginning of the frame. The Classical CRC register is not affected, hence this issue does not affect the reception of Classical frames.

In CAN communication, the CAN module may enter an integrating state (either by resetting the CCCR.INIT or by protocol exception event) while a frame is active on the bus. In this case, the 11 recessive bits are counted between the acknowledge bit and the following start of frame. All nodes have synchronized at the beginning of the dominant acknowledge bit. This means that the edge of the following start of frame bit cannot fall on the sample point, hence the issue does not occur. The issue occurs only when the CAN is by local errors, mis-synchronized with regard to the other nodes.

Glitch filtering as specified in ISO 11898-1:2015 is fully functional.

Edge filtering was introduced for applications where the data bit time is at least 2-tq (of nominal bit time) long. In that case, edge filtering requires at least two consecutive dominant time quanta before the counter counting the 11 recessive bits for idle detection is restarted. This means edge filtering covers the theoretical case of occasional 1-tq long dominant spikes on the CAN bus that would delay idle detection. Repeated dominant spikes on the CAN bus would disturb all CAN communication, so the filtering to speed up idle detection would not help network performance.

When this rare event occurs, the CAN sends an error frame and the sender of the affected frame retransmits the frame. When the retransmitted frame is received, the CAN has left the integration phase and the frame will be received correctly. Edge filtering is only applied during the integration phase and it is never used during normal operation. Because the integration phase is very short with respect to "active communication time", the impact on total error frame rate is negligible. The issue has no impact on data integrity.

The CAN enters the integration phase under the following conditions:

- When CCCR.INIT is set to '0' after start-up
- After a protocol exception event (only when CCCR.PXHD = 0)

Scope:

The erratum is limited to FD frame reception when edge filtering is active (CCCR.EFBI = '1') and when the end of the integration phase coincides with a falling edge at the Rx input pin.

Effects:

The calculated CRC value does not match the CRC value of the received FD frame and the CAN module sends an error frame. After retransmission the frame is received correctly.

Workaround:

Disable edge filtering or wait on retransmission in the event that this rare event occurs.

Affected Silicon Revisions

A							

X							

2.4.2 Dominant Bit of Intermission

When NBTP.NTSEG2 is configured to zero (Phase_Seg2(N) = 1), and when there is a pending transmission request, a dominant third bit of Intermission may cause the CAN to wrongly transmit the first identifier bit dominant instead of recessive, even if this bit was configured as '1' in the Tx Buffer Element of the CAN module.

Workaround

A phase buffer segment 2 of length '1' (Phase_Seg2(N) = 1) is not sufficient to switch to the first identifier bit after the sample point in Intermission where the dominant bit was detected.

The CAN protocol according to ISO 11898-1 defines that a dominant third bit of Intermission causes a pending transmission to be started immediately. The received dominant bit is handled as if the CAN has transmitted a Start-of-Frame (SoF) bit.

The ISO 11898-1 specifies the minimum configuration range for Phase_Seg2(N) to be 2..8 tq. Therefore, excluding a Phase_Seg2(N) of '1' will not affect CAN conformance.

Effects:

If NBTP.NTSEG2 = 0, it may occur that the CAN transmits the first identifier bit dominant instead of recessive.

Update configuration range of NBTP.NTSEG2 from 0..127 tq to 1..127 tq in the CAN documentation.

Affected Silicon Revisions

A							
X							

2.5 Clock Failure Detector (CFD)

2.5.1 CFD with XOSC/XOSC32K Oscillator

When the CFD is enabled for the XOSC/XOSC32K oscillator and the oscillator input signal is stuck at 1, the clock failure detection works correctly but the switch to the safe clock will fail.

Workaround

Two possible workarounds are as follows:

1. If the main clock source comes from the XOSC/XOSC32K oscillator, the only workaround is indirect (i.e., using the WDT in firmware and switch to safe clock source in firmware at WDT reset).
2. Because the clock failure detection is functional, once the STATUS.CLKFAIL is set, and if the STATUS.CLKSW is not set, manually switch to safe clock from firmware by changing the configurations of the Generic Clock Generators that use the XOSC/XOSC32K oscillator as a clock source to use another source clock instead.

Affected Silicon Revisions

A							

X							

2.6 Device

2.6.1 Reverse Current in VDDIOB Domain

For the device with 100-pin, 120-pin, and 128-pin counts, when VDDIOB is supplied with the voltage less than VDDIO - 0.7V, reverse current in VDDIOB cluster is observed.

Workaround
None. Pin PB13 must be tied to ground.

Affected Silicon Revisions

A							
X							

2.6.2 Internal Pull-up on the RESET Pin

The internal pull-up of the RESET pin is not functional.

Workaround
An external 100K pull-up must be added on the RESET pin.

Affected Silicon Revisions

A							
X							

2.6.3 Detection of a Debugger Probe

The detection of a debugger probe could fail if the "BOD33 Disable" fuse is cleared (i.e., BOD33 is enabled).

Workaround
To secure the detection of debugger probes, enable BOD33 using the SUPC.BOD33 register instead of the "BOD33 Disable" fuse. The "BOD33 Disable" fuse must be kept set.

Affected Silicon Revisions

A							
X							

2.6.4 VBAT Mode

V_{BAT} mode is not functional.

Workaround
None.

Affected Silicon Revisions

A							
X							

2.6.5 Internal Reference

When the internal reference is used with the DAC and ADC, their outputs become non-linear when the operating temperature is less than 0°C.

Workaround

The internal reference must be used only for positive temperatures (i.e., above 0°C).

Affected Silicon Revisions

A							
X							

2.6.6 Device Operation for Temperature < -20°C

If the operating temperature is less than -20°C, the device does not start.

Workaround

Apply an external reset pulse at power-up when V_{DD} is higher than 2V, or keep reset line low until V_{DD} is lower than 2V.

A							
X							

2.7 Device Service Unit (DSU)

2.7.1 CRC32

DSU CRC32 will not complete when targeting NVM memory space while the NVM cache is disabled.

Workaround

Be sure to always enable the NVM cache when performing a DSU CRC32 request targeting the NVM memory space.

Affected Silicon Revisions

A							
X							

2.8 48 MHz Digital Frequency-Locked Loop (DFLL48M)

2.8.1 COARSE or FINE Calibration Values During the Locking Sequence

If the DFLL48M reaches the maximum or minimum COARSE or FINE calibration values during the locking sequence, an out of bounds interrupt will be generated. These interrupts will be generated even if

the final calibration values at DFLL48M lock are not at maximum or minimum, and might therefore be false out of bounds interrupts.

Workaround
Check that lockbits, DFLLLCKC and DFLLLCKF, in the OSCCTRL Interrupt Flag Status and Clear register (INTFLAG) are both set before enabling the DFLLOOB interrupt.

Affected Silicon Revisions

A							
X							

2.8.2 STATUS.DFLLRDY Bit in Close Loop Mode

In Close Loop mode, the STATUS.DFLLRDY bit does not rise before lock fine occurs. Therefore, the information about DFLL ready to start Close Loop mode is not available.

Workaround
None.

Affected Silicon Revisions

A							
X							

2.8.3 DFLLVAL.FINE Value When DFLL48M Re-enabled

If the DFLL is disabled and then re-enabled, the DFLLVAL.FINE value is ignored by the DFLL module, which will then start its lock fine process at another frequency.

Workaround
Before writing the final configuration in the DFLLCTRLB register, the DFLL module must be re-enabled in Open Loop mode to read and rewrite the DFLLVAL register.

1. `OSCCTRL->DFLLMUL.reg = X; // Write new DFLLMULL configuration`
2. `OSCCTRL.DFLLCTRLB.reg = 0; // Select Open loop configuration`
3. `OSCCTRL.DFLLCTRLA.bit.ENABLE = 1; // Enable DFLL`
4. `OSCCTRL.DFLLVAL.reg = OSCCTRL->DFLLVAL.reg; // Reload DFLLVAL register`
5. `OSCCTRL.DFLLCTRLB.reg = X; // Write final DFLL configuration`

Affected Silicon Revisions

A							
X							

2.9 Digital-to-Analog Converter (DAC)

2.9.1 Smoothing of the Output Signal in differential Mode

In Differential mode the smoothing of the output signal is not fully functional. Smoothing works normally in Differential mode as long as the value of two consecutive data are both positive or negative. The behavior is incorrect when the data changes from positive to negative or vice versa.

Workaround
None.

Affected Silicon Revisions

A							
X							

2.9.2 VDDANA as the DAC Reference

The selection of VDDANA as the DAC reference in DAC.CTRLB.REFSEL is non-functional.

Workaround
The VDDANA must be connected externally to a V_{REF} pin and DAC.CTRLB.VREFAU must be selected.

Affected Silicon Revisions

A							
X							

2.9.3 DAC on Negative Input AIN3

No analog compare will be done on Comparator 1 (AC1) when using the DAC on negative input AIN3.

Workaround
Use the internal VDD scaler.

Affected Silicon Revisions

A							
X							

2.9.4 Interpolation Mode

If the Interpolation mode is enabled (with filter integrated to the DAC), the last data from the filter is missing, and therefore, the DAC final output value does not correspond to the DAC input value.

Although interrupt events are generated at the end of conversion (EOC), the EOC occurs before the final value from the filter and is of no use in the application.

Workaround
None.

Affected Silicon Revisions

A							
X							

2.10 Direct Memory Access Controller (DMAC)

2.10.1 Linked Descriptors

When at least one channel using linked descriptors is already active, a channel Fetch Error (FERR) could occur on enabling a channel with no linked descriptor or the second descriptor (index 1) of the channel being enabled could be fetched by one of the already active channels using linked descriptors. These errors can occur when a channel is being enabled during the link request of another channel and if the channel number of the channel being enabled is lower than the channel already active.

Workaround

When enabling a channel while other channels using linked descriptors are already active, the channel number of the new channel to enable must be greater than the other channel numbers.

Affected Silicon Revisions

A							
X							

2.11 Ethernet MAC (GMAC)

2.11.1 Ethernet Functionality in 64-pin Packages

Ethernet functionality in 64-pin packages is not available.

Workaround

None.

Affected Silicon Revisions

A							
X							

2.12 External Interrupt Controller (EIC)

2.12.1 Edge Detection

When enabling EIC, SYNCBUSY.ENABLE is released before EIC is fully enabled. Edge detection can be done only after three cycles of the selected GCLK (GCLK_EIC or CLK_ULP32K).

Workaround

None.

Affected Silicon Revisions

A							
X							

2.12.2 Asynchronous Edge Detection

When the asynchronous edge detection is enabled and the system is in Standby mode, only the first edge will be detected. The following edges are ignored until the system wakes up.

Workaround

Use the asynchronous edge detection with debouncer enabled. It is recommended to set the DPRESCALER.PRESCALER and DPRESCALER.TICKON to have the lowest frequency possible. To reduce the power consumption, set the EIC GCLK frequency as low as possible or select the ULP32K clock (EIC CTRLA.CKSEL set).

Affected Silicon Revisions

A							
X							

2.13 Fractional Digital Phase-Locked Loop (FDPLL)

2.13.1 Low-Frequency Input Clock on FDPLLn

When using a low-frequency input clock (≤400kHz) on FDPLLn, FDPLL unlocks could occur while the output frequency is stable.

Workaround

When using a low-frequency input clock (≤ 400KHz) on FDPLLn, enable the lock bypass feature to avoid FDPLL unlocks.

Affected Silicon Revisions

A							
X							

2.13.2 FDPLL Ratio in DPLLnRATIO

When changing the FDPLL ratio in DPLLnRATIO register on-the-fly, STATUS.DPLLnLDRTO will not be set when the ratio update will be completed.

Workaround

Wait for the interruption flag INTFLAG.DPLLnLDRTO instead.

Affected Silicon Revisions

A							
X							

2.14 Non-Volatile Memory Controller (NVMCTRL)

2.14.1 NVM Read Corruption

NVM reads could be corrupted when mixing NVM reads with Page Buffer writes.

Workaround

Disable cache lines before writing to the Page Buffer when executing from NVM or reading data from NVM while writing to the Page Buffer. Cache lines are disabled by writing a one to CTRLA.CACHEDIS0 and CTRLA.CACHEDIS1.

Affected Silicon Revisions

A							
X							

2.15 Peripheral Access Controller (PAC)

2.15.1 PAC Protection Error in FREQM

FREQM reads on the Control B register (FREQM.CTRLB) generate a PAC protection error.

Workaround

None.

Affected Silicon Revisions

A							
X							

2.15.2 PAC Protection Error in CCL

Writing the Software Reset bit in the Control A register (CTRLASWRST) will trigger a PAC protection error.

Workaround

Clear the CCL PAC error each time a CCL software reset is executed.

Affected Silicon Revisions

A							
X							

2.16 I/O Pin Controller (PORT)

2.16.1 PORT Read/Write Attempts on Non-Implemented Registers

PORT read/write attempts on non-implemented registers, including addresses beyond the last implemented register group (PA, PB,...), do not generate a PAC protection error.

Workaround
None.

Affected Silicon Revisions

A							
X							

2.16.2 PORT Pull-Up/Pull-Down Resistor

The pull-down on PA24/PA25 are activated during power-up and when Sleep mode is OFF. On all other pins, except those in the VSWOUT cluster, the pull-up is activated during power-up and when Sleep mode is OFF.

Workaround
None.

Affected Silicon Revisions

A							
X							

2.17 Real-Time Counter (RTC)

2.17.1 Write Corruption

A 8-bit or 16-bit write access for a 32-bit register, or 8-bit write access for a 16-bit register can fail for the following registers:

- COUNT register in COUNT32 mode
- COUNT register in COUNT16 mode
- CLOCK register in CLOCK mode

Workaround
Write the registers with:

- A 32-bit write access for COUNT register in COUNT32 mode, CLOCK register in CLOCK mode
- A 16-bit write access for the COUNT register in COUNT16 mode

Affected Silicon Revisions

A							
X							

2.18 Serial Communication Interface (SERCOM)

2.18.1 SERCOM-USART: Auto-Baud Mode

In USART Auto-Baud mode, missing stop bits are not recognized as inconsistent sync (ISF) or framing (FERR) errors.

Workaround
None.

Affected Silicon Revisions

A							
X							

2.18.2 SERCOM-USART: Collision Detection

In USART operating mode with Collision Detection enabled (CTRLB.COLDEN=1), the SERCOM will not abort the current transfer as expected if a collision is detected and if the SERCOM APB Clock is lower than the SERCOM Generic Clock.

Workaround
The SERCOM APB clock must always be higher than the SERCOM Generic Clock to support collision detection. .

Affected Silicon Revisions

A							
X							

2.18.3 SERCOM-USART: Debug Mode

In USART operating mode, if DBGCTRL.DBGSTOP=1, data transmission is not halted after entering Debug mode.

Workaround
None.

Affected Silicon Revisions

A							
X							

2.18.4 SERCOM-USART: 32-bit Extension Mode

When 32-bit Extension mode is enabled and data to be sent is not in multiples of 4 bytes, which means the length counter must be enabled, and additional bytes will be sent over the line.

Workarounds
Use any one of the following workarounds:

1. Write the Inter-Character Spacing bits (CTRLC.ICSPACE) to a non-zero-value.
2. Do not use length counter in firmware by keeping the data to be sent is in multiples of 4 bytes.

Affected Silicon Revisions

A							

X							

2.18.5 SERCOM-UART: TXINV and RXINV Bits

The TXINV and RXINV bits in the CTRLA register have inverted functionality.

Workaround

In software interpret the TXINV bit as a functionality of RXINV, and conversely, interpret the RXINV bit as a functionality of TXINV.

Affected Silicon Revisions

A							
X							

2.18.6 SERCOM-I^{2}C: SDAHOLD Timing

SDAHOLD timing of the SERCOM-I^{2}C does not match the value shown in the current device data sheet. The following table shows the specified and real values of SDA Hold timing.

Table 2-1. SDA Hold Timing

SDA Hold Time Value	Specified SDA Hold Time	Real SDA Hold Time
0x0	Disabled	Disabled
0x1	50 ns to 100 ns	20 ns to 40 ns
0x2	300 ns to 600 ns	100 ns to 250 ns
0x3	400 ns to 800 ns	150 ns to 350 ns

Workaround

None.

Affected Silicon Revisions

A							
X							

2.18.7 Repeated Start in High-Speed Master Write Operation

For High-Speed Master Write operations, writing CTRLB.CMD = 0x1 issues a STOP command instead of a Repeated Start making repeated start not possible in that mode.

Workaround

None.

Affected Silicon Revisions

A							
X							

2.18.8 Repeated Start in High-Speed Master Read Operation

For High-Speed Master Read operations, sending a NACK (CTRLB.CMD = 0x2) forces a STOP to be issued making repeated start not possible in that mode.

Workaround

None.

Affected Silicon Revisions

A							
X							

2.18.9 STATUS.CLKHOLD Bit in Master and Slave Modes

The STATUS.CLKHOLD bit in master and slave modes can be written whereas it is a read-only status bit.

Workaround

Do not clear STATUS.CLKHOLD bit to preserve the current clock hold state.

Affected Silicon Revisions

A							
X							

2.18.10 SERCOM-I²C: I²C in Slave Mode

In I²C mode, LENERR, SEXTOUT, LOWTOUT, COLL and BUSERR bits are not cleared when INTFLAG.AMATCH is cleared.

Workaround

Manually clear status bits LENERR, SEXTOUT, LOWTOUT, COLL and BUSERR by writing these bits to 1 when set.

Affected Silicon Revisions

A							
X							

2.18.11 SERCOM-I²C: Slave Mode with DMA

In I²C Slave Transmitter mode, at the reception of a NACK, if there is still data to be sent in the DMA buffer, the DMA will push a data to the DATA register. Because a NACK was received, the transfer on the I ²C bus will not occur causing the loss of this data.

Workaround

Configure the DMA transfer size to the number of data to be received by the I²C master. DMA cannot be used if the number of data to be received by the master is not known..

Affected Silicon Revisions

A							
X							

2.18.12 SERCOM-I²C: I²C Slave in DATA32B Mode

When SERCOM is configured as an I²C slave in 32-bit Data Mode (DATA32B=1) and the I²C master reads from the I²C slave (slave transmitter) and outputs its NACK (indicating no more data is needed), the I²C slave still receives a DRDY interrupt.

If the CPU does not write a new data to the I²C slave DATA register, I²C slave will pull SDA line, which will result in stalling the bus permanently.

Workarounds

1. Write a dummy data to data register when a NACK is received from the master.
2. Use command #2 (SERCOMx->I2CS.CTRLB.bit.CMD = 2) when a NACK is received from the master.

Important: Because STATUS.RXNACK always indicates the last received ACK, to determine when a NACK is received from the I²C master, the I²C slave software needs to consider I2CS.STATUS.RXNACK only on the second DRDY interrupt after receiving the AMATCH interrupt.

Affected Silicon Revisions

A							
X							

2.18.13 SERCOM-I²C: 10-bit Addressing Mode

10-bit addressing in I²C Slave mode is not functional.

Workaround

None.

Affected Silicon Revisions

A							
X							

2.18.14 SERCOM-I²C: Repeated Start

When the Quick command is enabled (CTRLB.QCEN=1), software can issue a repeated Start by writing either CTRLB.CMD or ADDR.ADDR bit fields. If in these conditions, SCL Stretch Mode is CTRLA.SCLSM=1, a bus error will be generated.

Workaround

Use Quick Command mode (CTRLB.QCEN=1) only if SCL Stretch Mode is CTRLA.SCLSM=0.

Affected Silicon Revisions

A							
X							

2.18.15 SERCOM-SPI: Data Preload

In SPI Slave mode and with Slave Data Preload Enabled (CTRLB.PLOADEN=1), the first data sent from the slave will be a dummy byte if the master cannot keep the Slave Select (SS) line low until the end of transmission.

Workarounds

In SPI Slave mode, the Slave Select pin (SS) must be kept low by the master until the end of the transmission if the Slave Data Preload feature is used (CTRLB.PLOADEN=1).

Affected Silicon Revisions

A							
X							

2.19 Supply Controller (SUPC)

2.19.1 Buck Converter Mode

Buck Converter mode is not supported when using PLLs. As a result, the information given in Table 54-9 “Active Current Consumption - Active Mode” data for Buck converter mode with FDPLL and DFLL configurations is not valid and must be disregarded.

Workaround

Use the LDO Regulator mode when using FDPLL and DFLL configurations.

Affected Silicon Revisions

A							
X							

2.20 Timer/Counter (TC)

2.20.1 PERBUF/CCBUFx Register

When clearing the STATUS.PERBUFV/STATUS.CCBUFx flag, the SYNCBUSY flag is released before the PERBUF/CCBUFx register is restored to its appropriate value.

Workaround

Clear successively twice the STATUS.PERBUFV/STATUS.CCBUFx flag to ensure that the PERBUF/CCBUFx register value is restored before updating it.

Affected Silicon Revisions

A							
X							

2.21 Timer/Counter for Control Applications (TCC)

2.21.1 TCC with EVSYS in SYNC/RESYNC Mode

TCC peripheral is not compatible with an EVSYS channel in SYNC or RESYNC mode.

Workaround

Use TCC with an EVSYS channel in ASYNC mode.

Affected Silicon Revisions

A							
X							

2.21.2 Dithering Mode with External Retrigger Events

Using TCC in Dithering mode with external retrigger events can lead to an unexpected stretch of right-aligned pulses, or shrink of left-aligned pulses.

Workaround

Do not use retrigger events or actions when the TCC module is configured in Dithering mode.

Affected Silicon Revisions

A							
X							

3. Data Sheet Clarifications

The following typographic corrections and clarifications are to be noted for the latest version of the device data sheet (DS60001507B):

No issues to report at this time.

4. Appendix A: Revision History

Rev. D (08/2018)
The current device data sheet revision letter was updated.

The following silicon issues were added:

- Configurable Custom Logic (CCL):
  - Enable Protected Registers
  - Sequential Logic Reference
- Device:
  - Reverse Current in VDDIOB Domain
- SERCOM:
  - Repeated Start in Master Write Operation in 10-bit Addressing Mode
  - Repeated Start in High-Speed Master Write Operation
  - Repeated Start in High-Speed Master Read Operation
  - STATUS.CLKHOLD Bit in Master and Slave Modes
- Supply Controller (SUPC):
  - Buck Converter Mode
- TCC:
  - TCC with EVSYS in SYNC/RESYNC Mode

Rev. C (04/2018)
The current device data sheet revision letter was updated.

The following silicon issues were added:

- Analog-to-Digital Converter (ADC):
  - Reference Buffer Offset Compensation
- Peripheral Access Controller (PAC):
  - PAC Protection
  - PAC Protection
- Real-Time Counter (RTC):
  - Write Corruption
- SERCOM-I2C:
  - Slave Mode with DMA
  - I^2C Slave in DATA32B Mode
  - I^2C Slave Mode in 10-bit Address
  - Repeated Start
- SERCOM-SPI
  - Data Preload
- SERCOM-UART:
  - Collision Detection

All Data Sheet Clarifications were removed.

Rev. B (10/2017)
This revision includes the following additions:

Silicon Issues

- Ethernet Functionality in 64-pin Packages

Data Sheet Clarifications

- ADC Operating Conditions
- GMAC IEEE 802.3AZ Energy Efficient Support
- SERCOM Baud Rate Equations
- SERCOM in SPI Mode Timing
- TQFP 64-pin Package
- DAC Operating Conditions

Rev. A (7/2017)
Initial release of this document.

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