

## N-channel 600 V, 0.175 $\Omega$ typ., 19.5 A, FDmesh™ II Power MOSFET (with fast diode) in PowerFLAT™ 8x8 HV package

Datasheet – production data

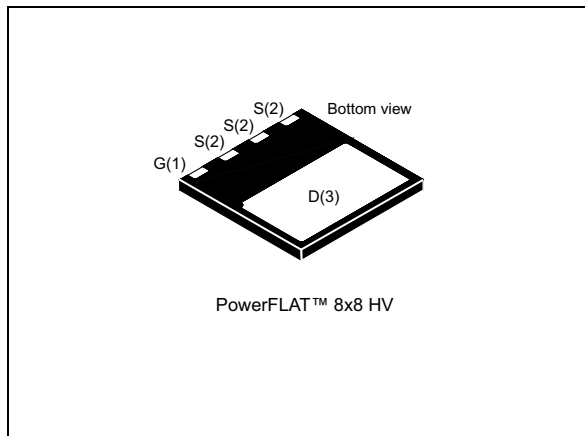
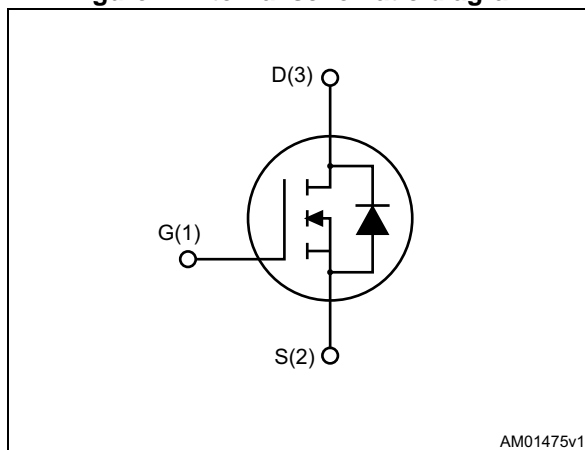


Figure 1. Internal schematic diagram



### Features

Order code	$V_{DS} @ T_{Jmax}$	$R_{DS(on) max}$	$I_D$
STL23NM60ND	650 V	0.199 $\Omega$	19.5 A

- Fast-recovery body diode
- Low gate charge and input capacitance
- Low on-resistance
- 100% avalanche tested
- High dv/dt ruggedness

### Applications

- Switching applications

### Description

This FDmesh™ II Power MOSFET with fast-recovery body diode is produced using MDmesh™ II technology. Utilizing a new strip-lay-out vertical structure, this device features low on-resistance and superior switching performance. It is ideal for bridge topologies and ZVS phase-shift converters.

Table 1. Device summary

Order code	Marking	Package	Packaging
STL23NM60ND	23NM60ND	PowerFLAT™ 8x8 HV	Tape and reel

# Contents

<b>1</b>	<b>Electrical ratings</b> .....	<b>3</b>
<b>2</b>	<b>Electrical characteristics</b> .....	<b>4</b>
2.1	Electrical characteristics (curves) .....	6
<b>3</b>	<b>Test circuits</b> .....	<b>8</b>
<b>4</b>	<b>Package mechanical data</b> .....	<b>9</b>
<b>5</b>	<b>Packaging mechanical data</b> .....	<b>13</b>
<b>6</b>	<b>Revision history</b> .....	<b>15</b>

# 1 Electrical ratings

**Table 2. Absolute maximum ratings**

Symbol	Parameter	Value	Unit
$V_{DS}$	Drain-source voltage	600	V
$V_{GS}$	Gate-source voltage	$\pm 25$	V
$I_D^{(1)}$	Drain current (continuous) at $T_C = 25\text{ }^\circ\text{C}$	19.5	A
$I_D^{(1)}$	Drain current (continuous) at $T_C = 100\text{ }^\circ\text{C}$	11.7	A
$I_{DM}^{(1),(2)}$	Drain current (pulsed)	78	A
$I_D^{(3)}$	Drain current (continuous) at $T_{amb} = 25\text{ }^\circ\text{C}$	2.75	A
$I_D^{(3)}$	Drain current (continuous) at $T_{amb} = 100\text{ }^\circ\text{C}$	1.75	A
$I_{DM}^{(2),(3)}$	Drain current (pulsed)	11	A
$P_{TOT}^{(1)}$	Total dissipation at $T_C = 25\text{ }^\circ\text{C}$	150	W
$P_{TOT}^{(3)}$	Total dissipation at $T_{amb} = 25\text{ }^\circ\text{C}$	3	W
$I_{AR}$	Avalanche current, repetitive or not-repetitive (pulse width limited by $T_j$ max)	9	A
$E_{AS}$	Single pulse avalanche energy (starting $T_j = 25\text{ }^\circ\text{C}$ , $I_D = I_{AR}$ , $V_{DD} = 50\text{ V}$ )	700	mJ
$dv/dt^{(4)}$	Peak diode recovery voltage slope	40	V/ns
$T_{stg}$	Storage temperature	- 55 to 150	$^\circ\text{C}$
$T_j$	Max. operating junction temperature	150	$^\circ\text{C}$

1. The value is rated according to  $R_{thj-case}$
2. Pulse width limited by safe operating area.
3. When mounted on FR-4 board of inch<sup>2</sup>, 2oz Cu.
4.  $I_{SD} \leq 19.5\text{ A}$ ,  $di/dt \leq 600\text{ A}/\mu\text{s}$ ,  $V_{DD} = 80\% V_{(BR)DSS}$ ,  $V_{DS(peak)} < V_{(BR)DSS}$

**Table 3. Thermal data**

Symbol	Parameter	Value	Unit
$R_{thj-case}$	Thermal resistance junction-case max	0.83	$^\circ\text{C}/\text{W}$
$R_{thj-amb}^{(1)}$	Thermal resistance junction-ambient max	45	$^\circ\text{C}/\text{W}$

1. When mounted on FR-4 board of inch<sup>2</sup>, 2oz Cu.

## 2 Electrical characteristics

( $T_C = 25\text{ °C}$  unless otherwise specified)

**Table 4. On /off states**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	$V_{GS} = 0, I_D = 1\text{ mA}$	600			V
$dv/dt^{(1)}$	Drain-source voltage slope	$V_{DD} = 480\text{ V}, I_D = 19.5\text{ A}, V_{GS} = 10\text{ V}$		30		V/ns
$I_{DSS}$	Zero gate voltage drain current	$V_{GS} = 0, V_{DS} = 600\text{ V}$			1	$\mu\text{A}$
		$V_{GS} = 0, V_{DS} = 600\text{ V}, T_C = 125\text{ °C}$			100	$\mu\text{A}$
$I_{GSS}$	Gate-body leakage current	$V_{DS} = 0, V_{GS} = \pm 20\text{ V}$			$\pm 100$	nA
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}, I_D = 250\text{ }\mu\text{A}$	3	4	5	V
$R_{DS(on)}$	Static drain-source on-resistance	$V_{GS} = 10\text{ V}, I_D = 10\text{ A}$		0.175	0.199	$\Omega$

1. Characteristic value at turn off on inductive load

**Table 5. Dynamic**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$C_{iss}$	Input capacitance	$V_{DS} = 50\text{ V}, f = 1\text{ MHz}, V_{GS} = 0$	-	2100	-	pF
$C_{oss}$	Output capacitance		-	80	-	pF
$C_{riss}$	Reverse transfer capacitance		-	10	-	pF
$C_{oss\text{ eq}}^{(1)}$	Equivalent output capacitance	$V_{GS} = 0, V_{DS} = 0\text{ to }480\text{ V}$	-	310	-	pF
$R_G$	Intrinsic gate resistance	$f = 1\text{ MHz}, \text{ gate DC Bias} = 0, \text{ test signal level} = 20\text{ mV}$	-	4	-	$\Omega$
$Q_g$	Total gate charge	$V_{DD} = 480\text{ V}, I_D = 19.5\text{ A}, V_{GS} = 10\text{ V}, \text{ (see Figure 14)}$	-	69	-	nC
$Q_{gs}$	Gate-source charge		-	13	-	nC
$Q_{gd}$	Gate-drain charge		-	35	-	nC

1.  $C_{oss\text{ eq}}$  is defined as a constant equivalent capacitance giving the same charging time as  $C_{oss}$  when  $V_{DS}$  increases from 0 to 80%  $V_{DSS}$

Table 6. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	$V_{DD} = 300\text{ V}$ , $I_D = 10\text{ A}$ , $R_G = 4.7\ \Omega$ , $V_{GS} = 10\text{ V}$ (see <a href="#">Figure 13</a> )	-	21	-	ns
$t_r$	Voltage rise time		-	19	-	ns
$t_{d(off)}$	Turn-off delay time		-	92	-	ns
$t_f$	Current fall time		-	42	-	ns

Table 7. Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$I_{SD}$	Source-drain current		-		19.5	A
$I_{SDM}^{(1)}$	Source-drain current (pulsed)		-		78	A
$V_{SD}^{(2)}$	Forward on voltage	$I_{SD} = 19.5\text{ A}$ , $V_{GS} = 0$	-		1.3	V
$t_{rr}$	Reverse recovery time	$I_{SD} = 19.5\text{ A}$ , $di/dt = 100\text{ A}/\mu\text{s}$ , $V_{DD} = 60\text{ V}$ (see <a href="#">Figure 15</a> )	-	190		ns
$Q_{rr}$	Reverse recovery charge		-	1.2		$\mu\text{C}$
$I_{RRM}$	Reverse recovery current		-	13		A
$t_{rr}$	Reverse recovery time	$I_{SD} = 19.5\text{ A}$ , $di/dt = 100\text{ A}/\mu\text{s}$ , $V_{DD} = 100\text{ V}$ , $T_j = 150\text{ }^\circ\text{C}$ (see <a href="#">Figure 15</a> )	-	270		ns
$Q_{rr}$	Reverse recovery charge		-	2.0		$\mu\text{C}$
$I_{RRM}$	Reverse recovery current		-	15		A

1. Pulse width limited by safe operating area
2. Pulsed: pulse duration = 300  $\mu\text{s}$ , duty cycle 1.5%

## 2.1 Electrical characteristics (curves)

Figure 2. Safe operating area

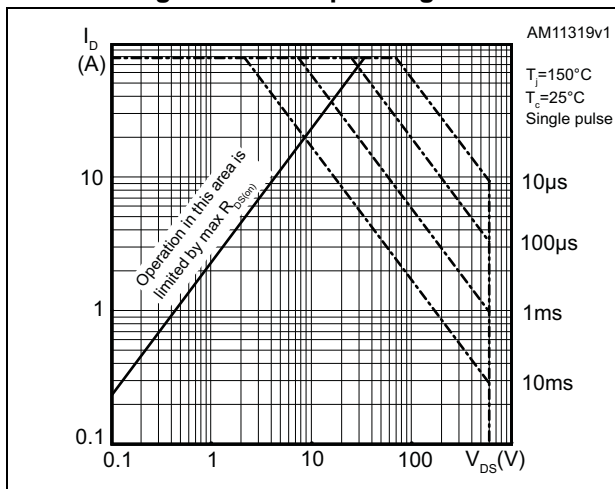


Figure 3. Thermal impedance

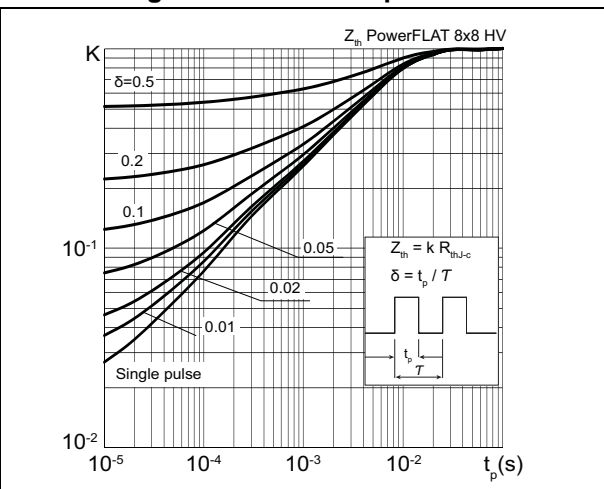


Figure 4. Output characteristics

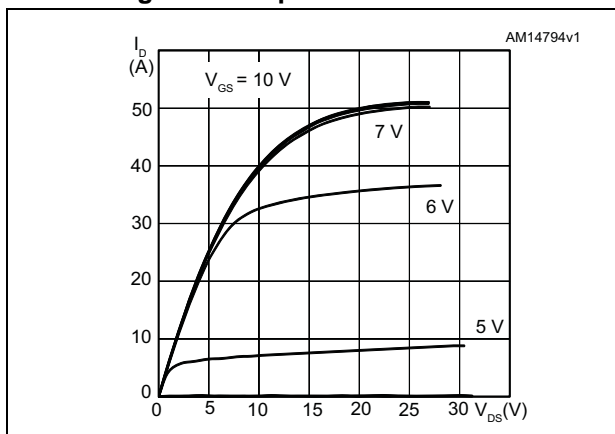


Figure 5. Transfer characteristics

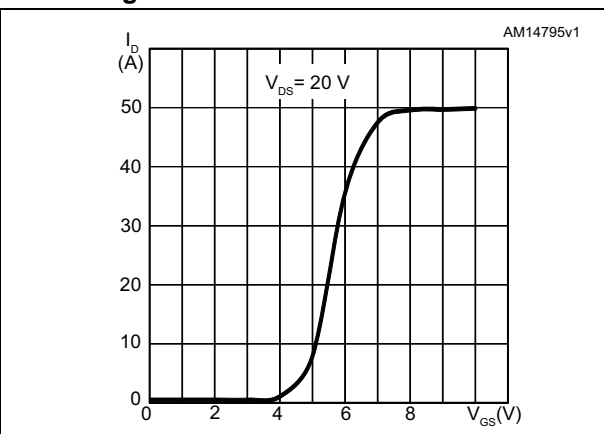


Figure 6. Normalized  $B_{(BR)DSS}$  vs temperature

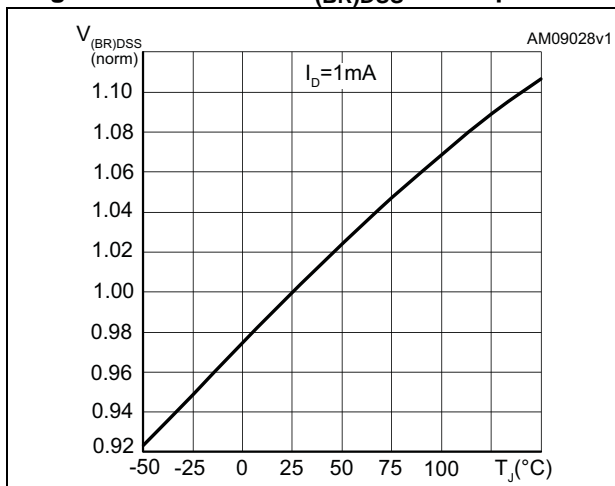


Figure 7. Static drain-source on-resistance

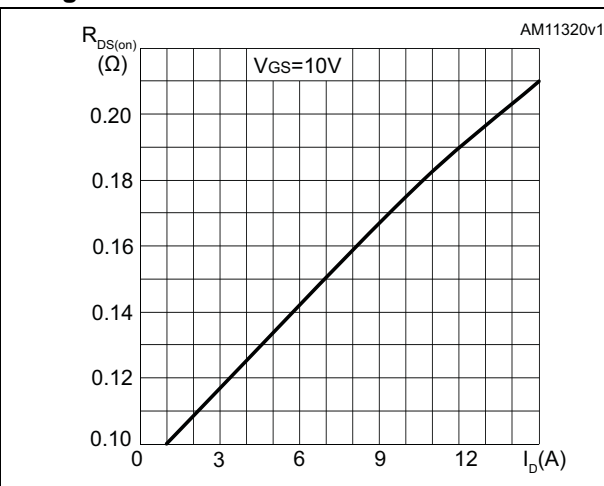


Figure 8. Gate charge vs gate-source voltage

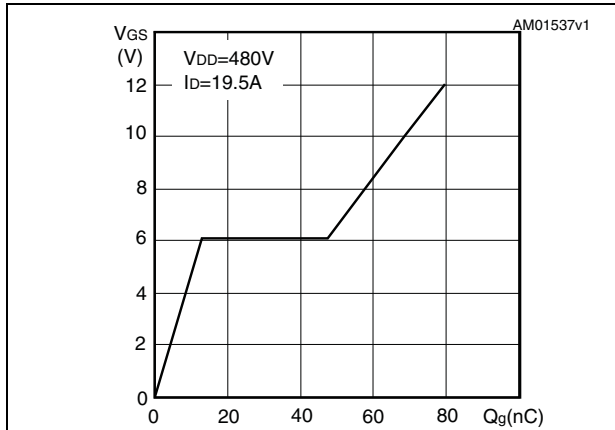


Figure 9. Capacitance variations

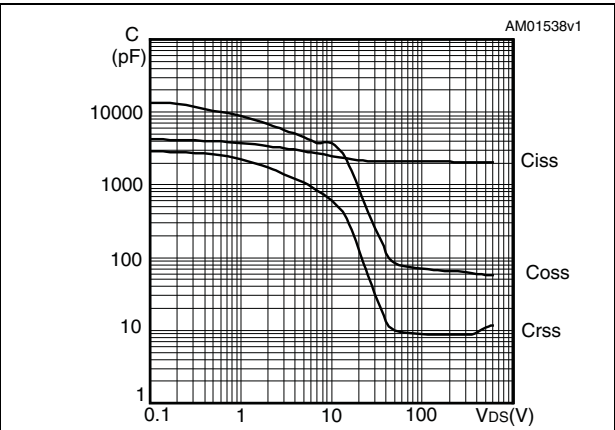


Figure 10. Normalized gate threshold voltage vs temperature

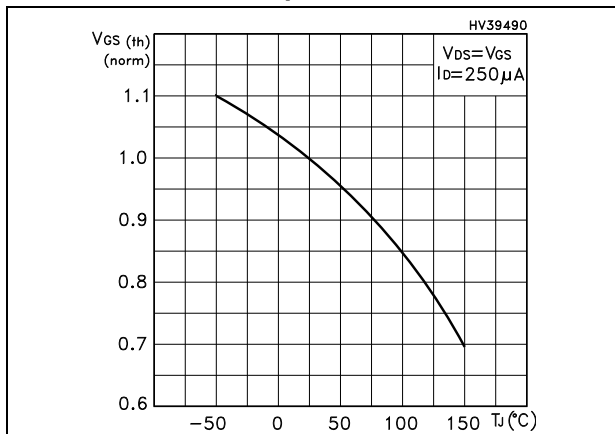


Figure 11. Normalized on-resistance vs temperature

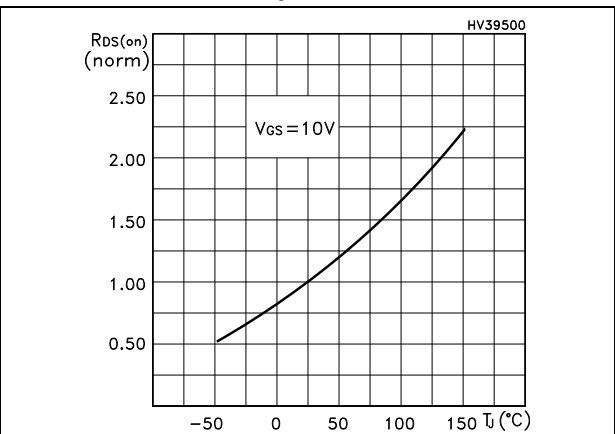
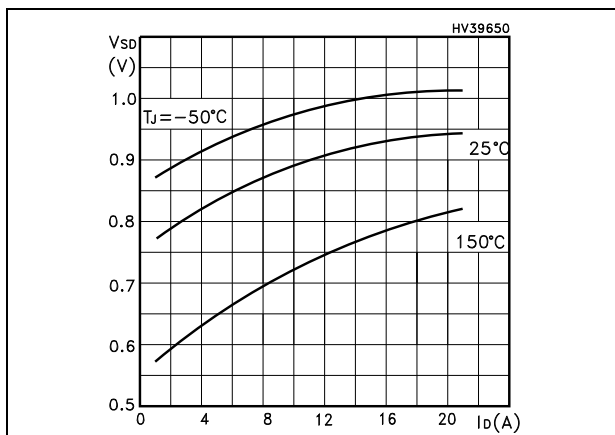
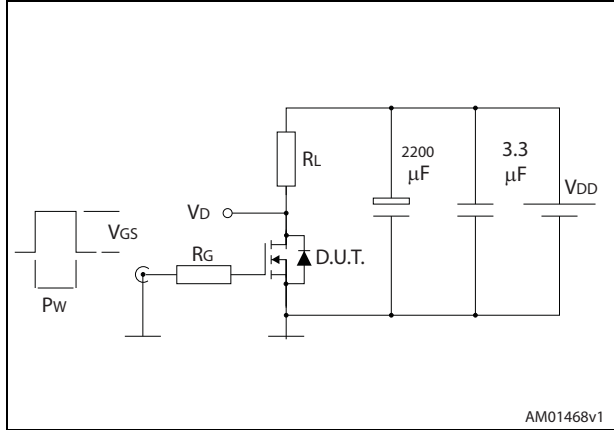


Figure 12. Source-drain diode forward characteristics



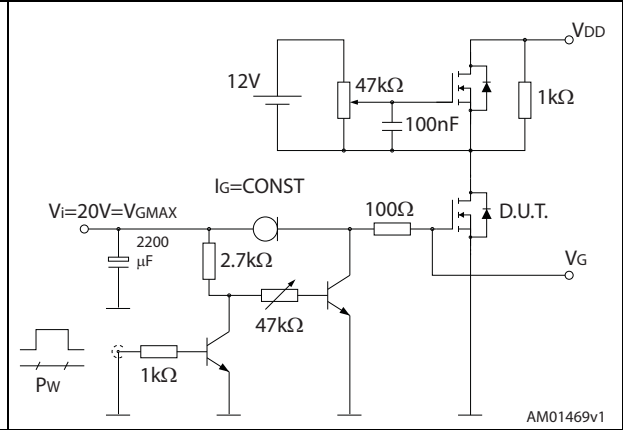
### 3 Test circuits

**Figure 13. Switching times test circuit for resistive load**



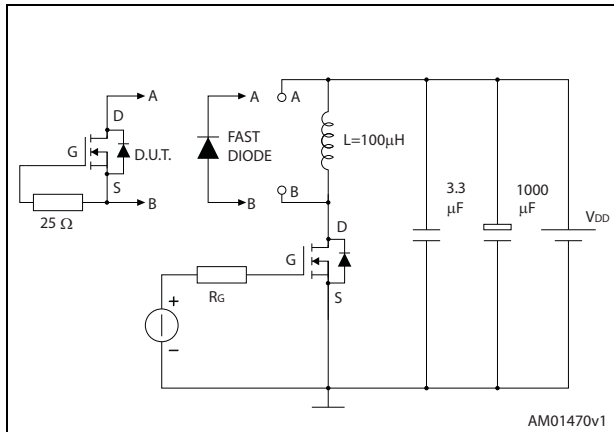
AM01468v1

**Figure 14. Gate charge test circuit**



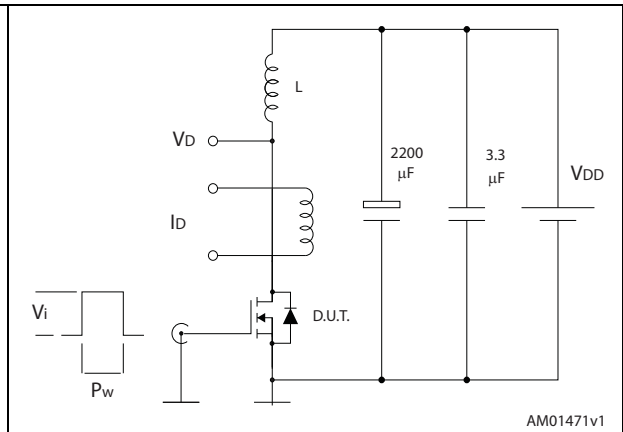
AM01469v1

**Figure 15. Test circuit for inductive load switching and diode recovery times**



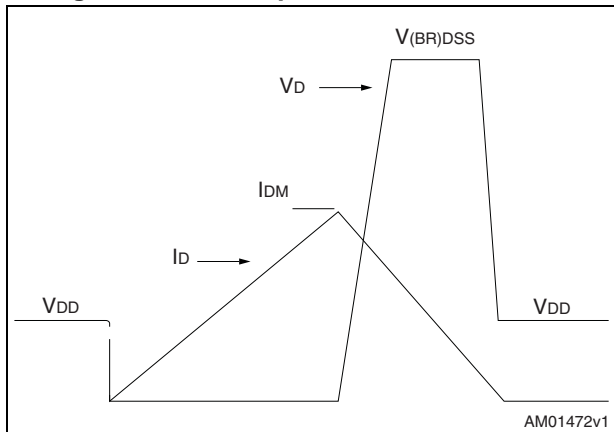
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**Figure 16. Unclamped inductive load test circuit**



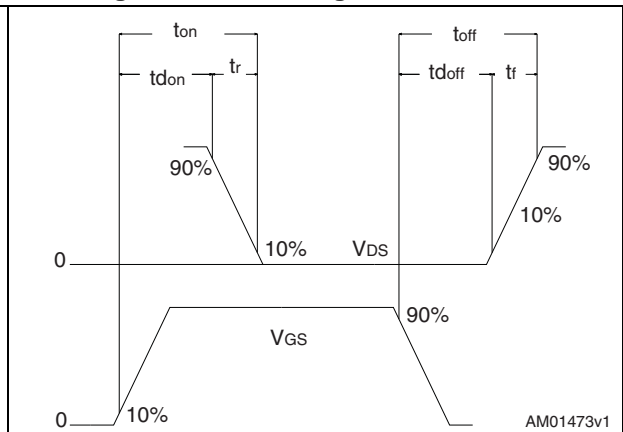
AM01471v1

**Figure 17. Unclamped inductive waveform**



AM01472v1

**Figure 18. Switching time waveform**



AM01473v1



## 4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK<sup>®</sup> packages, depending on their level of environmental compliance. ECOPACK<sup>®</sup> specifications, grade definitions and product status are available at: [www.st.com](http://www.st.com). ECOPACK<sup>®</sup> is an ST trademark.

Figure 19. PowerFLAT™ 8x8 HV drawing mechanical data

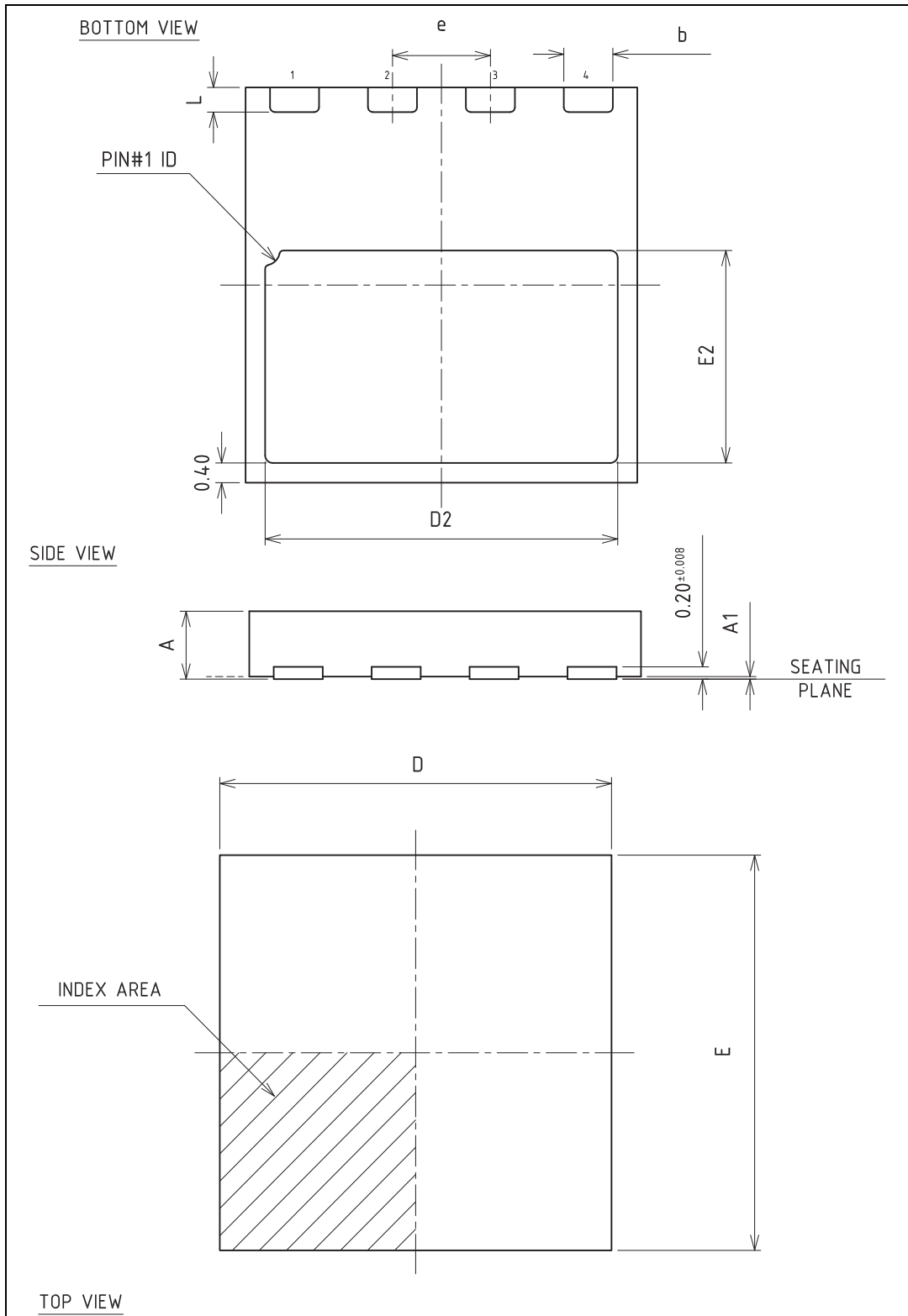
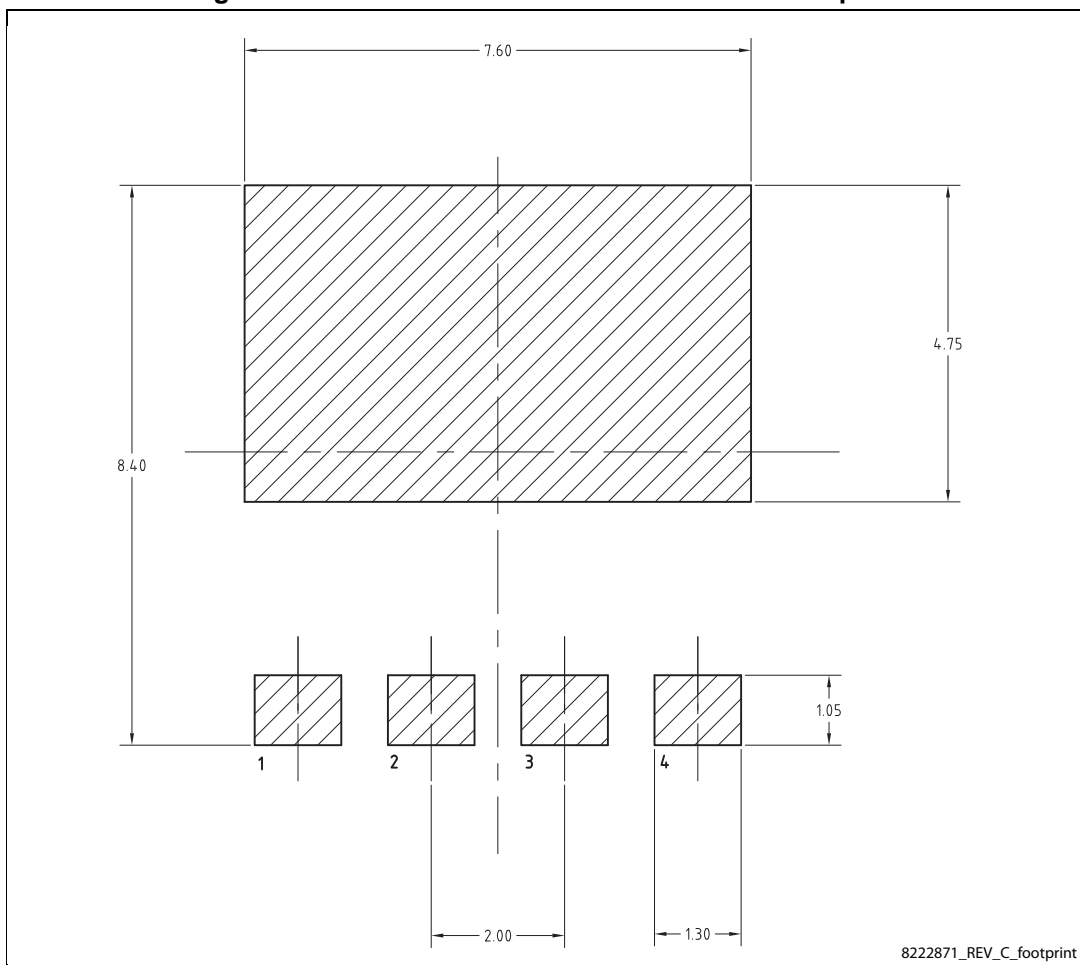


Table 8. PowerFLAT™ 8x8 HV mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	0.80	0.90	1.00
A1	0.00	0.02	0.05
b	0.95	1.00	1.05
D		8.00	
E		8.00	
D2	7.05	7.20	7.30
E2	4.15	4.30	4.40
e		2.00	
L	0.40	0.50	0.60

Figure 20. PowerFLAT™ 8x8 HV recommended footprint



8222871\_REV\_C\_footprint

# 5 Packaging mechanical data

Figure 21. PowerFLAT™ 8x8 HV tape

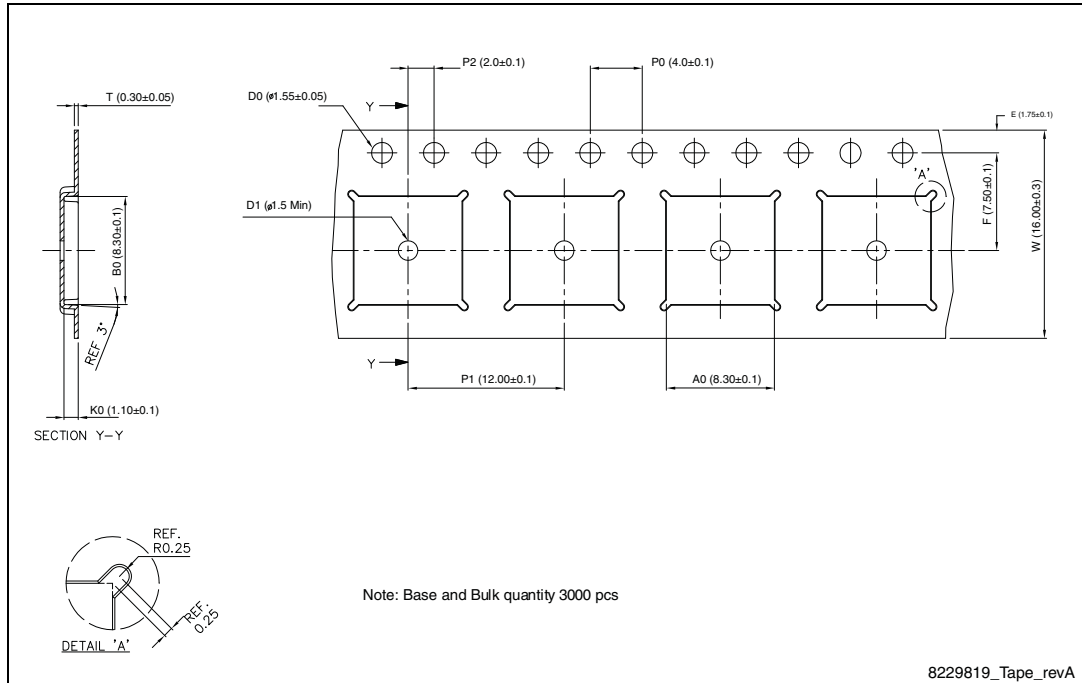


Figure 22. PowerFLAT™ 8x8 HV package orientation in carrier tape.

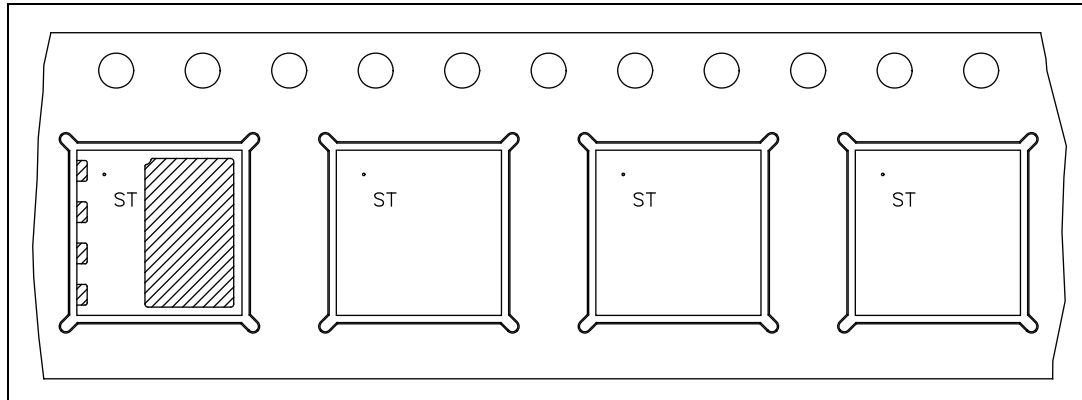
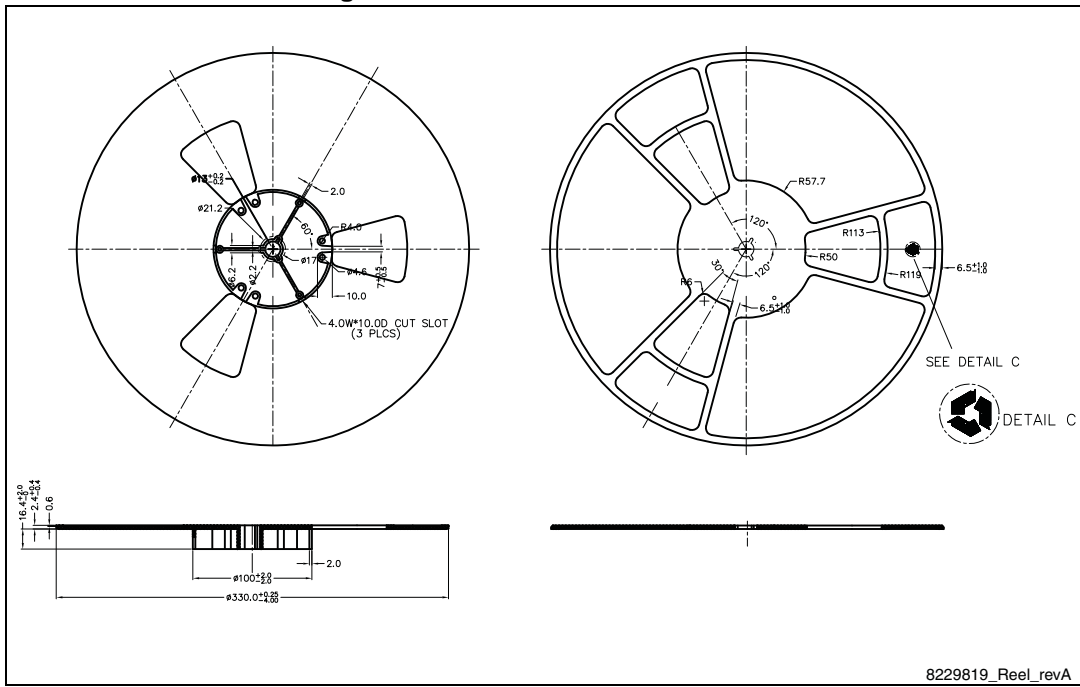


Figure 23. PowerFLAT™ 8x8 HV reel



8229819\_Reel\_revA

## 6 Revision history

**Table 9. Document revision history**

Date	Revision	Changes
28-Apr-2010	1	First release.
01-Mar-2013	2	<ul style="list-style-type: none"> <li>– <a href="#">Section 4: Package mechanical data</a> has been modified.</li> <li>– <a href="#">Section 2.1: Electrical characteristics (curves)</a> has been inserted.</li> <li>– Minor text changes.</li> </ul>
17-Dec-2014	3	<p>Minor text and formatting changes throughout document.</p> <p>On Cover page, updated Features and Description.</p> <p>In <a href="#">Table 2: Absolute maximum ratings</a>, changed Values for both <math>P_{TOT}</math> rows.</p> <p>In <a href="#">Table 7: Source drain diode</a>, changed Units for both <math>Q_{rr}</math> rows.</p> <p>In <a href="#">Figure 3: Thermal impedance</a>, added inset with plot and formulas.</p> <p>In <a href="#">Section 3: Test circuits</a>, updated figures.</p> <p>In <a href="#">Section 4: Package mechanical data</a>, updated figures and tables.</p>

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