

BLC8G27LS-160AV

Power LDMOS transistor

Rev. 4 — 2 December 2016

AMMPLÉON

Product data sheet

1. Product profile

1.1 General description

160 W LDMOS packaged asymmetrical Doherty power transistor for base station applications at frequencies from 2496 MHz to 2690 MHz.

Table 1. Typical performance

Typical RF performance at $T_{case} = 25$ °C in the Doherty demo board.

Test signal	f	V _{DS}	P _{L(AV)}	G _p	η _D	ACPR
	(MHz)	(V)	(W)	(dB)	(%)	(dBc)
1-carrier W-CDMA	2496 to 2690	28	31.6	14.5	43	-30 [1]

[1] Test signal: 3GPP test model 1; 1 to 64 DPCH; PAR = 7.2 dB at 0.01 % probability on CCDF.

1.2 Features and benefits

- Excellent ruggedness
- High efficiency
- Low thermal resistance providing excellent thermal stability
- Decoupling leads to enable improved video bandwidth
- Lower output capacitance for improved performance in Doherty applications
- Designed for low memory effects providing excellent pre-distortability
- Internally matched for ease of use
- Integrated ESD protection
- Compliant to Restriction of Hazardous Substances (RoHS) Directive 2002/95/EC

1.3 Applications

- RF power amplifier for W-CDMA base stations and multi carrier applications in the 2496 MHz to 2690 MHz frequency range

2. Pinning information

Table 2. Pinning

Pin	Description	Simplified outline	Graphic symbol
1	drain1 (main)		 aaa-007731
2	drain2 (peak)		
3	gate1 (main)		
4	gate2 (peak)		
5	video decoupling (main)		
6	video decoupling (peak)		
7	source [1]		

[1] Connected to flange.

3. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
BLC8G27LS-160AV	-	air cavity plastic earless flanged package; 6 leads	SOT1275-1

4. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DS}	drain-source voltage		-	65	V
V_{GS}	gate-source voltage		-0.5	+13	V
T_{stg}	storage temperature		-65	+150	°C
T_j	junction temperature [1]		-	225	°C

[1] Continuous use at maximum temperature will affect the reliability, for details refer to the online MTF calculator.

5. Thermal characteristics

Table 5. Thermal characteristics

Symbol	Parameter	Conditions	Typ	Unit
Main device				
$R_{th(j-case)}$	thermal resistance from junction to case	$T_{case} = 80\text{ °C}; V_{DS} = 28\text{ V}; I_{Dq} = 490\text{ mA}$		
		$P_L = 32\text{ W}$	0.509	K/W
		$P_L = 100\text{ W}$	0.363	K/W

Table 5. Thermal characteristics ...continued

Symbol	Parameter	Conditions	Typ	Unit
Peak device				
R _{th(j-case)}	thermal resistance from junction to case	T _{case} = 80 °C; V _{DS} = 28 V; I _{Dq} = 490 mA		
		P _L = 32 W	0.069	K/W
		P _L = 100 W	0.284	K/W

6. Characteristics

Table 6. DC characteristics

T_j = 25 °C unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Main device						
V _{(BR)DSS}	drain-source breakdown voltage	V _{GS} = 0 V; I _D = 0.9 mA	65	-	-	V
V _{GS(th)}	gate-source threshold voltage	V _{DS} = 10 V; I _D = 90 mA	1.5	1.9	2.3	V
V _{GSq}	gate-source quiescent voltage	V _{DS} = 28 V; I _D = 300 mA	1.6	2.0	2.4	V
I _{DSS}	drain leakage current	V _{GS} = 0 V; V _{DS} = 28 V	-	-	1.4	μA
I _{DSX}	drain cut-off current	V _{GS} = V _{GS(th)} + 3.75 V; V _{DS} = 10 V	-	17	-	A
I _{GSS}	gate leakage current	V _{GS} = 11 V; V _{DS} = 0 V	-	-	140	nA
g _{fs}	forward transconductance	V _{DS} = 10 V; I _D = 90 mA	-	0.78	-	S
R _{DS(on)}	drain-source on-state resistance	V _{GS} = V _{GS(th)} + 3.75 V; I _D = 3.15 A	-	174	260	mΩ
Peak device						
V _{(BR)DSS}	drain-source breakdown voltage	V _{GS} = 0 V; I _D = 1.1 mA	65	-	-	V
V _{GS(th)}	gate-source threshold voltage	V _{DS} = 10 V; I _D = 110 mA	1.5	1.9	2.3	V
V _{GSq}	gate-source quiescent voltage	V _{DS} = 28 V; I _D = 600 mA	1.6	2.0	2.4	V
I _{DSS}	drain leakage current	V _{GS} = 0 V; V _{DS} = 28 V	-	-	1.4	μA
I _{DSX}	drain cut-off current	V _{GS} = V _{GS(th)} + 3.75 V; V _{DS} = 10 V	-	20	-	A
I _{GSS}	gate leakage current	V _{GS} = 11 V; V _{DS} = 0 V	-	-	140	nA
g _{fs}	forward transconductance	V _{DS} = 10 V; I _D = 110 mA	-	0.97	-	S
R _{DS(on)}	drain-source on-state resistance	V _{GS} = V _{GS(th)} + 3.75 V; I _D = 3.85 A	-	145	215	mΩ

Table 7. RF characteristics

Test signal: 1-carrier W-CDMA; PAR = 7.2 dB at 0.01 % probability on the CCDF; 3GPP test model 1; 1 - 64 DPCH; f₁ = 2496 MHz; f₂ = 2690 MHz; RF performance at V_{DS} = 28 V; I_{Dq} = 250 mA (main); V_{GS(amp)peak} = 0.70 V; T_{case} = 25 °C; unless otherwise specified; in an asymmetrical Doherty production test circuit at 2496 MHz to 2690 MHz.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
G _p	power gain	P _{L(AV)} = 31.6 W	13.3	14.3	-	dB
RL _{in}	input return loss	P _{L(AV)} = 31.6 W	-	-13	-6	dB
η _D	drain efficiency	P _{L(AV)} = 31.6 W	36	41	-	%
ACPR	adjacent channel power ratio	P _{L(AV)} = 31.6 W	-	-30	-25	dBc

Table 8. RF characteristics

Test signal: 1-carrier W-CDMA; PAR = 7.2 dB at 0.01 % probability on the CCDF; 3GPP test model 1; 1 - 64 DPCH; f = 2690 MHz; RF performance at $V_{DS} = 28$ V; $I_{Dq} = 250$ mA (main); $V_{GS(amp)peak} = 0.7$ V; $T_{case} = 25$ °C; unless otherwise specified; in an asymmetrical Doherty production test circuit at 2496 MHz to 2690 MHz.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
PAR _O	output peak-to-average ratio	$P_{L(AV)} = 63$ W	3.75	4.7	-	dB
P _{L(M)}	peak output power		146	170	-	W

7. Test information

7.1 Ruggedness in Doherty operation

The BLC8G27LS-160AV is capable of withstanding a load mismatch corresponding to a VSWR = 10 : 1 through all phases under the following conditions: $V_{DS} = 28$ V; $I_{Dq} = 250$ mA (main); $V_{GS(amp)peak} = 0.7$ V; $P_L = 120$ W (CW); f = 2496 MHz.

7.2 Impedance information

Table 9. Typical impedance of main device

Measured load-pull data of main device; $I_{Dq} = 570$ mA (main); $V_{DS} = 28$ V.

f (MHz)	Z _S [1] (Ω)	Z _L [1] (Ω)	P _L [2] (W)	η _D [2] (%)	G _p [2] (dB)
Maximum power load					
2496	2 – j6.9	1.6 – j7.6	109	56	13.7
2600	3 – j7	1.5 – j8.1	107	52.8	13.9
2690	5.2 – j8.7	1.5 – j8.1	103	54.6	14.8
Maximum drain efficiency load					
2496	2 – j6.9	2.6 – j6.6	89	64	15.6
2600	3 – j7	2.6 – j6.6	79	63	16.5
2690	5.2 – j8.7	2.1 – j7.1	81	61	16.7

[1] Z_S and Z_L defined in [Figure 1](#).

[2] at 3 dB gain compression.

Table 10. Typical impedance of peak device

Measured load-pull data of peak device; $I_{Dq} = 680$ mA (peak); $V_{DS} = 28$ V.

f (MHz)	Z _S [1] (Ω)	Z _L [1] (Ω)	P _L [2] (W)	η _D [2] (%)	G _p [2] (dB)
Maximum power load					
2496	2 – j6.9	3.3 – j8.3	128	56.9	15.2
2600	3 – j7	3.3 – j8.3	118	57	15.6
2690	5.2 – j8.7	4 – j10	120	52.5	15.6

Table 10. Typical impedance of peak device ...continued

Measured load-pull data of peak device; $I_{Dq} = 680 \text{ mA (peak)}$; $V_{DS} = 28 \text{ V}$.

f	Z _S [1]	Z _L [1]	P _L [2]	η _D [2]	G _p [2]
(MHz)	(Ω)	(Ω)	(W)	(%)	(dB)
Maximum drain efficiency load					
2496	2 – j6.9	3.5 – j5.8	94	63	17
2600	3 – j7	3.5 – j5.8	83	60	17.7
2690	5.2 – j8.7	3.3 – j7.7	97	59	17.4

[1] Z_S and Z_L defined in [Figure 1](#).

[2] at 3 dB gain compression.

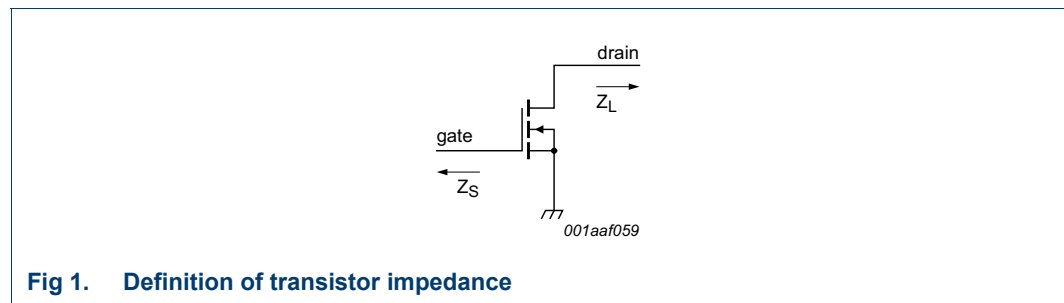


Fig 1. Definition of transistor impedance

7.3 Recommended impedances for Doherty design

Table 11. Typical impedance of main device at 1 : 1 load

Measured load-pull data of main device; $I_{Dq} = 570 \text{ mA (main)}$; $V_{DS} = 28 \text{ V}$.

f	Z _S [1]	Z _L [1]	P _L [2]	η _D [3]	G _p [3]
(MHz)	(Ω)	(Ω)	(dBm)	(%)	(dB)
2496	2 – j6.9	2.7 – j7.1	49.7	40	18.5
2600	3 – j7	2.7 – j7.1	49.4	41	19.3
2690	5.2 – j8.7	2.7 – j7.1	49.1	42	19.5

[1] Z_S and Z_L defined in [Figure 1](#).

[2] at 3 dB gain compression.

[3] at P_{L(AV)} = 44.5 dBm.

Table 12. Typical impedance of main device at 1 : 2.5 load

Measured load-pull data of main device; $I_{Dq} = 750 \text{ mA (main)}$; $V_{DS} = 28 \text{ V}$.

f	Z _S [1]	Z _L [1]	P _L [2]	η _D [3]	G _p [3]
(MHz)	(Ω)	(Ω)	(dBm)	(%)	(dB)
2496	2 – j6.9	2.9 – j4.5	44.56	48	19.8
2600	3 – j7	2.9 – j4.5	44.44	53	20.9
2690	5.2 – j8.7	3 – j4.9	44.5	50.3	20.8

[1] Z_S and Z_L defined in [Figure 1](#).

[2] at 3 dB gain compression.

[3] at P_{L(AV)} = 44.5 dBm.

7.4 VBW in Doherty operation

The BLC8G27LS-160AV shows 130 MHz (typical) video bandwidth in Doherty demo board in 2600 MHz at $V_{DS} = 28\text{ V}$; $I_{Dq} = 250\text{ mA}$ and $V_{GS(amp)peak} = 0.8\text{ V}$.

7.5 Test circuit

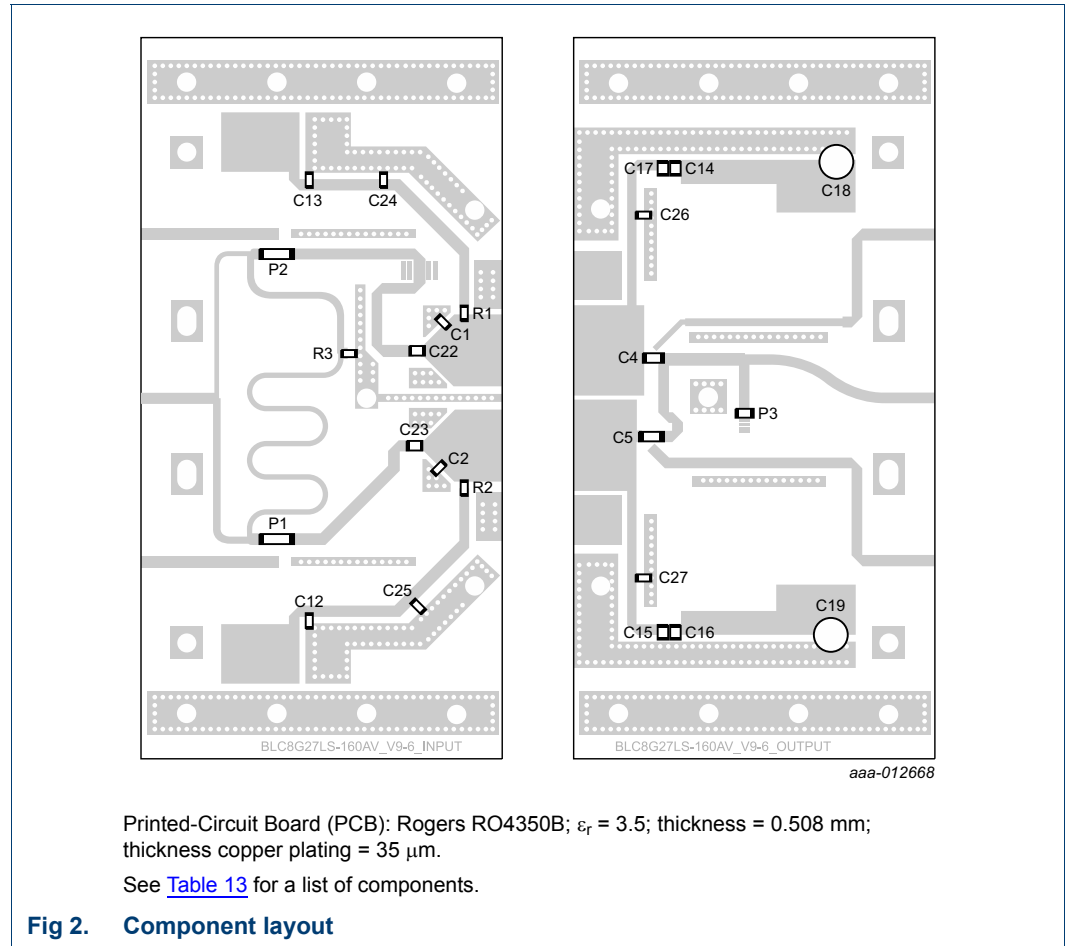
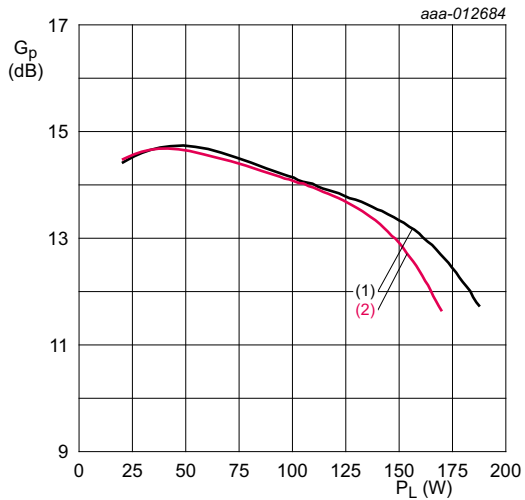


Table 13. List of components
See [Figure 2](#) for component layout.

Component	Description	Value	Remarks
C1, C2	multilayer ceramic chip capacitor	0.3 pF	ATC 600F
C4	multilayer ceramic chip capacitor	3.3 pF	ATC 600F
C5, C22, C23, C24, C25, C26, C27	multilayer ceramic chip capacitor	10 pF	ATC 600F
C12, C13	multilayer ceramic chip capacitor	1 μF	Murata, SMD 1206
C14, C15, C16, C17	multilayer ceramic chip capacitor	10 μF	Murata, SMD 1206
C18, C19	electrolytic capacitor	2200 μF , 63 V	BCcomponents
P1, P2, P3	copper foil strip	-	needed for tuning
R1, R2	resistor	5.1 Ω	SMD 0805

7.6 Graphical data

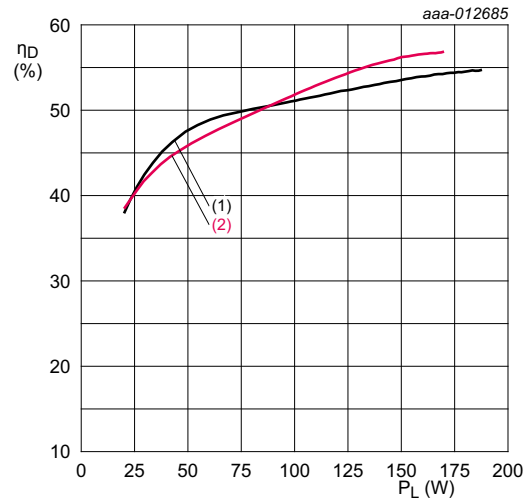
7.6.1 Pulsed CW



$V_{DS} = 28\text{ V}$; $I_{Dq} = 250\text{ mA}$ (main device);
 $V_{GS(amp)peak} = 0.65\text{ V}$; $t_p = 100\text{ }\mu\text{s}$; $\delta = 10\text{ }\%$.

- (1) $f = 2496\text{ MHz}$
- (2) $f = 2690\text{ MHz}$

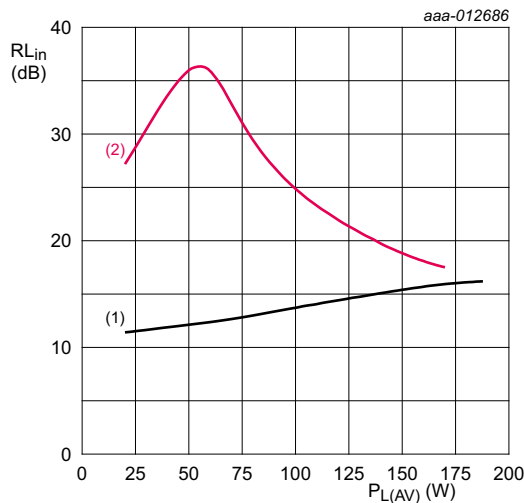
Fig 3. Power gain as a function of output power; typical values



$V_{DS} = 28\text{ V}$; $I_{Dq} = 250\text{ mA}$ (main device);
 $V_{GS(amp)peak} = 0.65\text{ V}$; $t_p = 100\text{ }\mu\text{s}$; $\delta = 10\text{ }\%$.

- (1) $f = 2496\text{ MHz}$
- (2) $f = 2690\text{ MHz}$

Fig 4. Drain efficiency as a function of output power; typical values

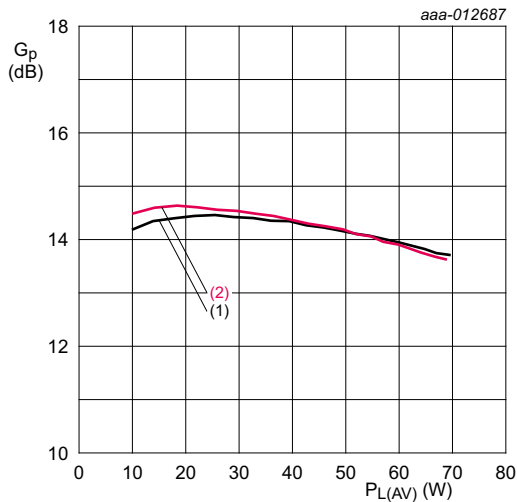


$V_{DS} = 28\text{ V}$; $I_{Dq} = 250\text{ mA}$ (main device); $V_{GS(amp)peak} = 0.65\text{ V}$; $t_p = 100\text{ }\mu\text{s}$; $\delta = 10\text{ }\%$.

- (1) $f = 2496\text{ MHz}$
- (2) $f = 2690\text{ MHz}$

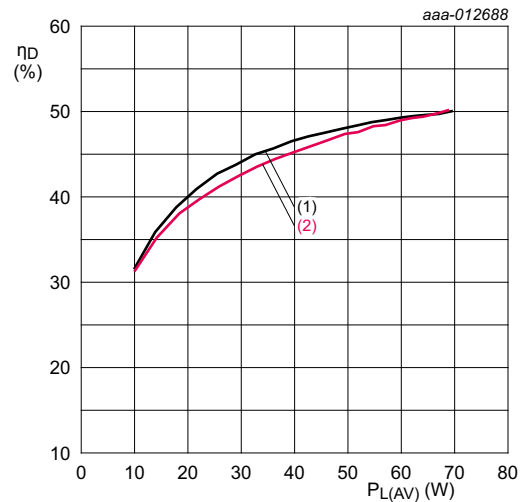
Fig 5. Input return loss as a function of average output power; typical values

7.6.2 1-Carrier W-CDMA



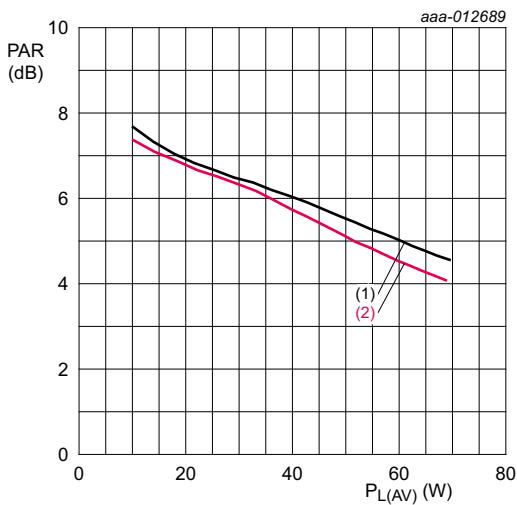
$V_{DS} = 28\text{ V}; I_{DQ} = 250\text{ mA}$ (main device);
 $V_{GS(amp)peak} = 0.65\text{ V}$.
 (1) $f = 2496\text{ MHz}$
 (2) $f = 2690\text{ MHz}$

Fig 6. Power gain as a function of average output power; typical values



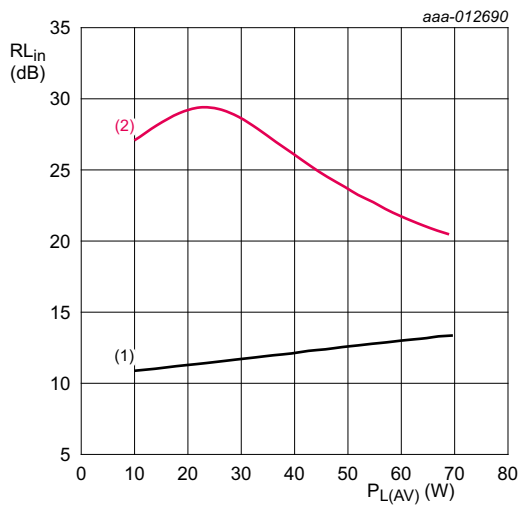
$V_{DS} = 28\text{ V}; I_{DQ} = 250\text{ mA}$ (main device);
 $V_{GS(amp)peak} = 0.65\text{ V}$.
 (1) $f = 2496\text{ MHz}$
 (2) $f = 2690\text{ MHz}$

Fig 7. Drain efficiency as a function of average output power; typical values



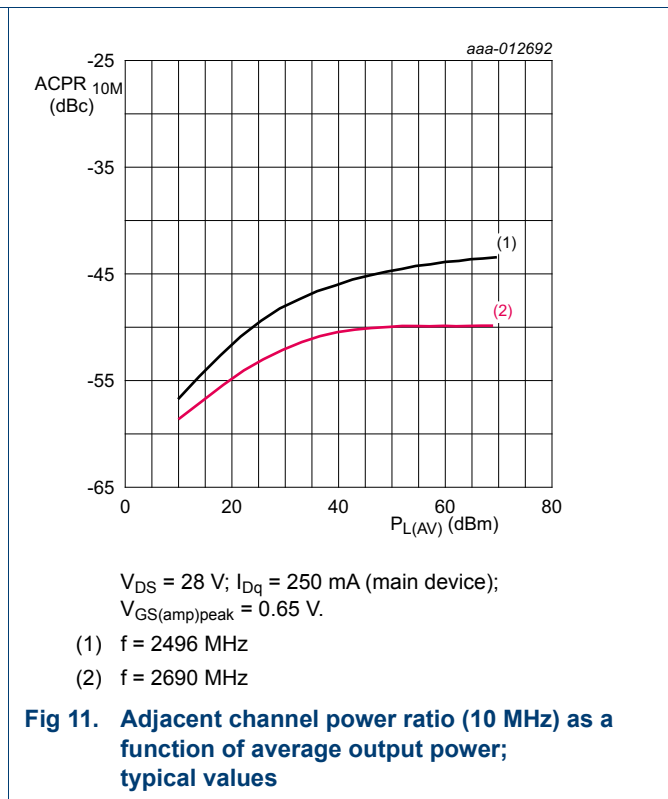
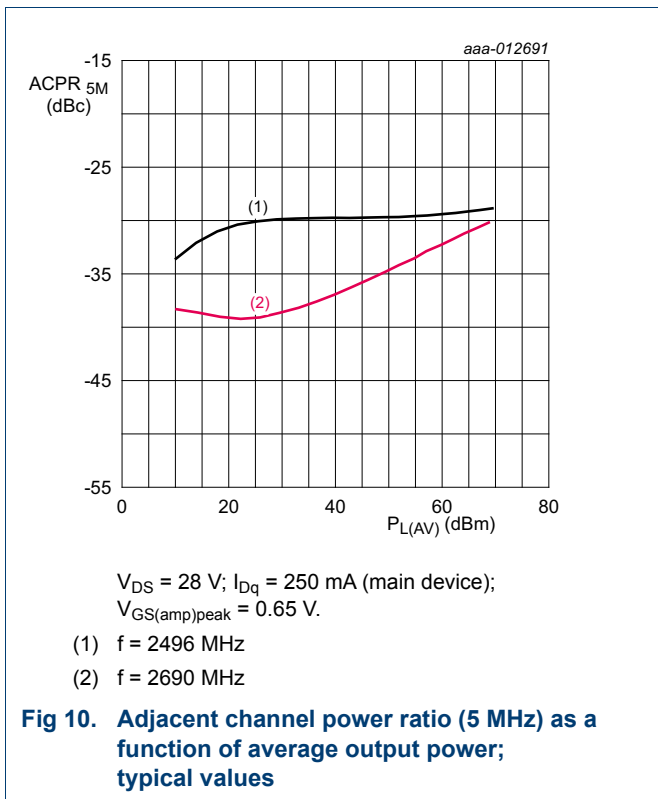
$V_{DS} = 28\text{ V}; I_{DQ} = 250\text{ mA}$ (main device);
 $V_{GS(amp)peak} = 0.65\text{ V}$.
 (1) $f = 2496\text{ MHz}$
 (2) $f = 2690\text{ MHz}$

Fig 8. Peak-to-average power ratio as a function of average output power; typical values

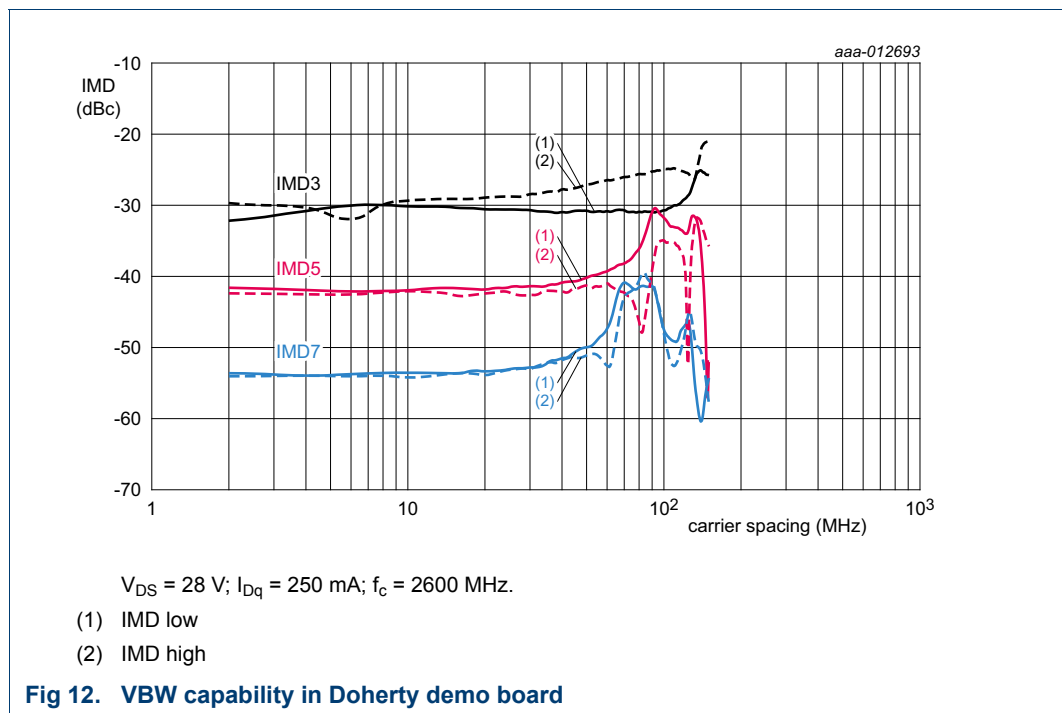


$V_{DS} = 28\text{ V}; I_{DQ} = 250\text{ mA}$ (main device);
 $V_{GS(amp)peak} = 0.65\text{ V}$.
 (1) $f = 2496\text{ MHz}$
 (2) $f = 2690\text{ MHz}$

Fig 9. Input return loss as a function of average output power; typical values



7.6.3 2-Tone VBW



8. Package outline

Air cavity plastic earless flanged package; 6 leads

SOT1275-1

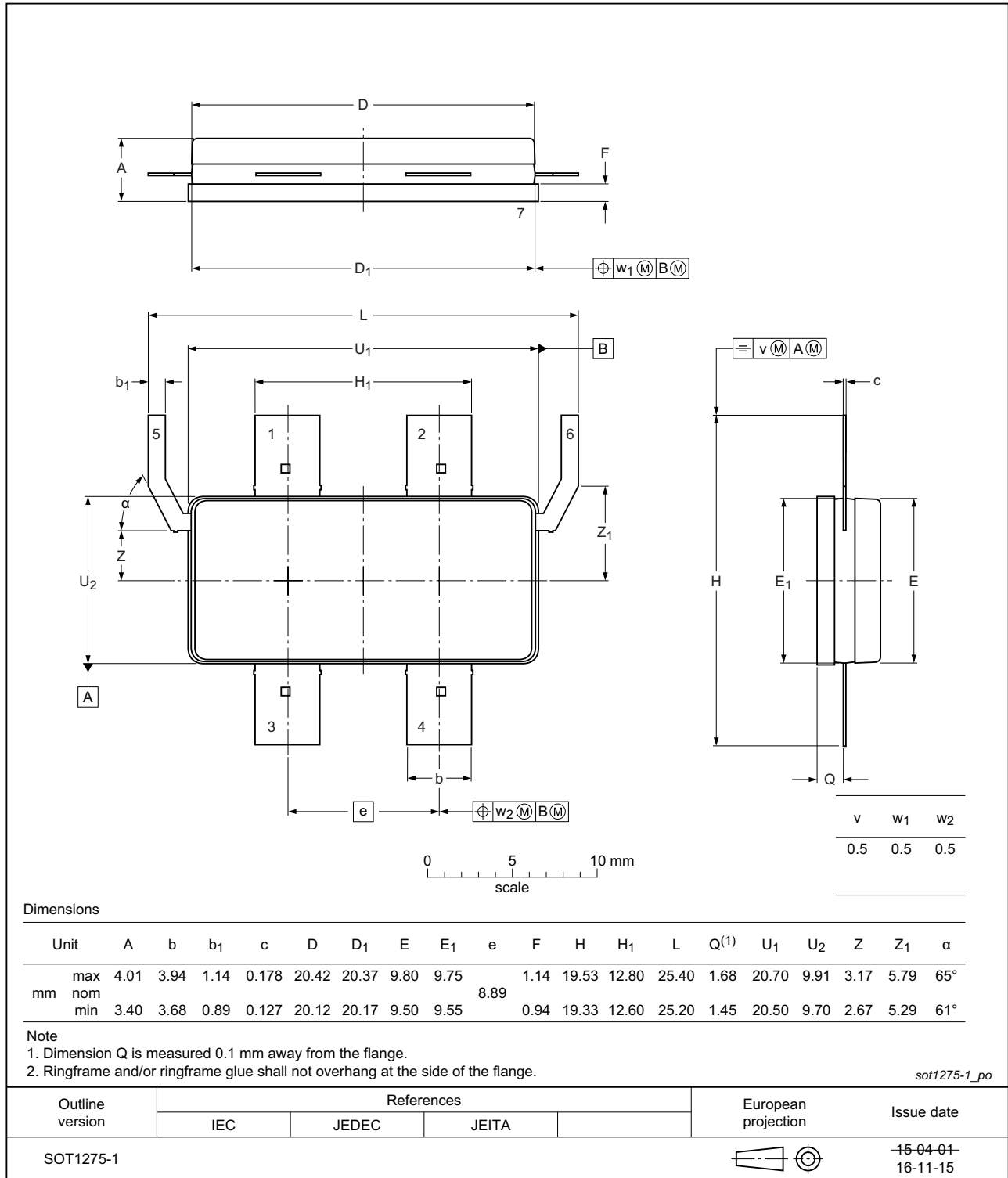


Fig 13. Package outline SOT1275-1

9. Handling information

CAUTION



This device is sensitive to ElectroStatic Discharge (ESD). Observe precautions for handling electrostatic sensitive devices.

Such precautions are described in the *ANSI/ESD S20.20*, *IEC/ST 61340-5*, *JESD625-A* or equivalent standards.

Table 14. ESD sensitivity

ESD model	Class
Charged Device Model (CDM); According to ANSI/ESDA/JEDEC standard JS-002	C2A [1]
Human Body Model (HBM); According to ANSI/ESDA/JEDEC standard JS-001	2 [2]

[1] CDM classification C2A is granted to any part that passes after exposure to an ESD pulse of 500 V, but fails after exposure to an ESD pulse of 750 V.

[2] HBM classification 2 is granted to any part that passes after exposure to an ESD pulse of 2000 V, but fails after exposure to an ESD pulse of 4000 V.

10. Abbreviations

Table 15. Abbreviations

Acronym	Description
3GPP	3rd Generation Partnership Project
CCDF	Complementary Cumulative Distribution Function
CW	Continuous Wave
DPCH	Dedicated Physical CHannel
ESD	ElectroStatic Discharge
LDMOS	Laterally Diffused Metal-Oxide Semiconductor
MTF	Median Time to Failure
PAR	Peak-to-Average Ratio
SMD	Surface Moulded Device
VBW	Video BandWidth
VSWR	Voltage Standing Wave Ratio
W-CDMA	Wideband Code Division Multiple Access

11. Revision history

Table 16. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
BLC8G27LS-160AV v.4	20161202	Product data sheet	-	BLC8G27LS-160AV v.3
Modifications:	<ul style="list-style-type: none"> Figure 13 on page 10: updated package outline drawing SOT1275-1 Section 9 on page 11: updated Handling information 			
BLC8G27LS-160AV v.3	20150901	Product data sheet	-	BLC8G27LS-160AV v.2
BLC8G27LS-160AV v.2	20140603	Product data sheet	-	BLC8G27LS-160AV v.1
BLC8G27LS-160AV v.1	20130523	Objective data sheet	-	-

12. Legal information

12.1 Data sheet status

Document status ^{[1][2]}	Product status ^[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL <http://www.ampleon.com>.

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13. Contact information

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